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Radiation-Tolerant All-Digital PLL/CDR with Varactorless LC DCO in 65 nm CMOS

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Abstract: This paper presents the first fully integrated radiation-tolerant All-Digital Phase-Locked Loop (PLL) and Clock and Data Recovery (CDR) circuit for wireline communication applications. Several radiation hardening techniques are proposed to achieve state-of-the-art immunity to Single-Event Effects (SEEs) up to 62.5 MeV cm^2 mg^{-1} as well as tolerance to the Total Ionizing Dose (TID) exceeding 1.5 Grad. The LC Digitally Controlled Oscillator (DCO) is implemented without MOS varactors, avoiding the use of a highly SEE sensitive circuit element. The circuit is designed to operate at reference clock frequencies from 40 MHz to 320 MHz or at data rates from 40 Mbps to 320 Mbps and displays a jitter performance of 520 fs with a power dissipation of only 11 mW and an FOM of −235 dB.

Keywords: All-Digital; PLL; CDR; Single-Event Effects; radiation hardening

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1. Introduction

Phase-locked loops, including Clock/Data Recovery circuits, play an important role in the reliability of radiation tolerant systems, being typically responsible for providing and conditioning clocks of high spectral purity and stability. With the emergence of ever more stringent timing precision and stability requirements in both High Energy Physics applications [1] as well as communications circuits for space applications [2], PLLs operating in radiation environments need to provide radiation tolerance without sacrificing performance.

Without extensive circuit hardening efforts, conventional PLL architectures have been found to be sensitive to ionizing radiation, both with regards to SEE as well as TID effects. While their SEE sensitivity is the origin of transient but recoverable fault conditions, the sensitivity to TID ultimately limits the application of these circuits in harsh radiation environments, where reliable operation must be sustained up to radiation doses exceeding 1 Grad [3].

All-Digital Phase-Locked Loop (ADPLL) architectures offer a unique opportunity to eliminate many of these sensitivities and therefore improve radiation tolerant PLL circuits in multiple regards: Firstly, most sensitive analog circuits can be replaced with their digital counterparts. While the design and hardening of analog circuit components in advanced technology nodes become more difficult to accomplish, digital circuits can be hardened against SEE systematically using techniques such as Triple Modular Redundancy (TMR) and temporal redundancy [4], while continuing to exploit the performance gain these nodes provide. At the same time, all-digital architectures allow the tight integration of Digital Signal Processing (DSP) algorithms, which may be leveraged to achieve improved

locking times or robust circuit calibration capabilities [5]. Being implemented with digital circuits, such functionalities can become intrinsically immune to TID degradation.

In this article, we propose an All-Digital PLL circuit tolerant to SEE and high TID, which is based on a varactorless LC DCO implemented in a 65 nm CMOS technology. We augment the classical ADPLL architecture with the inclusion of SEE protection for all digital circuit components. To accomplish this goal, we take advantage of the availability of systematic SEE hardening techniques for digital circuits. The LC DCO, which constitutes the sole remaining mixed signal circuit component, is implemented without MOS varactors, which we show to be a beneficial implementation in radiation environments. The chosen architecture eliminates conceptual SEE sensitivities found in conventional PLLs, while, at the same time, significantly reducing the impact of TID, enabling the use of PLL circuits in challenging radiation environments. As a case study, the proposed circuit targets common clocking requirements of the High Luminosity Large Hadron Collider (HL-LHC) experiments. These systems typically operate on a reference clock or data stream derived from a 40 MHz bunch crossing clock and often simultaneously require multiple low-jitter clocks up to 1.28 GHz.

The remainder of this paper is organized as follows: Section 2 gives an overview of radiation effects in conventional PLL architectures. Section 3 motivates the application of an All-Digital PLL architecture to systematically mitigate radiation effects, including the proposal of suitable hardening techniques. Section 4 describes the circuit implementation, and Section 5 presents the measurements of the circuit performance and radiation tolerance.

2. Radiation Effects in Conventional PLL Designs

Radiation effects in conventional PLL designs have been the focus of numerous studies in the past. We limit the discussion of radiation effects to circuits based on LC tank Voltage-Controlled Oscillators (VCOs) as this topology is most often chosen for low power and low phase noise circuit implementations. Conventional PLL circuits are comprised of a linear Phase-Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF), LC VCO and a feedback divider, which closes the feedback loop. Following the general classification of radiation effects in integrated circuits, we can separate their sensitivity to radiation into transient (SEE) and cumulative (TID) effects [6]. SEE in particular can be divided into two relevant classes: Single-Event Upsets (SEUs) refer to events altering the state of memory elements, which remain persistent until overwritten or corrected. On the other hand, Single-Event Transients (SETs) specifically refer to temporary changes in voltages or logic levels that recover without further intervention. Both effects, when not mitigated, can have catastrophic impact on the operation of digital circuits.

First, considering only single-event effects, a number of shortcomings of the conventional PLL architecture have been reported in the past. The PFD containing digital storage elements is generally sensitive to SEUs. Even though an upset in the PFD persists for, at most, one reference clock cycle, it may cause the charge pumps to remain enabled for a significant amount of time, which are otherwise (in steady state operation) only active for a very short period each reference clock cycle. Bit flips can also corrupt the state of the PFD, which results in cycle slips [7,8]. This sensitivity can be largely mitigated by the protection of the PFD using TMR [7]. A similar reasoning can be applied to the feedback divider: Corruption of any of the memory elements in the divider results in a phase jump of the feedback clock. This phase error subsequently needs to be corrected by the feedback loop. Again, a mitigation can be found in TMR implementations of the divider [7,9] or by applying Radiation-Hardened-by-Design (RHBD) techniques, such as Double Interlocked Cell (DICE) implementations for memory elements [10].

Another contributor to SEE sensitivity may be found in the charge pump driving the loop filter [8,11]. Current-based charge pumps specifically suffer from long recovery times after SETs due to their limited rate of charge evacuation, which again results in large accumulated phase and frequency errors. This sensitivity has been mitigated, for example, by the use of a tri-state voltage charge pump architecture, which reduces the number of

sensitive nodes and increases the rate of charge sourcing/sinking [12,13] at the cost of poor reference-spurs and process, voltage and temperature (PVT) sensitive static phase errors.

Finally, the LC VCO has been identified as a critical component sensitive to SEEs. Charge collection at the bias current source transistor drain node can be shown to result in a temporary reduction of oscillation amplitude and frequency [14,15]. This sensitivity can be significantly reduced by the addition of capacitance to this node [14]. Another sensitivity is located at the VCO tuning node. Typical MOS varactor tuning architectures have been found to be sensitive to charge collection, as reported in [16]. This sensitivity can be mitigated by adopting a modified tuning topology [9], which, however, has the drawback of introducing an additional pole at the tuning node of the VCO.

With regards to TID, the VCO and CP circuits can be identified as the main contributors to performance degradation. The degradation of the PLL's digital circuits (PFD and feedback divider) has no impact on PLL performance as long as timing requirements (setup/hold) are met. The degradation of the devices forming the VCO amplifier results in a reduction in their transconductance. This reduces the oscillation amplitude, which, through the presence of voltage-dependent capacitances at the oscillator nodes, is converted into a significant change of oscillation frequency [16]. Compensating for this shift in oscillation frequency requires extending the VCO tuning range to support operation at high doses. Furthermore, the reduced transconductance of the VCO amplifier will eventually result in failure to start or sustain stable oscillation. Another concern is the degradation of the active devices in the charge pump. A reduction in their current results in a reduction in loop gain, which reduces the bandwidth and damping of the closed-loop transfer function.

3. Radiation-Tolerant All-Digital PLL and CDR Architecture

The All-Digital PLL architecture offers an opportunity for the systematic elimination of many of the sensitivities that the conventional PLL architecture contains. The general SEE sensitivity of different All-Digital PLL architectures without any applied hardening strategies has been reported in the literature before [17,18]. Two analyses have shown that a bang-bang-ADPLL architecture, which lends itself to implementations of Integer-N PLL and CDR circuits, already exhibits inherent robustness due to its nonlinear phase detector. In such an architecture, the Digital Loop Filter (DLF) presents a critical SEE sensitivity, as SEUs may corrupt the frequency error information stored in the loop filter integrator registers. Prior work addressing SEE sensitivity of ADPLL demonstrated its findings using simulations and fault injection into non-hardened circuit implementations [19], but no radiation-tolerant implementation has been demonstrated experimentally. Possible design trade-offs and implementation aspects of hardening techniques were not addressed, and LC DCOs have been excluded from the discussion as a source of SEE.

As outlined earlier, digital circuits can generally be reliably protected against SEEs using redundancy techniques, such as TMR. Taking this into account, we propose a circuit architecture following Figure 1. Depending on the mode of operation, either a D-Flip-Flop (PLL operation) or an Alexander Phase Detector [20] (CDR operation) is used as a single bit phase detector. We propose to only use a single phase detector without any internal redundancy (TMR). A corruption of the phase detector output by SEE will only persist for a single reference clock cycle. Such an error can be tolerated to propagate through the loop, as it does not result in an appreciable phase error of the loop. Since both types of Bang-Bang Phase Detectors (BBPDs) do not offer frequency detection capability, a Frequency Counter (FCNT) is used during acquisition to bring the DCO frequency close to the reference clock frequency before enabling closed-loop control. An Acquisition Finite State Machine (FSM) is implemented for this purpose.

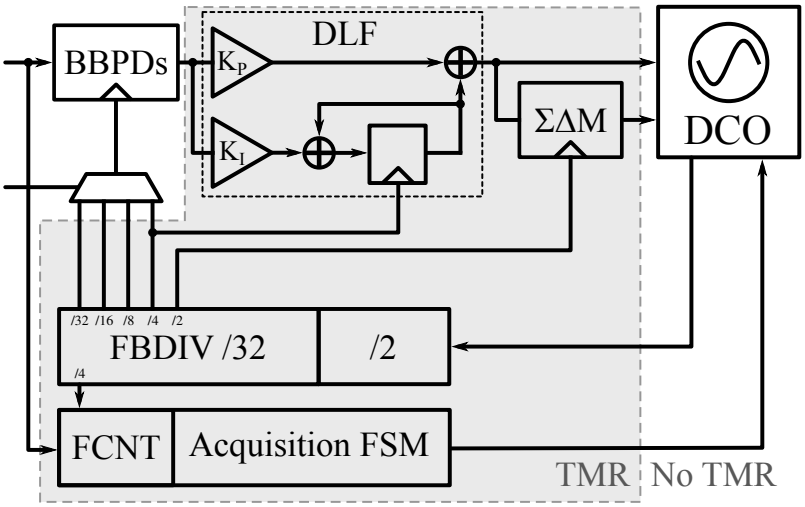

Figure 1. Architecture of the proposed All-Digital PLL/CDR circuit. All synchronous digital loop components are protected using TMR, only the DCO and BBPD remain without redundancy.

The proportional-integral digital loop filter replaces both the charge pump and loop filter circuits present in the conventional PLL architecture. Both the TID-stimulated degradation of the CP currents, as well as the sensitivity of the CP output switches to SEE discussed above, can be systematically removed by replacing the charge pumps with a digital filter. The SEE sensitivity of the DLF identified in [17] is mitigated by applying TMR protection to this circuit. A TMR protection scheme is also used in the ΣΔ-modulator, which is employed to improve frequency resolution and shift tuning quantization noise to high frequencies, where it is effectively filtered by the DCO transfer function [21]. A second-order Sigma-Delta Modulator (ΣΔM) is used, providing sufficient self-dithering during closed-loop operation to avoid the generation of spurious tones.

To achieve good phase noise performance, an LC tank oscillator is chosen as the DCO topology. Addressing both the sensitivity to SET and TID of the conventional LC VCO, the LC DCO is implemented without using MOS varactors. Other reported DCO designs utilize small MOS varactors with nonlinear control [5]; however, varactorless implementation has also been reported before [22,23]. By exclusively utilizing Metal-Oxide-Metal (MOM) capacitors fabricated using the highly controlled metallization processes available in CMOS technologies, sufficient tuning range, linearity and frequency resolution can be achieved. Avoiding the use of MOS varactors eliminates their inherent susceptibility to charge collection and therefore a potential SEE sensitivity of the circuit. At the same time, the capacitance of MOM structures offers reduced voltage-dependence, which reduces supply voltage sensitivity and limits TID-stimulated oscillator frequency shift. The DCO can additionally benefit from the omission of linearly controlled varactors as it eliminates a significant contributor to oscillator phase noise through the AM-PM conversion process of the voltage noise present on their tuning node [24], for instance, from the tail current source or supply voltage.

Finally, a synchronous binary counter divider is used in the PLL feedback path. The synchronous implementation lends itself to hardening against SEE using TMR in a similar way as the other digital loop components. To the advantage of our application, it also provides access to intermediate frequencies of the divider, which can be used for clocking the digital loop components (DLF and DCO ΣΔ-modulator) and allows flexible selection of the reference clock frequency and data rate.

4. Implementation

The proposed circuit was manufactured in a commercial 65 nm CMOS process with a nominal supply voltage of 1.2 V. The circuit occupies a total area of 0.28 mm^2, of which only

0.03 mm^2 (11%) is active area occupied by the digital loop components. A photomicrograph of the manufactured circuit is shown in Figure 2.

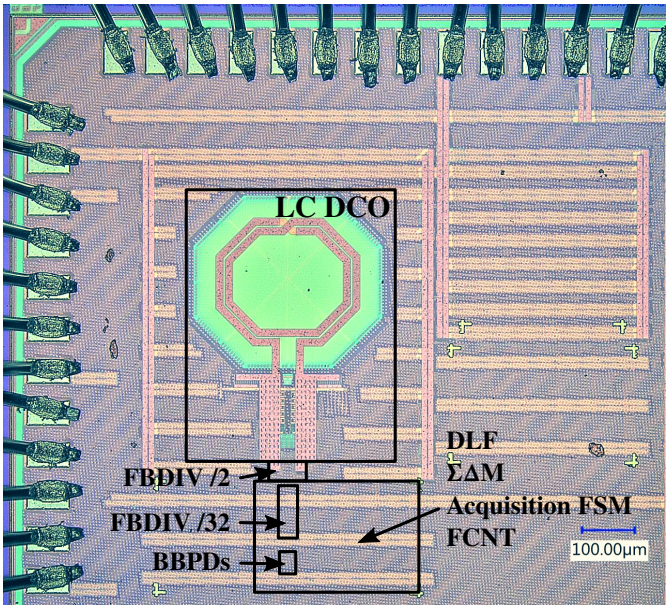

Figure 2. Photomicrograph of the All-Digital PLL/CDR circuit. The LC DCO occupies the majority of the circuit area. Critical digital components are implemented as small cells, while the remaining logic implemented in a sea-of-logic fashion.

4.1. LC DCO

To synthesize output frequencies between 40 MHz and 1280 MHz, an LC DCO operating at 2.56 GHz was designed. When considering the overall area, inductor quality factor and power consumption of the DCO and clock divider, this center frequency provides a suitable trade-off. The 2.56 GHz center frequency is low enough to allow the implementation of all dividers in the feedback path using CMOS circuits. This reduces power consumption and complexity compared to the Current-Mode Logic (CML) implementations often used at higher frequencies, such as, for the 5.12 GHz oscillator presented in [9]. A differential oscillator topology using cross-coupled NMOS and PMOS pairs is used, as shown conceptually in Figure 3. Bias current is provided by an NMOS tail current source. Because of the limited voltage swing this architecture produces, thin-oxide transistors can be used for the cross-coupled pair without reliability concerns and with the added benefit of their improved TID tolerance compared to the thick-oxide devices [25] required for larger oscillation amplitudes. Similar to DCO designs, such as [21], a coarse capacitor bank is used to cover PVT-related differences of the oscillator center frequency. An acquisition bank with improved resolution allows centering the fine tracking bank, which is then used for closed-loop operation. The PVT and acquisition bank settings are established during start-up using the FCNT acquisition FSM to remove large DCO frequency errors.

To cover the expected process and TID-related variations, the DCO is designed for a tuning range of 20%. This range is covered by the coarse PVT bank (C_{PVT}), which is segmented into four binary weighted LSB cells and four additional thermometric MSB cells. Each cell is implemented using MOM capacitors and NMOS switches, with the smallest binary cell implementing a 12.5 fF capacitance difference corresponding to a frequency step size of 6.5 MHz at 2.56 GHz. A smaller acquisition bank (C_{ACQ}) offers additional frequency tuning capabilities. To ensure optimal frequency centering of the small tracking bank (C_{TRK}) used for closed-loop control, the acquisition bank is implemented using 64 thermometric cells. Each unit cell adds 600 aF of capacitance to the tank when enabled, providing a frequency step size of 320 kHz. Both the PVT and the acquisition bank cells are implemented using the bottom-pinning switch architecture presented in [26]. A circuit

schematic is shown in Figure 4. Foundry MOM capacitors, C_{MOM}, and NMOS switch devices, M_{SW}, are used.

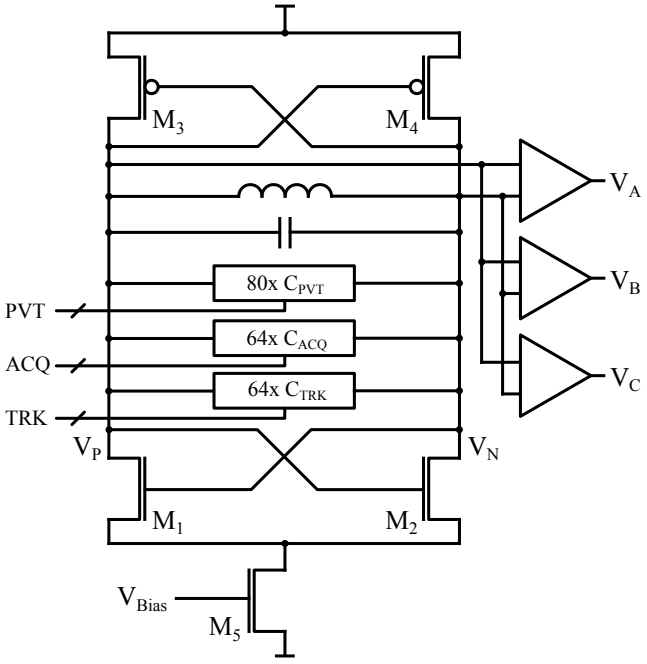

Figure 3. Schematic of the digitally controlled LC oscillator with redundant output buffers. Its frequency is controlled using PVT, acquisition (ACQ) and tracking (TRK) banks. Only the tracking bank is used for closed-loop control.

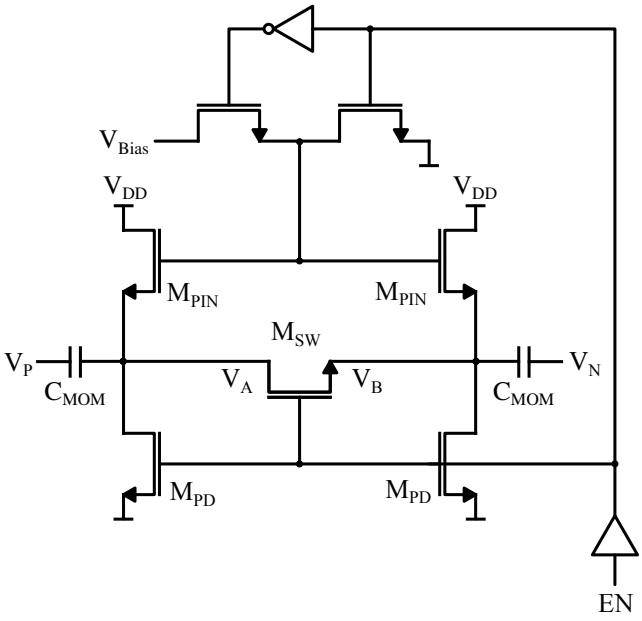

Figure 4. Digitally switched capacitor cells with bottom-pinning biasing [26]. When the main switch transistor M_{SW} is turned off, the NMOS pinning devices M_{PIN} fix the minimum of the oscillation voltage waveform close to the negative supply potential.

To avoid the degradation of the DCO phase noise and to minimize the production of spurious spectral components during closed-loop operation, the tracking bank needs to provide both fine-frequency resolution and high linearity. A custom MOM finger capacitor unit cell is utilized for frequency control. The implementation of this cell is shown in Figure 5. It is composed of four parallel minimum-width metal fingers, stacked across

two metallization layers. A grounded poly-silicon shield is implemented below the cell to minimize substrate noise coupling. The two outer metal fingers are connected to the tank oscillation nodes. To digitally modulate the capacitance of this cell, the inner two fingers can be shorted electrically using an NMOS switch, removing a single finger-to-finger capacitance from the tank. Using this arrangement, a capacitance difference of 66 aF can be realized, which provides a 35 kHz frequency resolution of the DCO. This tuning resolution is sufficient considering the phase noise performance of the oscillator and the adopted ΣΔM configuration. The high linearity of the tracking bank is achieved by 64 unit cells placed in a regular and closely matched layout. The capacitor configuration was designed using 2.5D electromagnetic simulations.

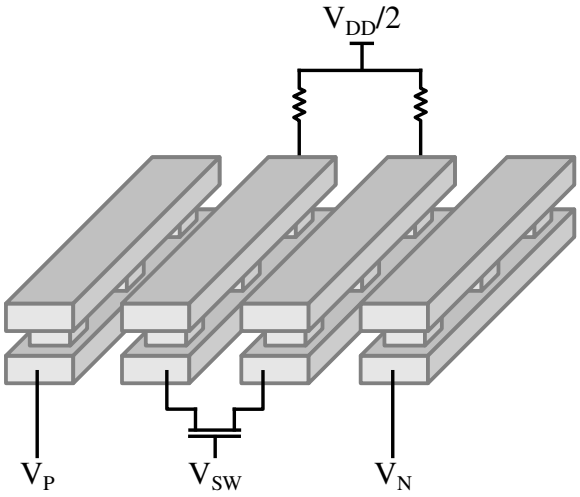

Figure 5. The implementation of the tracking bank custom MOM capacitor cells. Digital control of the cell capacitance is implemented by electrically connecting the innermost two fingers using an NMOS switch.

The DCO is equipped with three identical output buffers, which allows for hardening the remainder of the circuit against SEE using full TMR. These buffers also implement the conversion from differential to single-ended signalling.

4.2. Divide-by-Two Prescaler

Co-integrated with the redundant output buffers and differential to single-ended conversion is a divide-by-two True Single Phase Clock (TSPC) prescaler circuit. To mitigate SEE susceptibility, the prescaler is protected by full TMR, including triplicated voters in the feedback path. To allow sustaining operation at high levels of TID, the prescaler is implemented using a custom high-speed cell library utilizing Enclosed Layout Transistor (ELT) devices [27]. Since the critical path of this prescaler consists only of a single majority voter and the D-Flip-Flop setup time, the prescaler retains significant margins for TID degradation. Three single-ended 1.28 GHz clock signals are provided at the prescaler output.

4.3. Clocking and Clock Distribution

All digital loop components are clocked using frequencies generated by the Feedback Divider (FBDIV). As this divider is protected using TMR, it also provides three replicas of each clock frequency, which allows implementing a full TMR scheme with triplicated clocks. Full triplicating of the clock signals is necessary to mitigate the simultaneous corruption of redundant memory elements by SET affecting their common clock tree, which has catastrophic consequences when affecting the digital loop filter registers, for example.

Clock multiplexing is provided to select the operation frequency of the BBPDs. These can be operated at frequencies of 40, 80, 160 and 320 MHz. The DLF and ΣΔM are clocked

at 320 MHz and 640 MHz, respectively. Clock gating functionality allows the operation of these components at lower frequencies depending on the chosen reference frequency. An additional output clock distribution network provides three independent outputs clocks, providing either 40 MHz, 80 MHz, 160 MHz, 320 MHz, 640 MHz or 1280 MHz regardless of the chosen reference clock frequency.

4.4. Digital Loop

All digital loop components (FBDIV, BBPD, DLF and ΣΔM) are implemented using static CMOS logic. With the exception of the divide-by-two prescaler described above, these components are synthesized from RTL code using foundry-provided digital standard cell libraries utilizing ordinary active devices instead of ELTs. This design approach, in addition to improving technology portability, also facilitates the systematic inclusion of SEE hardening: TMR was inserted at the RTL design stage using the TMRG tool [28]. TMRG offers the automatic insertion of TMR protection to Verilog modules based on a small number of user constraints, which increases design automation and eliminates common sources of mistakes during redundancy insertion. Following synthesis, an automatic place and route methodology was applied for the majority of the loop components. Manual placement and routing was limited to the feedback divider and phase detectors, where it is required to preserve signal integrity. To avoid the corruption of memory elements protected by TMR by a multi-bit SEU, a minimum spacing of 15 µm between registers containing replicated information was enforced during placement.

Control over the loop transfer function is given by programmable loop filter coefficients in the proportional and integral paths. The coefficients K_P and K_I can be configured to powers of two between 2^{-10} to 2^5 times the tracking unit cell size. To prevent a corruption of the DLF and ΣΔM integrator registers by the accumulation of SEUs, majority voting is implemented in all circuit feedback paths.

The loop filter output controls the DCO tracking bank using two separate paths: The integer component of the loop filter output word directly drives thermometric unit cells, while its fractional component is generated by three thermometric bits driven by the ΣΔM. To maximize the tolerance of the digital components to TID, conservative setup and hold timings were utilized during implementation. Based on the reported degradation of digital circuits in the chosen technology [29], setup margins of at least 20% of the clock period were used. This allows a sufficient margin for the logic to slow down due to TID damage. Pessimistic hold margins exceeding the foundry recommendations by a factor of at least two have been used to allow for unequal delay degradation of different clocks with inter-clock timing arcs. Since the filter characteristics are defined by digital words rather than analog voltages or currents, the loop dynamics will not change under TID damage until the circuit fails due to violations of setup/hold constraints.

5. Measurements

Three samples were characterized across a supply voltage range of ±10% at room temperature. A Rohde & Schwarz FSWP8 phase noise analyzer was used for phase noise and integrated jitter measurements, while frequency measurements were performed using a Keysight 53220A frequency counter. CDR jitter tolerance performance was evaluated using an Agilent N4903B bit error rate tester.

5.1. DCO Characterization

Tuning range, linearity and step size of the three DCO tuning banks were characterized together with static power consumption and open loop phase noise.

The coarse tuning provided by the PVT bank was confirmed to be well-centered around the nominal oscillation frequency of 2.56 GHz and provide the expected 20% range. A frequency step size of ∼6.5 MHz is available around the center frequency. The open loop phase noise of the DCO was measured at the target center frequency, as shown in Figure 6. The phase noise at offset frequencies above 10 MHz is dominated by the clock

distribution network feeding the clock test outputs, which was not optimized for low jitter. The oscillator including its divide-by-two prescaler consumes 7.4 mW while providing a phase noise of −123 dBc/Hz (referred to 2.56 GHz) at a carrier offset frequency of 1 MHz. When accounting for the power dissipation of the prescaler (1.8 mW), this results in an oscillator Figure of Merit (FOM) ($\mathrm{FOM_{DCO}} = -\mathcal{L}(1\,\mathrm{MHz}) + 20\log_{10}\frac{f_{\mathrm{DCO}}}{1\,\mathrm{MHz}} - 10\log_{10}\frac{P_{\mathrm{DCO}}}{1\,\mathrm{mW}}$) of 183.7 dB.

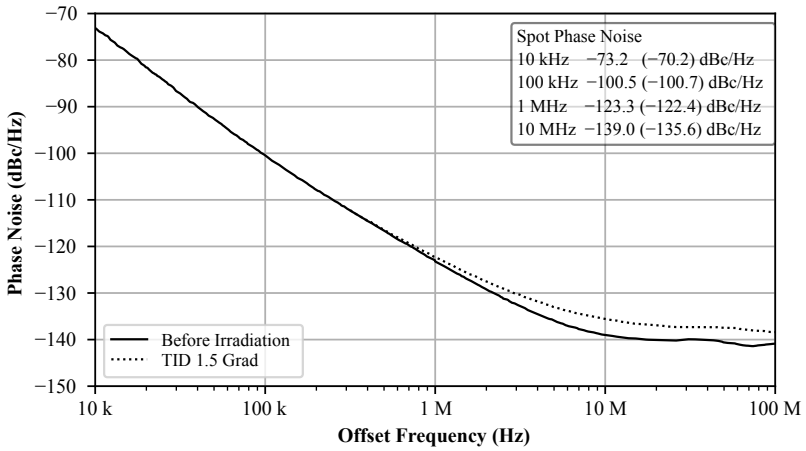

Figure 6. Open loop LC DCO phase noise measurement. Pre- and post-irradiation measurements are shown in solid and dashed lines, respectively. Values in parentheses indicate post-irradiation performance. Noise floor above 10 MHz is limited by clock distribution network.

To validate the custom tracking cell design, the linearity of the tracking bank was further characterized. The very small capacitance of the individual cells demands particular attention during measurements due to the drift of the free-running oscillator. For each tracking bank cell, two measurements were performed, comparing the oscillator frequency at two settings: One of the measurements is performed with all unit cells disabled, while during the second measurement, a fixed number of them are enabled. The obtained frequency difference between these short measurements is stable across long-term drifts of the oscillator, and therefore, multiple measurements can be averaged to reduce the measurement uncertainty. The characterization results can be seen in Figure 7. The thermometric bank offers exceptional differential and integral nonlinearity of better than worst case 0.04 LSB across the full range and a mean frequency step size of 12.7 ppm or 32.5 kHz per cell. This is equivalent to a capacitance difference of 61 aF per cell, which is well in agreement with the electromagnetic simulations.

5.2. PLL and CDR Performance

Closed-loop operation of the ADPLL circuit was tested at all foreseen reference frequencies in PLL and CDR modes of operation across the 1.2 V ± 10% supply voltage range. Typical closed-loop phase noise performance during PLL operation with a 320 MHz reference clock is shown in Figure 8. Integrated random jitter was measured to be 520 fs rms in a 100 Hz to 100 MHz integration band. Jitter tolerance of the CDR circuit operating on 320 Mbit s^{-1} input data is shown in Figure 9. The SONET OC-12 jitter tolerance specification, targeting similar data rates, is included for reference. During operation, the ADPLL circuit dissipates 11 mW of power at the nominal 1.2 V supply voltage. The digital loop components (phase detector, loop filter, ΣΔ modulator and feedback dividers) account for about 50% of the circuit power consumption. This measurement highlights that even with extensive TMR-based hardening against the SEE in place, the DCO still dominates the circuit power consumption in this design. While this property strongly depends on the oscillator design and phase noise requirements of the circuit, it seems fair to assume it will continue to hold in the future for radiation-tolerant designs targeting high-performance applications, especially when the increase of power efficiency for digital circuits in smaller CMOS nodes is taken into account.

A worst case reference spur of −50 dBc was measured at 80 MHz offset from a 640 MHz output clock. This spur was found to originate from power supply coupling between the core logic and the clock distribution network. Switching activity in the digital loop components modulates the clock distribution network supply, which stimulates periodic variations of its propagation delay, creating deterministic jitter. These spurs can be reduced by improving power supply rejection of these buffers or by better supply isolation.

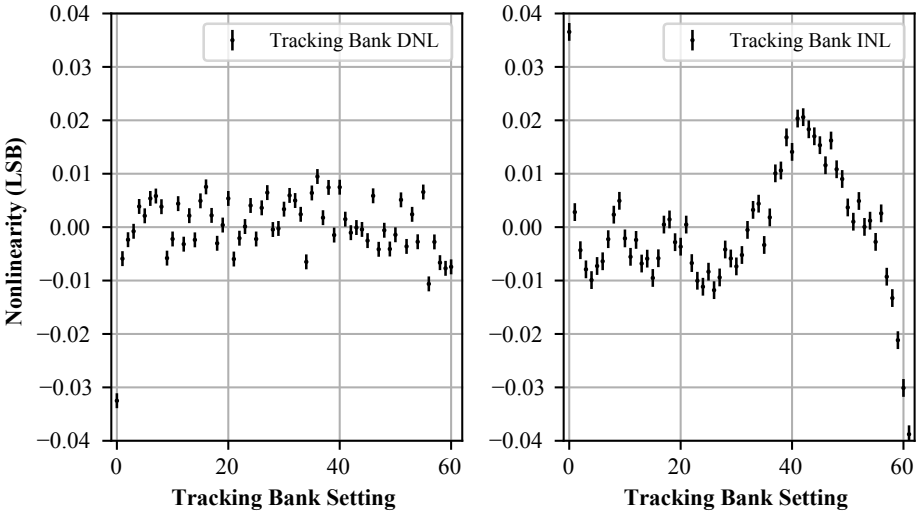

Figure 7. DCO tracking bank linearity measurements, including 95% confidence intervals. The absence of a dummy cell adjacent to cell 0 produces a small edge effect.

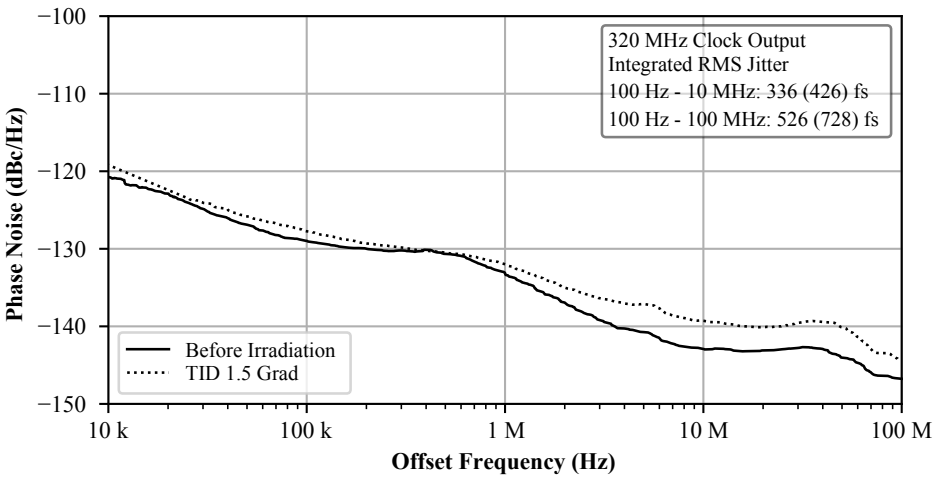

Figure 8. Closed-loop phase noise measurement of an All-Digital PLL circuit. Pre- and post-irradiation measurements are shown in solid and dashed lines, respectively. Values in parentheses indicate post-irradiation performance.

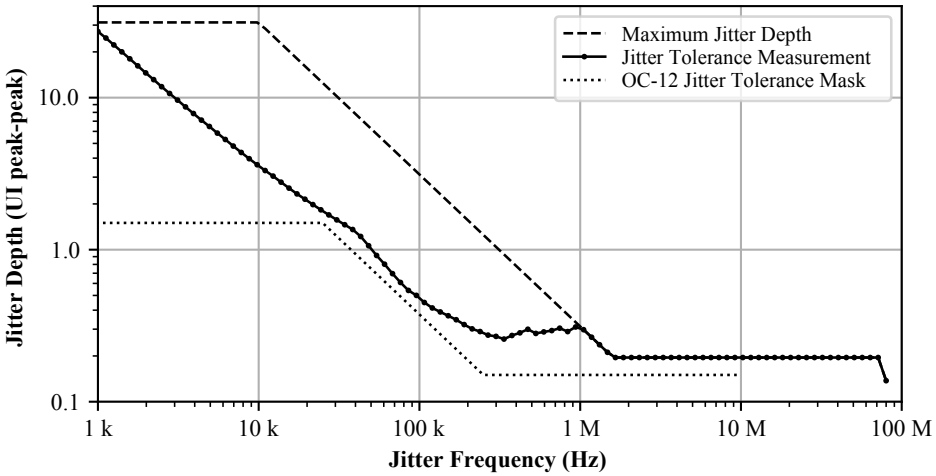

Figure 9. Closed-loop CDR jitter tolerance measurement obtained for a 320 Mbit s^{-1} input data rate. Jitter amplitude limits of the N4903B test setup are indicated with a dashed line.

5.3. Radiation Testing

For characterization of the circuit SEE sensitivity, irradiation with Heavy Ions was performed at the CRC Heavy Ion Facility in Louvain-la-Neuve, Belgium. Ions with Linear Energy Transfer (LET) between 3.3 MeV cm^2 mg^{-1} to 62.5 MeV cm^2 mg^{-1} were used for the measurement of the circuit cross-section. One of the PLL circuit clock outputs was instrumented with a transient phase measurement system, offering a resolution of 4 ps, as described in [30].

The experimentally determined SEE cross-section to heavy ion irradiation for two different phase excursion thresholds is shown in Figure 10. These measurements can be summarized as follows: A large cross-section but low magnitude sensitivity can be attributed to the spiral inductor. Temporary, positive frequency errors of the oscillator are stimulated by the irradiation of this large area [30]. This effect, while responsible for a saturation cross-section on the order of 1×10^{-3} cm^2 in this circuit, will not be discussed further here, as it exists in LC oscillators using planar inductors regardless of their loop architecture and also only results in small phase errors that scale with LET. As the underlying cause is a frequency error of the oscillator, the accumulated loop phase errors can be reduced by increasing the loop bandwidth. The responses of the circuit to this effect have been confined to phase excursions below 250 ps. This sensitivity has been previously discussed in [30].

The second class of SEE responses observed dominates the circuit cross-section for a 300 ps phase error threshold. An example of the observed transients for this class of effects is shown in Figure 11. The effect is characterized by a reduction in the DCO frequency for at least 20 µs. The origin of this sensitivity was identified in the bottom-pinning biasing scheme used for the PVT and acquisition banks (see Figure 4). While the turn-on time of switches M_{SW} and M_{PD} is in the order of one DCO oscillation period, establishing the bottom-pinning bias condition via M_{PIN} was found to require a long settling time, in line with the observed SEE response characteristics. For cells that are disabled during the irradiation, SETs affecting the enable input can temporarily turn on M_{SW} and M_{PD}, which disturbs the established bias condition by pulling V_A and V_B to the ground. While the biasing condition is re-established following this event, the DCO frequency remains slightly reduced, which results in an accumulation of phase errors in the loop. For the PVT cells, a stimulated frequency error of more than −50 ppm was measured during this settling time, and the sensitivity could be fully reproduced using SPICE simulations. A small number of these events at the highest experimental LET resulted in phase excursions up to 5 ns; however, no cycle slips of the PLL have been observed when operating with a 40 MHz reference clock frequency. Such high LET events are very unlikely to occur in

high-energy physics experiments [31]. Nonetheless, this class of SEE can be mitigated using a different capacitor switch implementation, such as the one proposed in [32]. The large phase response to such a small frequency error is a result of its amplification by the BBPD-ADPLL architecture, which is inherently unable to provide a response proportional to the phase error which the long transient DCO frequency error causes. This might make PLL architectures with linear digital phase detectors or automatic loop filter gain adjustments when slewing is detected an attractive extension of this work in the future. No SEE responses could be identified that originated in the digital loop components (DLF, ΣΔM, FBDIV), highlighting the merits and effectiveness of the systematic SEE hardening methodology applied. To confirm this conclusion, the same digital PLL core was also tested with a radiation-tolerant ring DCO, and during its irradiation, no SEE responses exceeding 100 ps could be found.

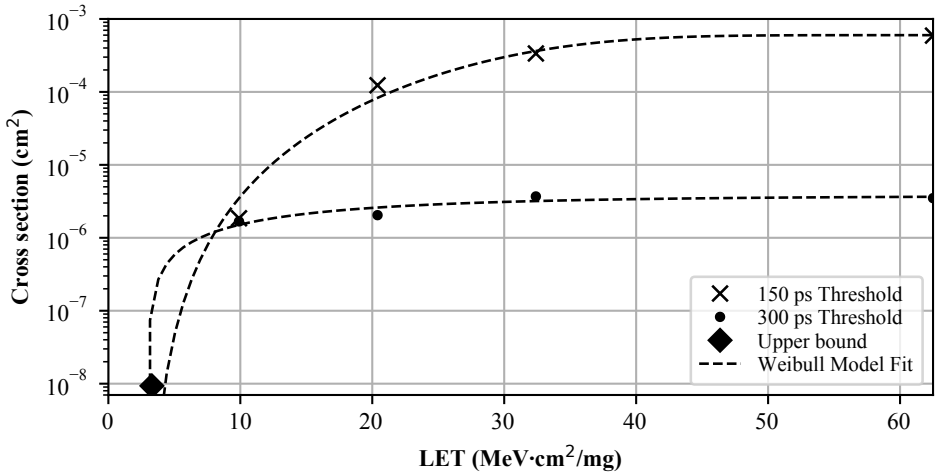

Figure 10. Experimental heavy ion cross-section for different phase excursion thresholds.

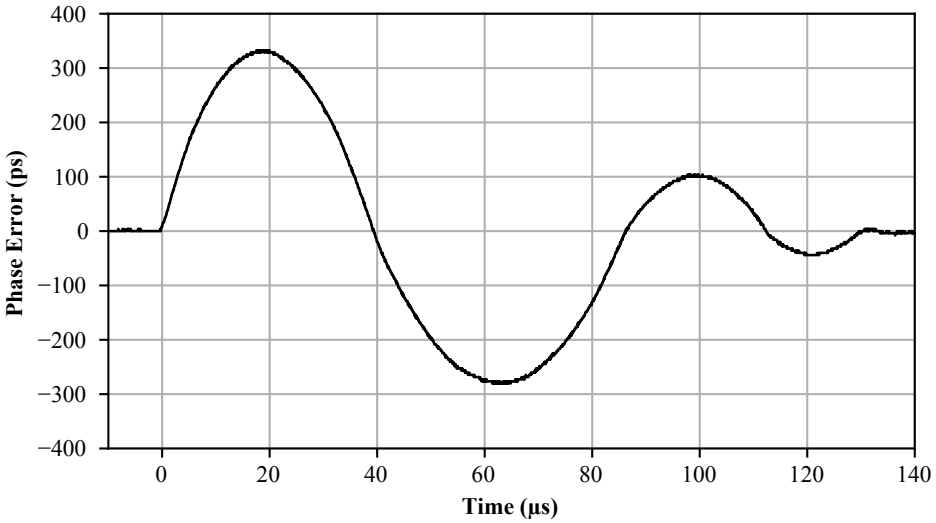

Figure 11. Example SEE phase transient stimulated by high LET (62.5 MeV cm^2 mg^{-1}) ions. The parabolic phase response characteristic for Bang-Bang PLLs is observed. The loop transitions back to the random noise regime after 130 µs.

For the evaluation of its TID tolerance, the circuit was irradiated at the CERN X-ray irradiation facility at a temperature of −10 °C. This temperature is in the range of typical temperatures adopted for future detectors in the harsh radiation environments of the HL-LHC and is therefore expected to give a representative estimate of TID tolerance. A dose rate of 8.9 Mrad/h was used to accumulate a dose of 1.5 Grad over 170 h. The circuit was

kept under bias permanently while repeatedly undergoing a characterization measurement routine.

During the irradiation, a consistent increase in the DCO free-running frequency was observed across all supply voltage and tuning control word settings. The evolution of the oscillation frequency at three different frequency settings is shown in Figure 12. The worst observed frequency shift remained within 0.8%, which is small compared to the total tuning range available (20%). This shift is a result of a change in common mode voltage and oscillation amplitude caused by the radiation-induced reduction in transconductance in the oscillator active devices [16]. Comparing this DCO design to the VCO design adopted in [9], we can find that the radiation-induced frequency shift is significantly reduced. As outlined in Section 4, the MOS varactors used in VCO designs tend to show a strong amplitude dependence, while the majority of capacitance in this DCO design is contributed to by MOM capacitances. The dominant nonlinear capacitance loading the tank in this design is the junction capacitance of the capacitor switches, which explains the significantly reduced sensitivity. This finding highlights the advantage of a varactorless DCO implementation over VCOs in terms of TID tolerance.

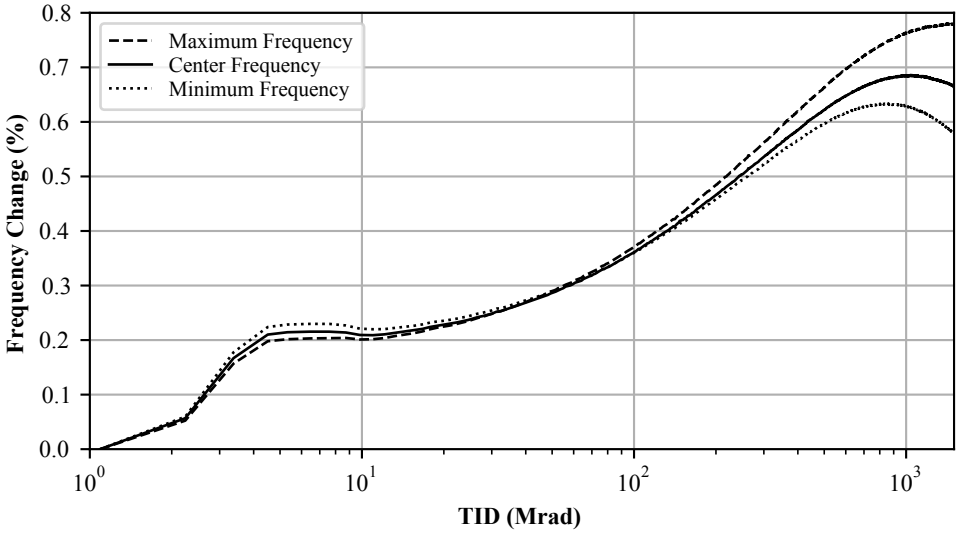

Figure 12. Evolution of DCO frequency under X-ray irradiation. A consistent frequency increase relative to the pre-irradiation value is seen for different frequency settings of the oscillator.

The circuit continued to operate normally up to 1.4 Grad. At this dose, a distinct drop of current consumption in the power domain supplying the DCO and divide-by-two prescaler was observed for the highest DCO frequency setting at the lower end of the specified supply voltage range. As the oscillation of the DCO did not cease and the PLL was still operational at this dose, this behavior can be explained by a failure of one of the TMR branches of the divide-by-two prescaler. Figure 6 shows the open loop phase noise performance of the oscillator at nominal operating conditions after the 1.5 Grad irradiation. Degradation is most pronounced at offset frequencies above 1 MHz and is dominated by the clock distribution network noise floor increase above 10 MHz. During the irradiation period, the circuit power dissipation was found to gradually reduce by about 15%.

Repeated measurements of the tracking bank tuning step size performed during the irradiation did not show a noticeable change. As the loop gain is otherwise determined primarily by the DLF, whose coefficients are insensitive to TID, the dynamic behavior of the PLL remained largely unaffected by the irradiation. This can be concluded from Figure 8, which compares the pre- and post-irradiation closed-loop noise performance. An increase in phase noise consistent with the previously discussed oscillator degradation can be observed. No locking failures have been observed during the test procedure, the PVT and acquisition banks were able to compensate for the oscillator frequency shift according to expectations and the output clock delay with respect to the reference clock

remained repeatable across the irradiation. No failures of the DLF, ΣΔM and divide-by-32 FBDIV were observed during the irradiation procedure, implying that the chosen synthesis strategy was adequate to achieve high radiation tolerance.

5.4. Summary

A comparison of this design to other radiation-tolerant PLL and CDR circuits reported in the literature is shown in Table 1. The proposed design outperforms the compared designs both in PLL FOM as well as in demonstrated TID tolerance. The remaining SEE sensitivity of the proposed circuit has been clearly identified, and a mitigation strategy has been proposed, which will allow eliminating any circuit cross-section for phase errors exceeding 250 ps, below which the inductor radiation effect will remain as the dominant contributor. In terms of area, the proposed circuit approaches the area of ring oscillator PLLs manufactured in the same technology [33], mainly because of the large area occupied by the loop filter capacitor in analog PLLs, which is realized as a digital integrator in this design.

Table 1. Comparison of radiation tolerant PLL/CDR designs.

Reference	This Work	[9]	[33]	[34]
Type	All-Digital PLL/CDR	Analog CDR	Analog CDR	Analog PLL
Oscillator	LC DCO	LC VCO	Ring VCO	LC VCO
Technology	65 nm	65 nm	65 nm	65 nm
Jitter (ps rms)	0.5	0.35	6.7	3.5
Power (mW)	11	34	7	18
Area (mm^2)	0.28	0.33	0.25	0.124
TID Tolerance (Mrad)	1500	350	600	250
FOM_{PLL} (dB)	−235	−234	−215	−217

6. Conclusions

A radiation-tolerant All-Digital PLL and CDR circuit suitable for applications in high-energy physics was designed, implemented and tested. Different advantages of a varactorless DCO architecture combined with a digital loop implementation to replace sensitive analog charge pumps have been demonstrated in the context of radiation hardening. The successful demonstration of an implementation approach heavily utilizing automated TMR insertion, together with automated place and route methodologies, shows that design reuse and technology portability opportunities are retained even for circuits requiring radiation tolerance.

A crucial observation is that the remaining single-event effect sensitivity has been identified in the DCO, which also remains the major mixed-signal component of the design. This underlines the continued difficulty of accurately predicting SEE sensitivities of such circuits and fully mitigating them during the design phase. This is in contrast to the digital design components, which were all successfully protected against SEU and SET by applying systematic and reliable design hardening techniques. A mitigation for the identified sensitivity has been proposed, which will allow pushing the envelope of radiation-tolerant All-Digital PLL circuits even further in future work.

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