Broadband Concepts for High Efficiency Microwave Power Amplifiers Using Gallium Nitride Technology

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To my parents

who have given me the opportunity of an education at the best institutions and support throughout my life.

To my lovely wife and children

who have always stood by me and dealt with all of my absence from many family occasions with a smile.

Abstract

Power amplifier units are the most important components in mobile radio base stations (RBSs). Their performance affects the overall performance of the base station in terms of output power and efficiency. A special high interest is the combination of high efficiency and wide bandwidth. This dissertation is dedicated to this central problem.

First, the design and characterization of a single-ended power amplifier (PA) with center frequency of 2.0 GHz is presented. The design methodology was based on class-E approach combined with a systematic design of broadband matching networks. Therefore, the output matching network was modified. The fabricated PA has achieved 70 % - 76 % power-added efficiency (PAE) with output power ranges between 43.5 to 45 dBm over 1.7 - 2.3 GHz.

In a second design, the bandwidth was expanded to cover more than an octave while maintaining similar performance; the input-/ output matching networks were redesigned for this purpose. This ultimately has resulted in a highly efficient ultra-wideband PA with a minimum output power of 43.0 dBm and PAE ranging between 60 % - 72 % over 1.1 - 2.7 GHz.

These results encourage an update of the topology and design methodology of the matching networks to further extend the bandwidth of operation. For this aim, a novel planar broadside coupled transformer is developed and used for the first time as a main part of the matching network in the designed PA. The fabricated PA, with a bandwidth of operation ranging between 0.5 - 2.7 GHz, has achieved a minimum output power of 43.0 dBm with PAE ranging between 50 % - 65 %.

For RBSs with output power beyond 100 W, larger components should be used. This results in lower input-/ output impedances of the used transistors. Designing an ultra wideband PA with high efficiency is therefore an immense challenge, due to the complexity of the matching networks and the resulting high losses. This challenge was pursued with the aim of realizing a 100 W, highly efficient PA for the frequency range from 0.6 GHz to 2.7 GHz. The fabricated PA has achieved typical output power of 100 W with 45 - 65 % PAE across the desired bandwidth.

Basically, it is desirable that the high efficiency of PAs at full load (saturation) is maintained as high as possible when decreasing the input power level (part load or back-off power ange). With this objective, the passive load modulation technique has been investigated to adapt the transistor load impedance depending on the output power level, so that the efficiency remains as high as possible even at back-off power range. First two prototype designs without tunable components were proposed and used as reference. In these two designs, only the output matching networks were different. The first one was optimized for full load and the second one was optimized for 6 dB back-off output power level. The full load PA delivered saturation output power of approximately 43.0 dBm with average maximum efficiency of 65 % and 6 dB OBO average efficiency of 36 % across 1.8 - 2.2 GHz. The 6 dB back-off optimized PA delivered average maximum efficiency of 50 % and 6 dB OBO average efficiecny of 52 % over the desired bandwidth. Accordingly, an improvement of the average efficiency at 6 dB back-off can reach up to 16 % appears to be possible.

Based on these results and conclusion, a third prototype has been proposed using an electronic tunable output matching network. A barium strontium titanate (BST) based varactors were used as variable capacitors. However, and due to the varactor losses, the performance of the previously described designs could not be achieved.

Zusammenfassung

Leistungsverstärker gehören zu den wichtigsten Komponenten in Mobilfunk-Basisstationen. Sie dominieren die elektrischen Eigenschaften der Basisstation in Bezug auf Ausgangsleistung und Wirkungsgrad. Ein besonders hohes Interesse besteht in der Verknüpfung von hohem Wirkungsgrad mit großer Bandbreite. Diese Dissertation widmet sich dieser zentralen Problemstellung.

Im ersten Beispiel werden Entwurf, Aufbau und Charakterisierung eines Leistungsverstärkers mit einer Mittenfrequenz von ca. 2,0 GHz vorgestellt. Die Entwurfsmethode geht von einem Klasse-E Verstärker aus, mit der Zielstellung, eine höhere Bandbreite zu realisieren. Dazu wurde das Ausgangs-Anpassungsnetzwerk gezielt modifiziert. An dem aufgebauten Verstärker wurden über den Frequenzbereich 1,7- bis 2,3 GHz Ausgangsleistungen zwischen 43,5- und 45 dBm gemessen, mit Wirkungsgraden von 70- bis 76 %.

In einem erweiterten Entwurf sollte die Bandbreite auf mehr als eine Oktave erhöht werden - nach Möglichkeit bei sonst unveränderter Performanz. Dafür wurden Ein- uns Ausgangs-Anpassungs-Netzwerke neu entworfen. An dem Verstärker wurde dann im Frequenzbereich 1,1- 2,7 GHz eine Ausgangsleistung von mehr als 43 dBm gemessen, mit einem Wirkungsgrad zwischen 60- und 72 %. Die vielversprechenden Ergebnisse dieses Entwurfs waren die Hauptmotivation für den Versuch, die Verstärkerbandbreite weiter zu erhöhen. Zu diesem Zweck wurde für das Ausgangs- Anpassungsnetzwerk ein neuartiger, planarer Leitungstransformator entwickelt. Der aufgebaute Verstärker erreichte damit im Frequenzbereich 0,5- bis 2,7 GHz eine Ausgangsleistung von mindestens 43 dBm mit Wirkungsgraden zwischen 50- und 65 %.

Für Basisstationen mit Ausgangsleistungen jenseits von 100 W müssen für die Endstufen größere Bauelemente verwendet werden, was niederohmigere Ein-/ Ausgangsimpedanzen der verwendeten Transistoren zur Folge hat. Die Erzielung hoher Bandbreiten bei gleichzeitig hohem Wirkungsgrad stellt deshalb eine immense Herausforderung dar, da auch die Verluste und Komplexität der Anpassungs-Netzwerke ansteigen. Dieser Fragestellung wurde mit dem Ziel nachgegangen, für den Frequenzbereich 0,6- bis 2,7 GHz einen Verstärker mit mindestens 100 W Ausgangsleistung und möglichst hohem Wirkungsgrad zu realisieren. Die Messungen am aufgebauten Prototyp bestätigten für den genannten Frequenzbereich typische Ausgangsleistungen von 100 W mit Wirkungsgraden zwischen etwa 45- und 65 %.

Grundsätzlich ist es wünschenswert, dass sich der im Allgemeinen hohe Wirkungsgrad von Verstärkern im Vollastbereich mit abnehmender Eingangsleistung (Teillastbereich oder Back-Off) so wenig wie möglich verringert. Mit dieser Zielstellung wurde die passive Lastmodulationstechnik untersucht, um die Transistor- Lastimpedanzen leistungsabhängig derart nachzuführen, dass der Wirkungsgrad auch im Teillast-Bereich möglichst hoch bleibt. Die ersten beiden Entwürfe wurden als Referenz herangezogen. Hier wurden zwei unterschiedliche, ansonsten aber nicht abstimmbare Ausgangs-Anpassungsnetzwerke eingesetzt, die zum einen für den Vollast- und zum anderen für den Back-Off-Bereich optimiert wurden. Der für Volllast ausgelegte Referenzverstärker lieferte im Frequenzbereich 1,8- bis 2,2 GHz eine Sättigungs-Ausgangsleistung von etwa 43,0 dBm und Volllast-/Teillast- Wirkungsgrade von etwa 65 und 36 %. Der für 6 dB Back-Off optimierte Verstärker lieferte Volllast-/Teillast- Wirkungsgrade

von etwa 50 und 52 %. Die Wirkungsgradverbesserung im Teillastbereich erreichte damit bis zu 16 %.

In einem weiteren Entwurf wurde ein elektronisch abstimmbares Ausgangs-Anpassungs-Netzwerk realisiert, unter Verwendung von Barium-Strontium-Titanat- (BST) basierten Varaktoren als variable Kondensatoren. Hauptsächlich wegen der Varaktorverluste konnte bei diesem Verstärker die Performanz der vorher beschriebenen Entwürfe nicht erreicht werden.

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Mhd. Tareq Arnous

11.05.2018

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Nomenclature

3G	Third generation of cellular wireless standards
4G	Fourth generation of cellular wireless standards
5G	Fifth generation mobile networks or fifth generation wireless systems
η	Efficiency
ε	Dielectric constant
Γ	Reflection coefficient
ACLR	Adjacent channel leakage ratio
ADS	Advanced design system
BJT	Bipolar junction transistor
BST	Barium Strontium Titanate
BW	Bandwidth
CCA	Current conduction angle
CO2	Carbon dioxide
DC	Direct current
DLM	Dynamic load modulation
DPD	Digital predistortion technique
DSM	Dynamic supply modulation
DSP	Dissipated power
DVB-T	Digital video broadcasting-terrestrial
EA	Envelop power amplifier
EDGE	Enhanced data rates for GSM evolution
EER	Envelope elimination and restoration
EM	Electromagnetic

ET	Envelope tracking
FET	Field-effect transistor
FMN	Fixed matching network
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GMSK	Gaussian minimum shift keying
GSM	Global system for mobile communications
HEMT	High electron mobility transistor
HSPA	High speed packet access
HT-PA	Harmonically tuned power amplifier
IDC	Interdigital capacitor
LDMOS	Laterally diffused metal oxide semiconductor
LEs	Lumped elements
LTE	Long-term evolution
LTE-A	LTE Advanced
LTE-A Pro	LTE Advanced Pro
MAG	Maximum available gain
MEMS	Micro-electro-mechanical systems
mm	Millimeter
MSG	Maximum stable gain
MSL	Microstrip lines
OBO	Output back-off
PA	Power amplifier
PAE	Power-added efficiency
PAPR	Peak-to-average power ratio
PDF	Probability density function
PSK	Phase-shift keying
Q	Quality factor

QAM	Quadrature amplitude modulation
RBS	Radio base station
RF	Radio frequency
Si	Silicon
SiC	Silicon Carbide
SMA	SubMiniature version A
SMPA	Switch-mode power amplifier
TLs	Transmission lines
TMN	Tunable matching network
TWA	Traveling wave amplifier
UHF	Ultra high frequency
UMTS	Universal mobile telecommunications system
V_{CON}	Control voltage
V_{knee}	Knee voltage
VSWR	Voltage standing wave ratio
W	Watt
WCDMA	Wideband code division multiple access
WiFi	Wireless fidelity
WiMAX	Worldwide interoperability for microwave access

1 Introduction

1.1 Motivation

The notion of the world becoming a global village was quite an unbelievable dream. Yet the wireless communication revolution has made this dream a reality. Today, the whole world is working and investing both money and effort into this domain. The notion of telecommunication has changed. It is no longer only voice or video call but also includes the exchange of data at high speed, sending and receiving documents, transferring money etc. A lot has already been achieved, but the most recent challenge is how to make the communication and data transfer more efficient and reliable. The requirements of this kind of communication are not restricted to humanity, as they are very important for all artificial intelligence systems. It is estimated that in 2021, the global mobile data traffic will increase up to 12 billion connections, as presented in [1], see the Fig. 1.1.

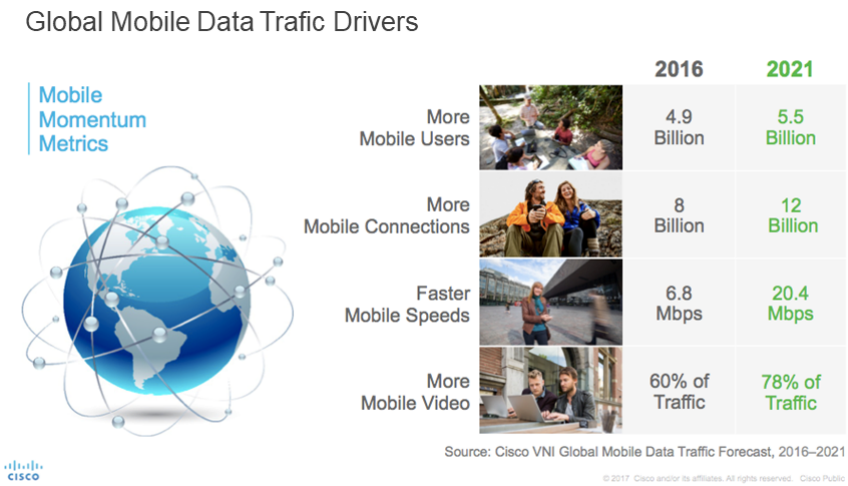


Figure 1.1: Comparison between the mobile momentum metrics in 2016 and 2021 [1].

To handle growing mobile data traffic requirements, mobile network operators have:

1. Expanded the bandwidth of operation of the radio base stations (RBSs) to increase the capacity.

2. Introduced a number of mobile radio standards such as GSM, UMTS, WiFi, 4G LTE, 5G, WiMax, etc.

3. Reduced the cell size in the network and significantly increased RBSs to meet demand.

Nevertheless, this results in increased energy consumption and causes additional CO2 emissions [3], as shown in Fig. 1.2. Currently, the annual worldwide power consumption of RBSs is 120 TWh, 50 % to 80 % of which is consumed by the power amplifier (PA). This amount can be compared to the 12 TWh power generated from the Grafenrheinfeld nuclear power plant each year. The total efficiency of the RBS is poor and defined as the ratio of the total RF-transmitted output power to the total consumed power in the RBS. Moreover, in wireless infrastructures, the RBS is the main contributor to the energy consumption and the highest contributors of CO2 emissions. Reducing the energy consumption of the RBS can reduce the CO2 emission and maximize its efficiency, as shown in Fig. 1.2. At the core of the RBS is the power amplifier one of the most critical blocks due to the fact that its performance strongly influences system features in terms of bandwidth, output power, efficiency, and operating temperature. Increasing the bandwidth of operation and the efficiency of the power amplifier therefore reduces the total energy consumption and CO2 emission. It also reduces the total cost of the RBS by reducing the cost and volume of the cooling system. This is an important and current topic of research in this domain.

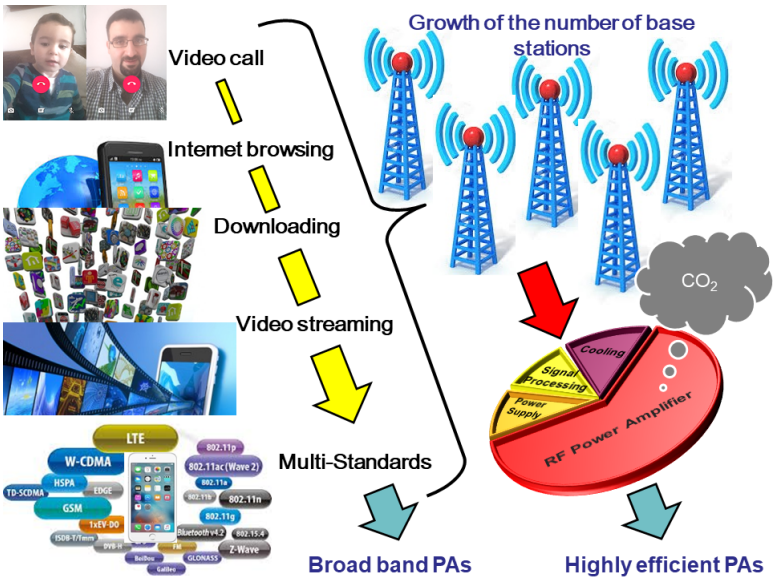


Figure 1.2: Main motivation of this dissertation for RBS.

Moreover, the need for higher data rates has brought about the use of higher frequencies with higher bandwidth and modulation complexities. In this manner, many new applications (3G, 4G, WiMAX, and 5G), especially in the frequency range between 1.8 GHz and 3 GHz have flourished in recent years, as shown in Fig. 1.3.

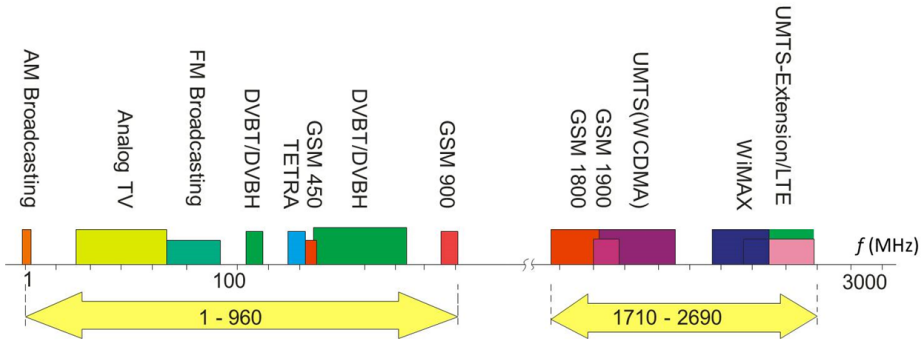
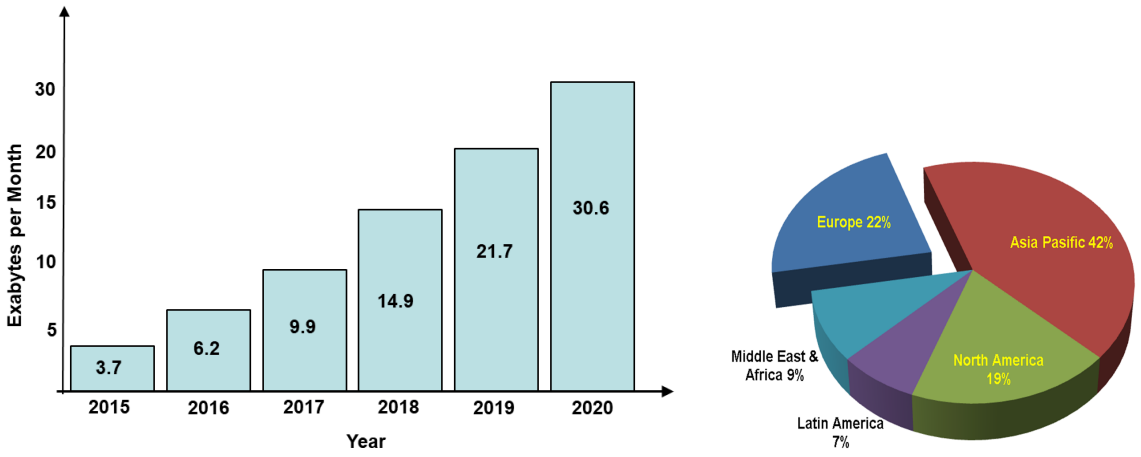


Figure 1.3: Diversity of modern wireless applications.

The exchange data shown by different sources show tremendous data communication increases in the upcoming years, as shown in Fig. 1.4(a). Based on these reports [1], mobile data communication usage will increase by 7 times between 2015 and 2020 Fig. 1.4(a). Furthermore, due to its 22 % share, as shown in Fig. 1.4(b), Europe would be the second largest user.



(a) (b)

Figure 1.4: (a) Global mobile data traffic forecast, 2015 to 2020; (b) worldwide data communication usage statistic [1].

The design of highly efficient, ultra-wideband power amplifiers is the result of a trade-off between several conflicting requirements such as efficiency versus linearity and efficiency versus bandwidth. The main focus scope of this dissertation is to figure out a scientific approach to overcome the previously presented challenging items to meet the demands of modern wireless communications. This dissertation has therefore studied those challenges and proposes a new approach to overcome these trade-offs. It mainly focuses on two topics:

- Presenting various approaches to design ultra-wideband and efficient power amplifiers.
- Presenting two approaches to design wideband and efficient power amplifiers at various output-back-off (OBO) power levels.

1.2 State-of-the-art results

This Section presents the performance of the demonstrated PAs and compares their performance to recently reported amplifiers. The author has mainly discussed two topics in this dissertation. Therefore, two state-of-the-art tables are illustrated.

1.2.1 State-of-the-art table of highly efficient wideband PAs

Many research groups are working on designing highly efficient, wideband power amplifiers. Table 1.1 presents the state-of-the-art results of the recently published papers in the highly efficient wideband power amplifier domain which are close to [Paper A, Paper B, Paper C, Paper D]. The comparison can be classified into four categories based on a bandwidth of operation and output power levels.

Table 1.1: State-of-the-art efficient wideband power amplifiers using GaN-HEMT.

Reference	**Freq [GHz]**	**P_{Out}[W]**	**Gain [dB]**	**Drain efficiency [%]**
2006 [4]	1.8 - 2.3	5 - 7	9 - 10	57 - 62
2009 [5]	2.0 - 2.5	7 - 12	10 - 13	74 - 77
2012 [6]	1.6 - 2.2	10 - 13	10 - 12	55 - 68
2012 [7]	1.45 - 2.45	11 - 16.8	9 - 12	70 - 80
2013 [8]	1.35 - 2.0	45	8.2 - 16.9	65 - 76
[Paper A]	**1.7 - 2.3**	**22 - 32**	**11.5 - 13**	**73 - 80**
2009 [9]	1.4 - 2.6	9 - 11	7 - 13	60 - 70
2010 [10]	1.55 - 2.75	10	10 - 12	55 - 56
2011 [11]	0.9 - 2.2	10 - 20	10 - 13	63 - 89
2012 [12]	1.3 - 3.3	10	11 - 12	58 - 83
[Paper B]	**1.1 - 2.7**	**20 - 31**	**9 - 12**	**65 - 78**
2009 [13]	0.35 - 8	7 - 10	8 - 10	20 - 33
2011 [14]	0.5 - 1.1	10.5	9.5 - 12	65 - 80
2014 [15]	1.5 - 5.5	10 - 22	5 - 9	50 - 57
2015 [16]	0.9 - 2.6	12 - 30	7.3 - 12.7	60 - 64
[Paper C]	**0.5 - 2.7**	**20 - 35**	**8 - 10.4**	**56 - 70**
2011[17]	1.55 - 2.25	100	12	65
2011[18]	1.0 - 2.0	90	11	58 - 72
2012 [19]	1.1 - 2.0	79.5 - 158	10 - 12	51 - 62
[Paper D]	**0.6 - 2.6**	**80 - 115**	**8.5 - 11.5**	**48 - 65**

The amplifier in [5] has higher efficiency than the PA in [Paper A]. Despite this, the amplifier in [Paper A] has a larger bandwidth and higher output power. The PA in [8] has a higher output power level with a comparable drain efficiency to the amplifier in [Paper A] but with a lower frequency range and high deviation in gain level over the operating frequency band. Moreover, the amplifier in [Paper B] has the best efficiency and the highest output power compared to the recently published PAs, which have a close bandwidth of

operation. In the third category of comparison, the PA in [Paper C] has the best efficiency and the highest output power. The last category, the amplifier in [Paper D] has slightly lower efficiency compared to the rest related work in this category, but the bandwidth of the PA in [Paper D] is at least two times bigger than the others.

1.2.2 State-of-the-art table of wideband dynamic passive load PAs

Table 1.2 also shows the state-of-the-art results of the recent wideband dynamic passive load power amplifier designs. The table concludes that this work is comparable to recently reported designs in this domain. Furthermore, most of the work which has been presented is for narrowband applications, whereas the work in this dissertation is concerned with wideband application using silicon hyperabrupt technology based varactors and BST-based varactors for the first time.

When it comes to [20] in particular, it has a higher bandwidth with less peak output power compared to [Paper E], due to the use of a small sized transistor. Moreover, load modulation and supply modulation technique have been used in [20] to achieve these results. By comparison, [Paper E] only presents a passive load modulation technique with two different tunable technologies.

Table 1.2: State-of-the-art efficient PAPR wideband power amplifiers.

Reference	**Freq[GHz]**	$\mathbf{P}_{Out-Max}$**[dBm]**	**Gain[dB]**	η_{Max} [%]	$\eta_{6dB_{OBO}}$ [%]
2012 [20]	1.0 - 1.9	39.5 - 40.5	8 - 12	65 - 75	47 - 62
2015 [21]	1.8 - 2.2	40.1 - 41.5	10 - 13.2	50 - 55	42.5
2017 [22]	1.71 - 1.785	45	-	60	35
2017 [23]	1.7 - 2.3	36 - 36.6	11 - 15	44 - 54	38 - 43
[Paper E]	**1.8 - 2.2**	**40 - 44.5**	**10 - 11**	**61 - 67**	**42 - 60**
[Paper E]	**1.8 - 2.2**	**40 - 44**	**6 - 9**	**58 - 70**	**42 - 62**

1.3 Dissertation contributions

This work has focused on developing of theory and technology for design and realization of highly efficient wideband power amplifiers. Improving the efficiency of the power amplifier results in reducing the operational cost, due to a reduction in DC supply and cooling requirements. It also results in decreasing the CO2 emission in RBS. This solution provides a simpler RBS installation, and less interference between RBSs, which finally results in optimizing the performance and density of the mobile network. The aim of [Paper A] was to design a broadband power amplifier with maximum available efficiency and output power based on matching the harmonic impedances. The bandwidth was limited in order to ensure a high efficiency performance. Comparatively, [Paper B] proposed a new approach for designing ultra-wideband power amplifier to solve the in-bands problem by adapting the fundamental optimum load impedances of low band impedances in order to match the in-bands 2^{nd} and 3^{rd} harmonics impedances. The contribution in [Paper C] has been used alongside this ap-

proach, a broadside coupled transformer in output matching network, to expand further the bandwidth operation. The contribution of [Paper D] has focused on increasing the output power using a larger transistor device for high power applications. Matching topology of a large transistor is more difficult than a small one due to the low optimum impedance value of the large transistor. Using the broadside coupled transformer alongside the new approach of determining the optimum load impedances, which have been used in [Paper B], has simplified the matching network topology and ensured a high efficiency performance with high output power.

Another important factor in the RBS-amplifier is the efficiency performance at various output-back-off power (OBO) levels, based on using modulated signals in modern wireless communication. Dynamic load modulation (DLM) is an interesting concept for enhancing the efficiency of PAs at back-off output power. The bottleneck of the DLM-PA is the interplay between the two different semiconductor devices transistor and varactor. The second part of this dissertation focuses on improving the efficiency of wideband PAs at various (OBO) power levels. The work in [Paper E] has characterized and compared two different technologies of varactors. The first one used silicon hyperabrupt technology, whereas the second one used BST technology. It highlighted the pros and cons of using each technology. The contribution in [Paper F] used a thin-film BST based varactor for the first time as a main part of the matching network to form a load modulation, based on the delivered output power level by controlling the DC-voltage of the BST based varactor.

In summary, this dissertation addresses, proposes and demonstrates a concept to improve the capacity and energy efficiency in power amplifiers at required lower costs.

1.4 Dissertation outlines

This dissertation is divided into five parts:

The first chapter presenting the introduction of the dissertation. It describes the background of the research and defines the objective of the dissertation. It illustrates the corresponding state-of-the-art table of this dissertation. Two tables are presented because the dissertation considers mainly two topics.

Chapter 2 presents the fundamentals of the power amplifier. The basic operations of transistors and power amplifiers are presented in this chapter. The equivalent circuit of the physical architecture of the transistor is illustrated. The most important parameters of the power amplifier are highlighted and various topologies of matching networks are presented. Moreover, the most common classes of operation of power amplifiers are presented for narrowband and wideband power amplifiers.

Chapter 3 represents the practical Section of this dissertation. This chapter focuses on designing highly efficient broadband power amplifiers under various approaches. Five designs are presented [Paper A, Paper B, Paper C, Paper D] including the design approach and presenting the measurement results of each design.

Chapter 4 presents all approaches of improving the efficiency of power amplifiers at various output back-off power levels such as dynamic supply modulation or dynamic load modulation

technique. This chapter focuses on enhancing the efficiency of broadband power amplifier at back-off output power level [Paper E, Paper F].

Chapter 5 concludes this dissertation with the achievements summary and suggestions.

2 Power Amplifier Fundamentals

The power amplifier is a key element in the transmitter system and the most critical component in RBSs since its performance affects the overall system in terms of output power, efficiency, bandwidth, linearity, and power consumption. This chapter presents all the factors that impact the power amplifier's performance. It starts with the physical architecture of the transistor, then moves on to the transistor equivalent circuit, illustrating the main demands of the matching network, describes the most common approaches in designing a matching network.

2.1 Active device characteristics

The transistor is the core component of designing a power amplifier. Over time, various types of transistors have been developed and used in the design of PAs. They can be divided into two categories. The Field Effect Transistors (FETs) and the Bipolar-Junction Transistors (BJTs) [24]. Silicon technology (Si) is the main semiconductor technology used in transistor fabrication. Due to the strong requirements for improving the RF performance of the transistor, other transistors are manufactured from the III-V compound semiconductors such as GaAs and GaN. Table 2.1 introduces major characteristics of the most used materials for the fabrication of transistors and illustrates why the GaN-HEMT has been used in this dissertation.

- **Dielectric constant:** The physical architecture of a transistor can be modeled with varying capacitances, inductances, resistances and current sources. The capacitance values are basically influenced by the dimensions of the transistor and the dielectric constant (ε) [25]. This capacitor should ideally be zero to simplify the design of the matching network and to match the low real impedance of transistor to high real impedance level, which is not realizable. For this reason, using a semiconductor with low ε reduces the associated capacitance, as shown in Eq. 2.1, and results in increase in the load impedance. GaN semiconductor has a low dielectric constant of ($\varepsilon = 8.90$) compared to other semiconductors in table 2.1. expect the diamond, which is not used for designing commercial transistors.

$$C_j = \varepsilon_0 \cdot \varepsilon_r \frac{A}{W} = A \cdot \sqrt{\frac{\varepsilon_0 \cdot \varepsilon_r \cdot e \cdot N_A \cdot N_D}{2 \cdot V_D \cdot (N_A + N_D)}} \tag{2.1}$$

where:

C_j: Junction capacitance [Farads]

ε_0: Permittivity of dielectric of free space (8.85×10^{-12}) [F/m]

ε_r: Permittivity of the dielectric of isolation
A: Area of plates or p-type and n-type regions $[m^2]$
W: Width of depletion region$[m]$
e: Electron charge ($1.60217646 \times 10^{-19}$) [Coulombs]
N_A: Concentration of acceptor atoms $[m^{-3}]$
N_D: Concentration of donor atoms $[m^{-3}]$
V_D: Diffusion voltage $[V]$

- **Bandgap energy:** is defined as the energy required for transferring an electron from the valence to conduction bands in a semiconductor. It impacts the maximum allowed temperature in the device and its power capabilities. A wider bandgap results in a higher operating temperature [26], thus allowing smaller devices with higher power density to be manufactured. Moreover, the higher value of the bandgap energy results in higher voltage handling capabilities and improvement in efficiency due to smaller scaling dimensions [27]. GaN is called a wide bandgap semiconductor due to its high bandgap of 3.4 eV compared to gallium arsenide (GaAs) 1.4 eV and silicon (Si) 1.1 eV. This wide bandgap offers the potential to design microwave devices with an improved RF output power compared to the traditional devices based on Si or GaAs [28].

- **Breakdown voltage:** impacts the maximum available power density of the transistor, because it refers to the maximum applied electric field without destroying the device, and results in an increase of RF power swing. The high breakdown voltage is worth increasing the doping concentration and reducing the dimensions of the device [29]. Table 2.1 shows, that GaN has the highest breakdown voltage, followed by SiC. This is why these two materials are preferred for high power transistors.

- **Electron mobility:** impacts the operation speed of the transistor, and therefore the power efficiency at a given frequency. Bulk GaN mobility is quite low compared to other semiconductor materials, as shown in Table 2.1, but thanks to the 2DEG which allows higher mobility, GaN-HEMT is a good candidate for PA design.

- **Saturation velocity:** impacts the current density and the operating frequency (f_T) of the transistor; in this regard, GaN enables relatively high current density and operating frequencies.

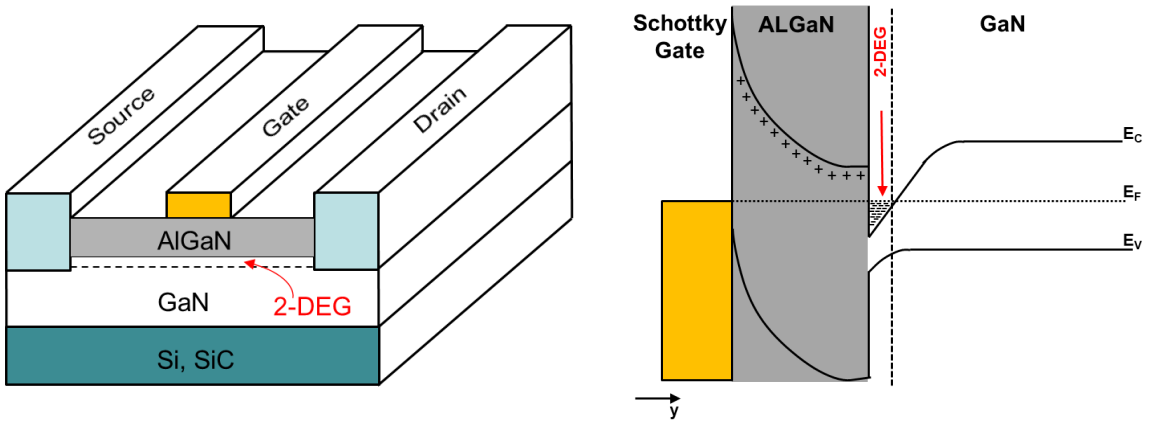
- **Thermal conductivity:** this parameter impacts the performance of the device over time. It evaluates the ability of conducting heat to the external environment. Furthermore, the thermal conductivity of the overall device relies strongly on the adopted substrate. The SiC devices provide higher power densities, up to 10 W/mm, with respect to the typical values 0.3 – 0.5 W/mm of GaAs based MESFETs, due to their wide energy bandgap and the higher thermal conductivity. GaN devices can operate at higher power densities than either GaAs or Si [27]. GaN is therefore the best candidates for high-power RF amplifiers. GaN-on-SiC has a power performance of approximately 5 W/mm, compared to approximately 1 W/mm for GaAs and 0.3 W/mm for Si.

Table 2.1: Semiconductors characteristics.

Property	**Si**	**4H-SiC**	**InP**	**GaAs**	**GaN**	**Diamond**
Dielectric constant	11.7	9.7	14	12.9	8.9	5.7
Bandgap Energy $[eV]$	1.11	3.2	1.34	1.43	3.4	5.45
Breakdown voltage	300	2000	500	400	5000	5000
Electron mobility $[cm^2/V \cdot s]$	1450	500	4000	8500	800	4500
Saturation velocity $[cm/s]$	9×10^6	2×10^7	1.9×10^7	1.3×10^7	2.3×10^6	2.7×10^6
Thermal conductivity $[W/cm \cdot K]$	1.5	4.9	0.68	0.46	1.7	20

2.2 GaN-HEMT technology

Aluminum Gallium Nitride/Gallium Nitride high electron mobility transistor (AlGaN/GaN-HEMT) technology has shown especially promising results with both pulsed and CW power densities in the region of 10 W/mm [30, 31]. The basic physical structure of the GaN-HEMT is presented in Fig. 2.1, where at a high temperature (approximately 1,100°C), GaN is adopted on one of two foreign substrates: silicon (Si) for power electronic applications or silicon carbide (SiC) for RF applications. The GaN-on-Si combination has a much poorer thermal performance and higher RF losses, but it is much cheaper. However, the GaN-on-SiC approach results in high power density, superior thermal conductivity and low RF losses, due to its inherent high electron mobility, high thermal conductivity, high breakdown voltage, high saturation velocity, and high power density, as previously explained.



(a) (b)

Figure 2.1: (a) Basic structure of GaN-HEMT; (b) band diagram of AlGaN/GaN-HEMT.

Given what has been described above, the GaN-HEMT has been chosen for this dissertation.

A well-established model topology of a GaN-HEMT is presented in [32] and shown in Fig. 2.2. The transistor consists of two parts:

1. **Intrinsic part** consisting of:
   - A current source describing the drain source channel current.

   The channel current is a voltage controlled current source described by [33].

$$I_{ds}(V_{gsi}, V_{dsi}) = f_1(V_{gsi}) \cdot f_2(V_{dsi}, V_{gsi}) \cdot f_3(V_{dsi}) \cdot f_4(\triangle T) \tag{2.2}$$

   where:

   $f_1(V_{gsi})$: Defines the transfer function of the transistor

   $f_2(V_{dsi}, V_{gsi})$: Defines the output conductance of the transistor

   $f_3(V_{dsi})$: Defines the triode region of the transistor

   $f_4(\triangle T)$: Models the behavior of the drain-source current with respect of the temperature

   V_{gsi}: Gate source internal voltage

   V_{dsi}: Drain source internal voltage

   - Two non-linear capacitances between the gate and drain terminals (C_{DG}), and gate and source terminals (C_{GS}). Both capacitances depend on the gate to source and the drain to gate voltages.
   - A drain source capacitance (C_{DS}) is used to model the channel capacitance. This capacitance is constant over the voltage. It is one of the advantages of HEMTs compared to other high-power RF transistors, such as LDMOS. In the LDMOS transistor, the (C_{DG}) is considered as a main non-linear capacitance, which is seen at the output of the transistor. This makes GaN-HEMT a good candidate for switch mode highly efficient power amplifier designs.
   - Small resistances describing the losses between these terminals (R_{GS}).

2. **Extrinsic part** consisting of:
   - Models of the terminal pads. Each of these pads is modeled as inductance, resistance and capacitance between the pads.
   - Models of the flanges. The flange of the drain and gate is modeled as a shunt capacitance (C_{Lead}) and it is connected to a resistor (R_{Lead}) and an inductance (L_{Lead}), as shown in Fig. 2.2.

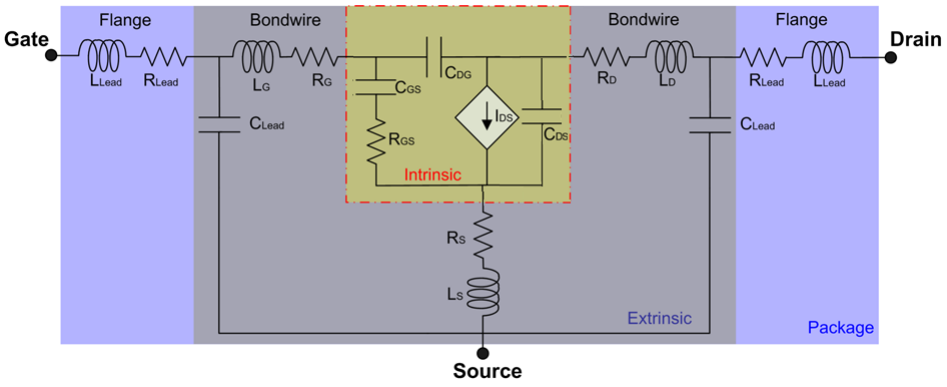


Figure 2.2: Large-Signal model of GaN-HEMT.

The equivalent circuit model of the intrinsic transistor is shown in Fig. 2.3. It consists mainly of a current source connected in parallel with high value drain source resistance (r_{ds}).

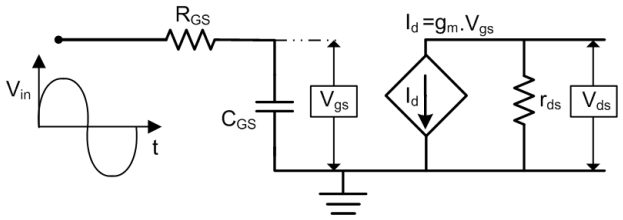


Figure 2.3: Simple equivalent circuit of the transistor.

The drain current source has upper and lower limits, and is used to calculate the optimum load impedance of the device, as presented in Eq. 2.3, where the drain voltage ranges from 0 to V_{max} and the drain current ranges from 0 to I_{max}. To get the maximum power in highly linear operation, the voltage and the current waveforms should swing between maximum and minimum ranges of DC drain voltage and current, as shown in Fig.2.4. The optimum load impedance of the maximum power is expressed as:

$$R_{opt,Load} = \frac{V_{max} - 0}{I_{max} - 0} = \frac{2 \cdot V_{DC}}{I_{max}} = \frac{V_{max}}{2 \cdot I_{DC}} = \frac{V_{DC}}{I_{DC}} \tag{2.3}$$

The drain current and voltage waveforms relation can be as well expressed through the load-line curve which has a slope of:

$$\sigma = \frac{1}{R_{opt,Load}} \tag{2.4}$$

Fig. 2.4 presents the load-line curve, the drain current and the voltage waveform relation. The Figure also presents all the cases of the load impedance values as follows:

- Case 1: $R_L < R_{opt,Load}$
  - Drain current swings between [0, I_{max}].
  - Drain voltage swings symmetrically around the V_{DC} between $-\frac{V_{max}}{2} < V < \frac{V_{max}}{2}$.

This operation is called a current clipping case.

- Case 2: $R_L > R_{opt,Load}$
  - Drain current swings symmetrically around the I_{DC} between $\frac{-I_{max}}{2} < I < \frac{I_{max}}{2}$.
  - Drain voltage swings between [0, V_{max}].

This operation is called a voltage clipping.

- Case 3: $R_L = R_{opt,Load}$
  - Drain current swings between [0, I_{max}].
  - Drain voltage swings between [0, V_{max}].

It can therefore be concluded that the transistor works with maximum rating condition in this case, where the drain current and voltage have maximum swing ranges.

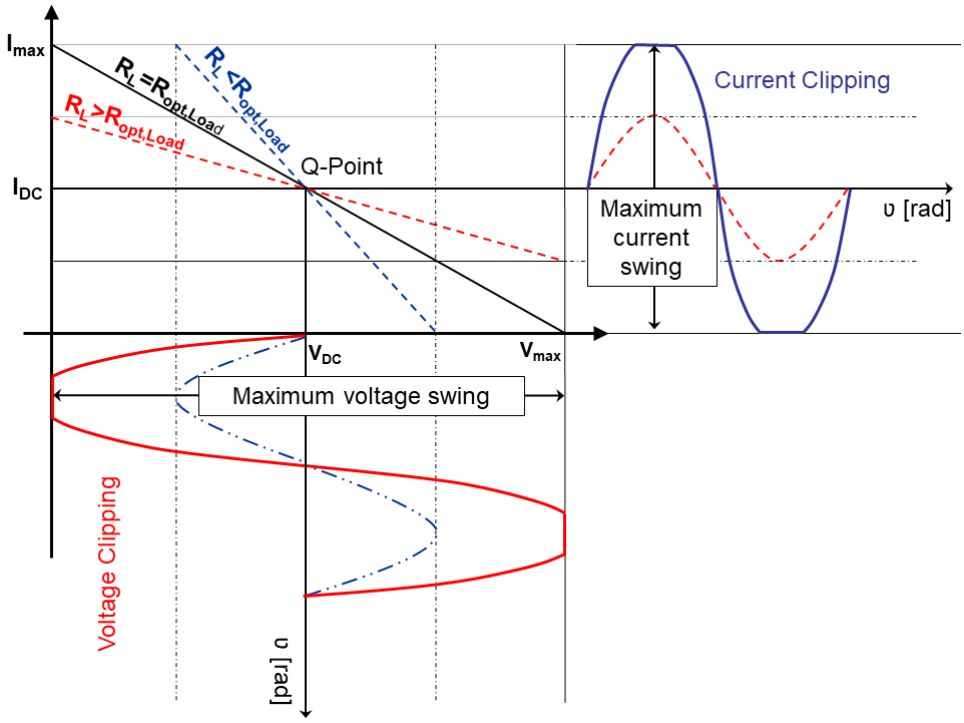


Figure 2.4: Load-line characteristic cases.

2.3 Definition of power amplifier parameters

A radio frequency power amplifier is generally defined as an electronic active circuit with an amplification function to amplify the supplied low radio frequency input power to high output power level. This amplification function refers to the gain of the amplifier. The active devices require a DC-supply to get this function.
Fig. 2.5 introduces various power definitions. The available power from the source is defined as $P_{av,S}$. It is equal to the P_{in} if the input matching network is a conjugate match at the source side. The $P_{av,L}$ is the device output power which is equal to the P_{out} if the output matching network is a conjugate match at the source side, ideally matched; otherwise, it is larger than the P_{out} because of the mismatch, resulting in losses.

1. **Power definitions**

   $DC-$**Input power (P_{DC})** is the provided power at DC to the DUT. The power amplification depends mainly on this power.

$$P_{DC} = V_{DC} \cdot I_{DC} \tag{2.5}$$

   where:

   V_{DC} : DC-supply voltage $[V]$

   I_{DC} : DC-supply current $[A]$

   - Based on Fig. 2.5, the P_{DC} also can be described based on the maximum drain current and voltage swing.
   - $RF-$**Input power (Pin)** is the available input power to the transistor.

$$P_{in} = \frac{1}{2} \cdot Re\left\{V_{in} \cdot I_{in}^{*}\right\} \tag{2.6}$$

   where:

   V_{in}: Input voltage of the transistor $[V]$

   I_{in} : Input current of the transistor $[A]$

   - $RF-$**Output power (P_{out})** is the delivered power to the external load.

$$P_{out} = \frac{1}{2} \cdot Re\left\{V_{out} \cdot I_{out}^{*}\right\} \tag{2.7}$$

   where:

   V_{out}: Output voltage of the transistor $[V]$

   I_{out} : Output current of the transistor $[A]$

- **Dissipated power ($\mathbf{P}_{diss}$)** refers to the total dissipated power in the amplifier, including ohmic losses, switching losses and losses in matching networks. It can be simply defined, based on Fig. 2.5, as:

$$P_{diss}[W] = P_{DC}[W] - P_{out}[W] \tag{2.8}$$

It can be as well defined as the overlapped area between the output voltage and current over a period T of the RF signal. Reducing the conduction angle leads to decrease the overlap area between the output voltage and current of the transistor and results in less dissipated power. Consequently, a highly efficient amplifier can be designed.

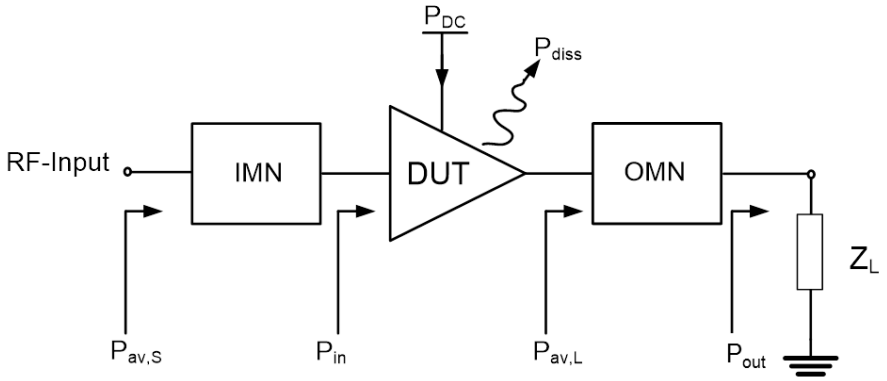


Figure 2.5: Generated power in power amplifier circuit.

2. **Gain definitions**

The gain characteristic has many definitions based on the defined input and output power.

- **Available Gain (G_A)** of PA is the ratio of available power from the DUT to the power available to the DUT, Eq. 2.9. It relies mainly on the source impedance.

$$G_A[W/W] = \frac{P_{av,L}[W]}{P_{av,S}[W]} \tag{2.9}$$

- **Power Gain (G)** of PA is defined as the ratio of the power delivered to an arbitrary load (P_{out}) to the power delivered to the network by the source (P_{in}) input power.

$$G[W/W] = \frac{P_{out}[W]}{P_{in}[W]} \tag{2.10}$$

- **Transducer Gain (G_T)** of PA is the ratio of power delivered to the load and the

available power at the source.

$$G_T[W/W] = \frac{P_{out}[W]}{P_{av,S}[W]} \tag{2.11}$$

The gain in linear units is rarely used. The main definition of the gain is in decibel units. The conversion from linear to decibel units can be expressed in the following equation:

$$G[dB] = 10 \cdot log(G)\,[W/W] \tag{2.12}$$

The main reason why the transducer gain is considered in each step of the PA design is that it is influenced by the source and load impedances. The high flat gain refers that the matching network for input and output of the DUT has perfectly fulfilled the required impedance transformation conditions. The gain of the PA is linear as long as the PA works in linear regions, but the transistor device is defined as a nonlinear device, hence the gain also being defined at compressions points, such as a gain at 1 dB compression point (G_{L-1}) dB or at 3 dB compression point (G_{L-3}) or even X dB compression point (G_{L-x}), where the output power and the efficiency reach the maximum available value as shown in Fig. 2.6.

3. **Efficiency definitions**

   The main factor to evaluate the effectiveness of the power conversion process for the PA is the efficiency. The efficiency of the power amplifier can be described under two definitions. The first definition is presented as the ratio of the delivered output power to the supplied power which is also called **Drain Efficiency** and is defined mathematically in Eq. 2.13.

$$\eta = \frac{P_{out}[W]}{P_{DC}[W]} = \frac{G[W/W] \cdot Pin[W]}{P_{DC}[W]} \tag{2.13}$$

   In the linear region, where the G remains constant, the efficiency of the PA increases exponentially with the logarithmic increases of the input power.

   However, as previously mentioned, if the P_{in} increases further, the gain and DC power start related on the P_{in}, and the efficiency tends to saturate to maximum value, due to the gain compression phenomena related to the nonlinear active device behavior. Therefore, the second definition of efficiency is called **Power-Added-Efficiency** (PAE), which is defined as the ratio between the added power and the supplied DC power.

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \eta \cdot (1 - \frac{1}{G}) \tag{2.14}$$

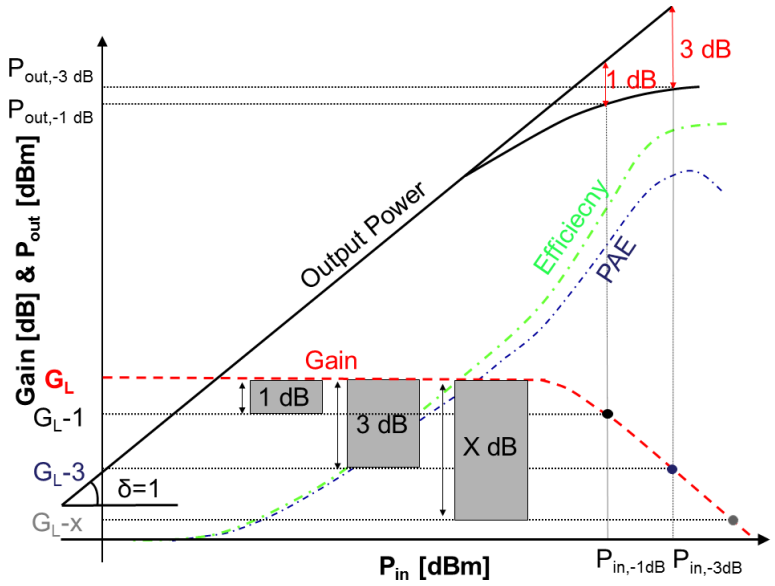


Figure 2.6: Typical performance of the PA versus the input power.

4. **Linearity definitions**

Linear amplifiers are defined as the following:

a) The output power waveform is identical in shape to the input signal.

b) The output signal in frequency domain does not contain other spectral components within or outside the amplifier bandwidth [33].

c) The drain voltage and current remain unclipped for all input power.

However, the power amplifier is mainly defined as a nonlinear component due to its sufficient work in the nonlinear zone at compression points. The nonlinear impact refers to the distortion of the signal waveform. The output power of the transistor consists of an infinite series of nonlinear components expressed via Volterra series form:

$$v_{out} = \alpha_1 v_i + \alpha_2 v_i^2 + \alpha_3 v_i^3 + \cdots \alpha_j v_i^j \tag{2.15}$$

where :

v_{out}: Output voltage $[V]$

v_i: Input voltage $[V]$

α_j: Voltage coefficients

The higher the distortion in the amplifier's output signal waveform is, the less linear the system is. For communications systems using constant amplitude modulation schemes, such as GSM900 which uses GMSK modulation, linearity is not a critical factor [34]. Whereas, the linearity for modern wireless communication standards using signals modulated by a variable amplitude envelope has the highest priority to minimize distortions on transmitted signals. Any increase in the efficiency of a power amplifier usually comes at the cost of linearity and vice versa.

The nonlinear behavior of a power amplifier includes harmonic distortion, intermodulation distortion or spectral spreading. Due to this, various techniques are presented in literature to characterize the linearity of the power amplifier, such as single tone, multitone (two-tone), or a dynamic signal (ACPR/ACLR) modulated signal. As previously mentioned, efficiency is a very important factor in PA's to increase battery lifetime and to minimize thermal problems. Nevertheless, linearity is required for spectrally efficient transmission of high data rate signals [35]. In order to compensate the trade-off between linearity and efficiency, many linearization techniques are introduced to linearize the PA, such as:

a) Feedback linearization technique: This technique forces the output signal to follow the input signal and can be applied at RF or baseband level. At RF level, a portion of the RF output signal of a power amplifier is fed back and subtracted from the RF input signal [34].

b) Feedforward technique: This technique can be used for multi-carrier applications requiring wide bandwidths, but it has a rather complex structure [34, 35].

c) Predistortion technique: This technique has been extensively used for linearization due to its simplicity and ability to be added to the amplifiers to be linearized as separate units [34]. It is basically based on the insertion of a nonlinear component prior to the nonlinear power amplifier in such a way that the combined transfer characteristic is linear, as shown in Fig. 2.7. Predistortion can also be achieved at RF or baseband level. In RF predistortion, the expanding predistorter characteristic is generated by subtracting the compressing amplifier characteristic from the targeted linear characteristic, as illustrated in Fig. 2.7. Improvements in ACPR by 10 dB are typical [34].

d) Digital predistortion technique (DPD): This technique allows the formation and update of the required predistortion characteristic at baseband or RF level [34]. Fig. 2.8 shows the continuous spectrum of modulated signal without using the DPD and with using the DPD.

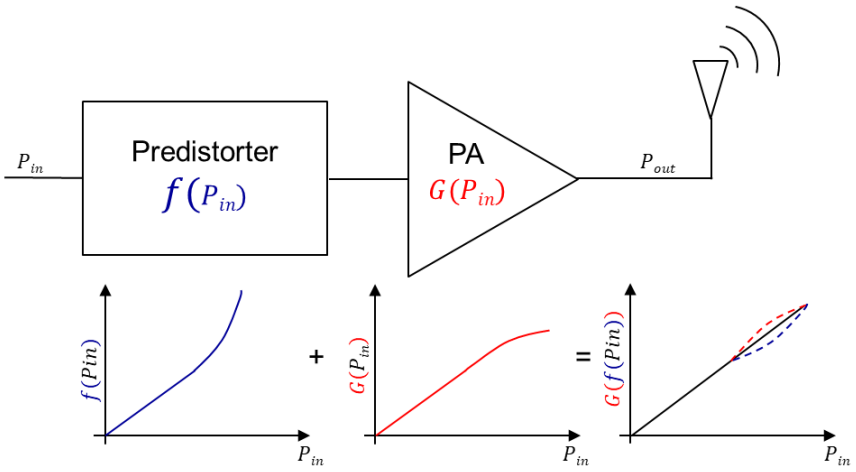


Figure 2.7: Concept of predistortion linearization [2].

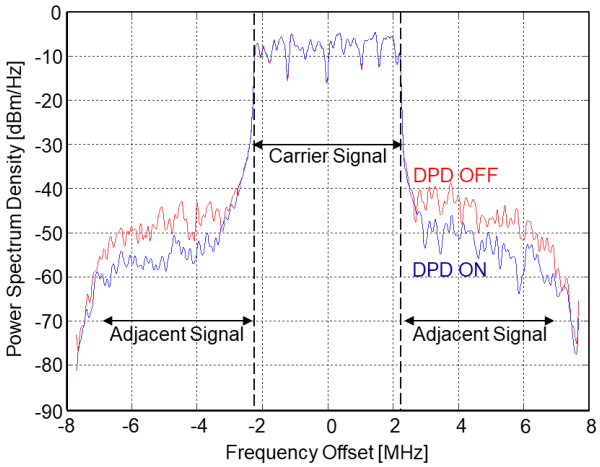


Figure 2.8: Linearization of a modulated signal using DPD.

5. **Stability definitions:**

Stabile power amplifier means that the PA is immune to causing spurious oscillations. All active devices can oscillate without applying any RF-signals due to the high gain response. To be precise, the transistor can oscillate if the supply voltage, impedance, input power, load mismatch or the temperature changes. This is why every PA ever designed must consider the stabilization of the system in order to avoid destroying the active device if the system oscillates. Rollet criteria (or Linville) and K-factor are the most common stability measures. If the K factor is greater than unity over the whole frequency spectrum, the design is unconditionally stable [36]. However, if the K factor is less than unity, then a stabilization network circuit must be involved with the input matching network to apply negative feedback or lossy matching in order to maintain

an unconditionally stable design.

$$K = \frac{1+ \mid \Delta \mid^2 - \mid S_{11} \mid^2 - \mid S_{22} \mid^2}{2 \cdot \mid S_{12} \mid \cdot \mid S_{21} \mid} \tag{2.16}$$

where:

$$\Delta = S_{11} \cdot S_{22} - S_{12} \cdot S_{21} \tag{2.17}$$

Various stabilization networks are presented in Fig. 2.9. The common in-band stability circuit is shown in Fig. 2.9(a), where a parallel RC circuit is connected in series to the gate. The capacitor is used to bypass the RF component in the desired bandwidth. This circuit stabilizes the design in the targeted bandwidth. The self-resonate frequency of this capacitor has therefore been chosen at the center frequency of the desired band. If the desired bandwidth is extremely wide, cascade circuits are used as shown in Fig. 2.9(b). For a narrowband unstable range, the technique in Fig. 2.9(c) is the best choice, because it is used to short out the unwanted RF component. To stabilize the design at lower frequency and from the *DC*-source, the technique in Fig. 2.9(d) was used, where a low ohmic shunt resistor R_{GG} is involved to stabilize the circuit at low frequencies. Frequently, two or many techniques are integrated together in order to ensure a stable design as shown in Fig. 2.9(f). Predominantly, the stability circuit must be located as close as possible to the gate terminal of the transistor in order to reduce the losses and ensure a stable design.

However, the Rollet criterion only concerns the stability of a linearized circuit around a DC steady case. In other words, it refers to stability analysis of small-signal. Nevertheless, pole-zero identification can be perfectly applied to evaluate the stability based on input power and frequency of the large-signal. This method is applicable for detecting the internal unstable loop in multistage amplifiers and can verify the Rollet method.

Moreover, designs with a high K factor also tend to have low gain and some extra gain can be retrieved by allowing positive feedback around the device, while keeping the K above the unity. Any device which has a greater K factor, but not so much greater than unity, shows a more aggressive gain/match characteristic than a theoretical unilateral device [37]. However, the stability circuit can directly limit the gain performance of the PA and results in reducing the gain from the available gain of the device. The maximum available gain of the DUT is not considered if the source or load impedances values are realistic or not. The stability of PA is caused due to the negative source impedances which the DUT prefers to see in order to get the maximum available gain.

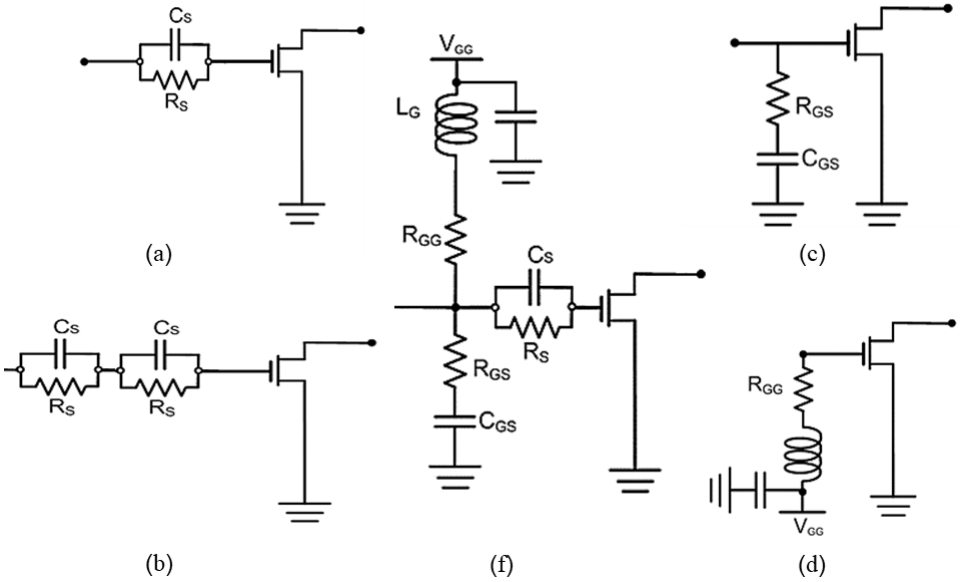


Figure 2.9: Various stabilization circuit topologies.

2.4 Amplifier classes of operation

The classification of power amplifiers presents the relation between voltage and current according to three main criteria:

- **Analog classes:** where the harmonic impedances are terminated with a short circuit. PAs are organized into four classes (class-A, class-AB, class-B, and class-C) depending on the quiescent bias point, which changes the current conduction angle (CCA) as required by each class.

- **Switch-mode classes:** where the active device in this category behaves as a switch and the harmonic impedances are terminated to different impedances such as (class-D, class-E, class-S, and class-F^{-1}). This class of operation can theoretically achieve 100 % efficiency because there is no power dissipated in the device [38].

- **Harmonically tuned classes:** where the active device is considered as a controlled current source and the selection of matching network topologies is based on the instance where the harmonic impedances are terminated to appropriate impedances (Tuned Load, class-F, and class-J). This classification is called harmonically tuned classes (HT-PA). Fig. 2.10 illustrates all the power amplifier category classes. To get a high efficiency PA, the overlap region between the current and voltage in time domain should ideally be zero, In other words, the load line curve must be in ON/Off cases to get 100 % efficiency. This introduction presents the main concept of switch mode PA.

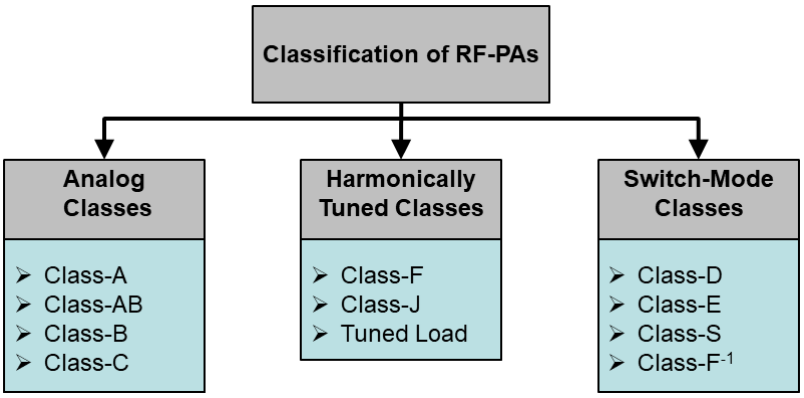


Figure 2.10: Common classification of PAs.

2.4.1 Analog power amplifier classes

These PA classes are also called conventional PA classes. This mainly depends on output CCA. The CCA also relies on the applied quiescent bias. Fig. 2.11 presents the relation between bias point and the current waveform for conventional classes, and illustrates the load line of individual classes from which the following relation can be extracted:

$$\frac{V_{max-C}}{I_{max}} < \frac{V_{max-B}}{I_{max}} < \frac{V_{max-AB}}{I_{max}} < \frac{V_{max-A}}{I_{max}} = \frac{2 \cdot V_{DC}}{I_{max}} \tag{2.18}$$

In other words, it can be described based on the optimum load impedance as follows:

$$R_{opt-C} < R_{opt-B} < R_{opt-AB} < R_{opt-A} = R_{opt-Load} \tag{2.19}$$

As the current conduction angle reduces, the overlapping between the current and voltage minimizes, and the clipping increases. As such, the efficiency increases at the expense of output power and linearity of the PA, as shown in Fig. 2.12.

For an amplifier which has a load line slope of $R_L = R_{opt-load}$, such as class-A, the DC input power, output power, and efficiency can be described based on the drain current and the voltage swing as follows:

$$P_{DC} = V_{DC} \cdot I_{DC} = \frac{1}{4} V_{max} \cdot I_{max} \tag{2.20}$$

$$P_{out} = \frac{1}{2} V_{DC} \cdot I_{DC} = \frac{1}{8} V_{max} \cdot I_{max} \tag{2.21}$$

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{1}{2} = 50\,\% \tag{2.22}$$

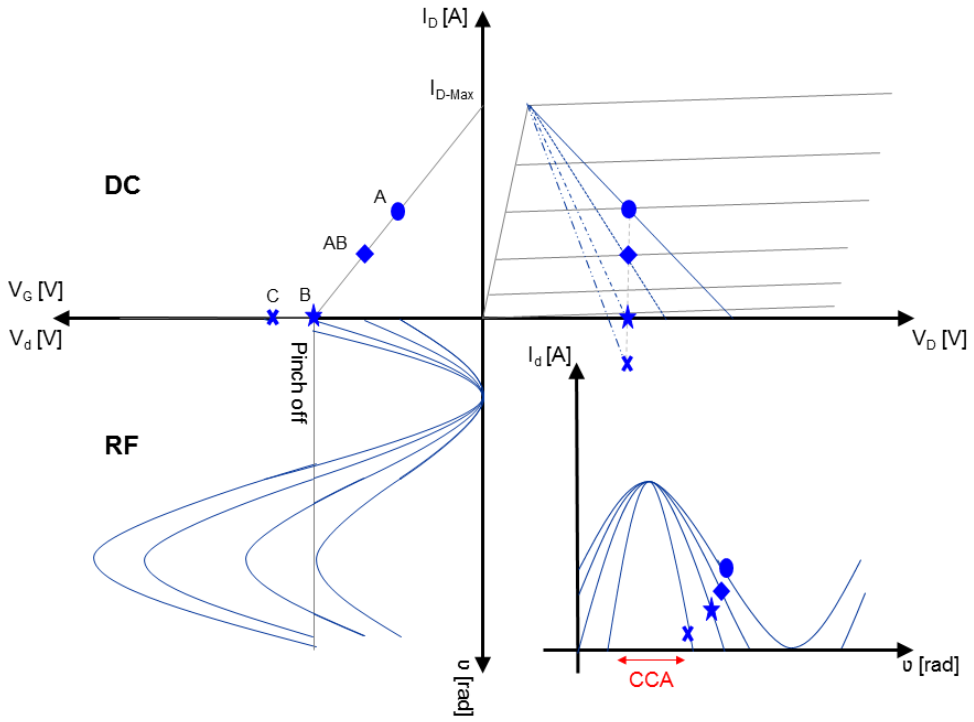


Figure 2.11: Waveforms of analog classes of PAs, load lines and bias points. class-A (● symbol), class-AB (◆ symbol), class-B (★ symbol), class-C (✖ symbol).

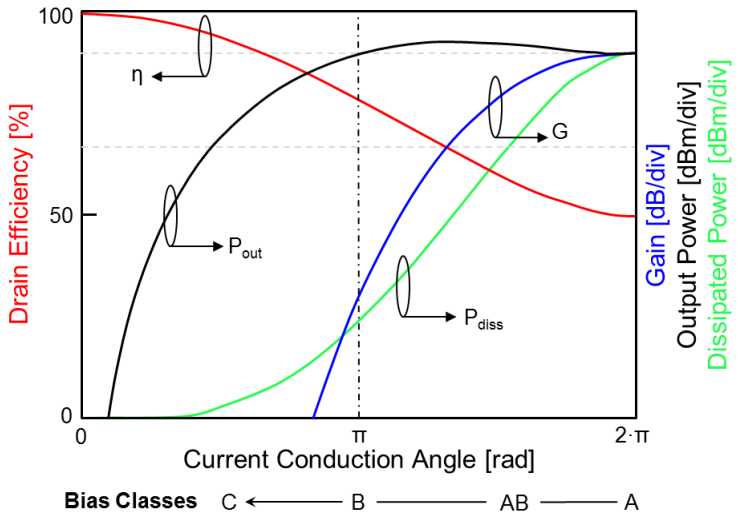


Figure 2.12: Efficiency, output power, gain, and dissipated power of analog PA classes.

Table 2.2 concludes the common specification of each conventional PA classes. The maximum drain efficiency (η_{max}) is defined as follows:

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = \frac{1}{2}\frac{V_{DC} \cdot I_{DS,f_0}}{V_{DC} \cdot I_{DC}} = \frac{(\theta - sin(\theta))}{2[2 \cdot sin(\frac{\theta}{2}) - \theta cos(\frac{\theta}{2})]} \tag{2.23}$$

where:

I_{DS,f_0} : Presents the drain output current conditions.

Table 2.2: Specification of each analog PA classes.

Class	θ $[rad]$	**Efficiency (η_{Max})**	**Linearity**	**Biasing Level**
Class-A	2π	$\eta \leqslant 50\,\%$	++	Between pinch off and saturation
Class-AB	$\pi < \theta < 2\pi$	$\eta \leqslant 78.5\,\%$	+/-	Above pinch off
Class-B	$\theta = \pi$	$\eta = 78.5\,\%$	-	Pinch off
Class-C	$\theta < \pi$	$\eta \leqslant 100\,\%$	--	Below pinch off

To conclude the properties of the analog class amplifier:

- As efficiency improves, the normalized output power and gain drop. Hence, if the output power and gain are reduced to zero, the efficiency becomes 100 %.
- Controlling the current is the only way to improve the efficiency.
- Delivering the power requires the transistor to be ON during throughout.

2.4.2 Switch-Mode power amplifier (SMPA) classes

As previously mentioned, the transistor works as a switch instead of a linear current source in conventional classes, as presented in Fig. 2.13. The switch has two states:

- **ON-state:** the device acts as a short circuit and the current flows through it, where the voltage must be zero.
- **OFF-state:** the device acts as an open circuit and no current flows through it, where the voltage should be equal to V_{max}.

In those two cases, no power can ideally be dissipated in the device, and 100 % efficiency can be achieved. However, the efficiency of the practical SMPA is less than 100 % due to many parameters, such as non-idealities of components (parasitic elements, finite on-resistance, non-zero transition time and non-zero knee voltage) [39].

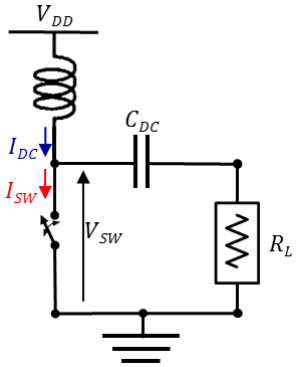


Figure 2.13: Basic concept of switch-mode PA.

1. **Class-E power amplifier**

   This PA was introduced by [40] in details. Fig. 2.14 shows the typical circuit schematic of class-E PA. The load network consists of:

   a) Inductor (L_0) in series with a capacitor (C_0) to pass the fundamental components to the rest of the network.

   b) Inductive load impedance ($j \cdot X_L$) to tune out the internal capacitance (C_{ds})

   In order to ensure a high efficiency in class-E PA, the following conditions should be fulfilled based on [25, 39, 40]:

   - The optimum load impedance is:

   $$Z_L = R_L + j \cdot X_L = R_L \cdot (1 + j \cdot tan(49.05^o)) \tag{2.24}$$

   where:

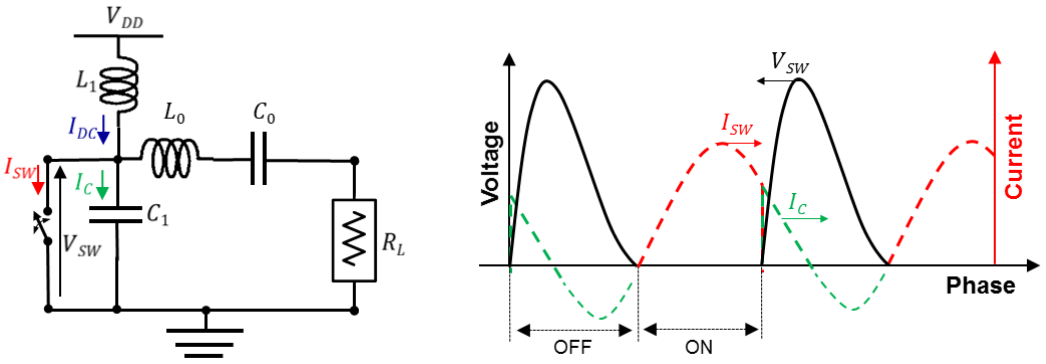
   $$R_L = 0.5768 \cdot \frac{V_{DC}^2}{P_{out}} \tag{2.25}$$

   - Limiting in operating frequency f_{max}, due to the transistor output capacitance (C_{ds}). The maximum operating frequency for class-E is:

   $$f_{max} = \frac{I_{sw-max}}{56.5 \cdot C_{ds} \cdot V_{DC}} \tag{2.26}$$

   - The output capacitance (C_{ds}) of the transistor is limited by the following equation:

   $$X_{ds} = \frac{0.1836}{R_L} \tag{2.27}$$

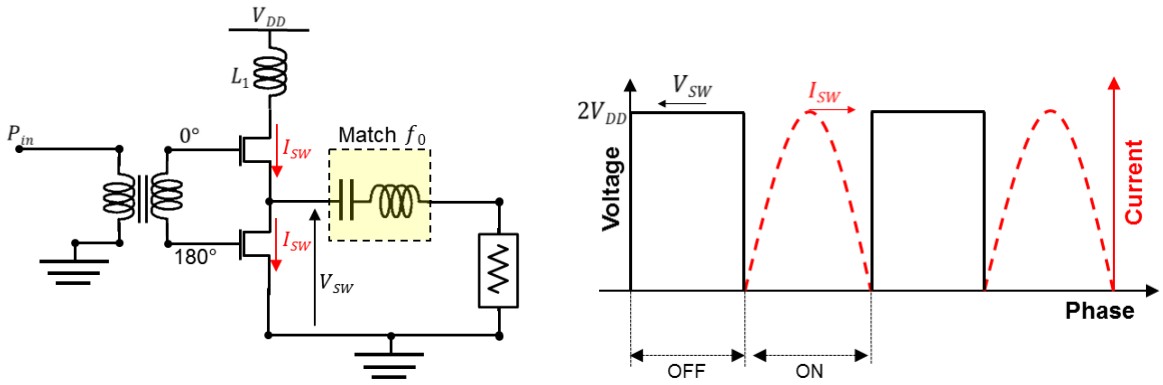


(a) (b)

Figure 2.14: (a) Circuit topology of class-E PAs; (b) ideal current and voltage waveforms of class-E PAs.

2. **Class-D power amplifier**

This power amplifier uses two transistors with a 180° out of phase and is called a voltage mode class-D power amplifier, where the switch voltage is tuned in a square shape waveforms, as shown in Fig. 2.15(b). It can also be called a current mode class-D or inverse class-D (class-D^{-1}), where the current waveform of the transistor is shaped in a square shape, as shown in Fig. 2.16(b)



(a) (b)

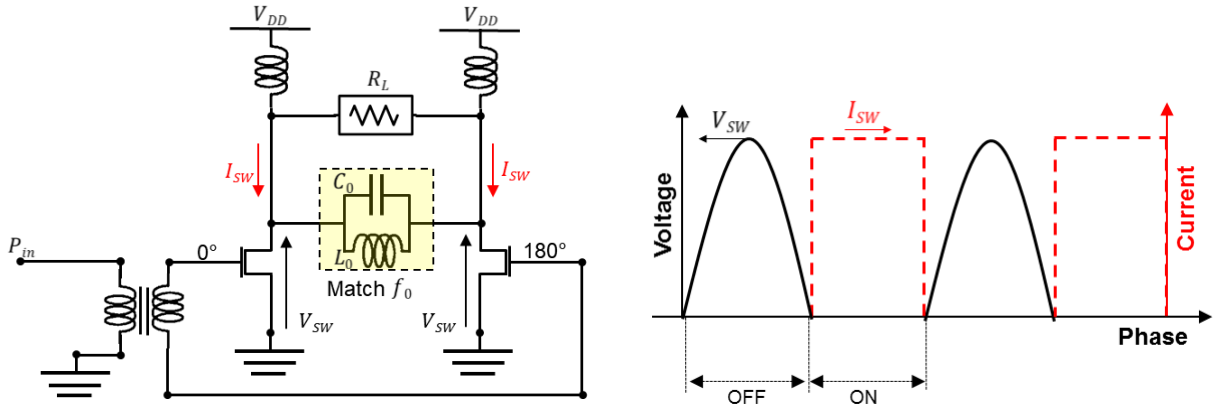
Figure 2.15: (a) Circuit topology of class-D PAs; (b) ideal current and voltage waveforms of class-D PAs.

This class of operation is common at low frequency and widely used in audio applications. This class can theoretically achieve 100 % efficiency, due to the fact that there is no overlap between current and voltage waveforms. Nevertheless, it is hard to be realized for microwave frequency ranges due to:

a) The difficulty of switching at high frequency.

b) Device parasitics such as drain-source capacitance and lead inductance result in losses in each cycle.

c) In reality, there are non-zero switch resistances, because capacitive and inductive parasitics restrict the shape of voltage waveform in class-D PA or the current waveform in inverse class-D (class-D^{-1}).



(a) (b)

Figure 2.16: (a) Circuit topology of inverse class-D PAs; (b) ideal current and voltage waveforms of class-D PAs.

3. **Inverse class-F (class-F^{-1}) power amplifier**

This is preferred method for designing high efficiency power amplifiers, where the designer only controls fundamental and second harmonic of the load impedances. The third harmonic, however, should be short circuited.

At large-signal measurement, the current and voltage swings are no longer purely sinusoidal, but contain a large number of harmonics. Nevertheless, controlling these harmonics results in a high conversion efficiency [41], which mainly defines the class inverse of class-F power amplifiers.

The following impedance conditions should be fulfilled to achieve a high efficiency and define the inverse class-F power amplifier:

$$Z_L[f_0] = Z_{opt} \tag{2.28}$$

$$Z_L[2nf]_{n>1} = \infty \tag{2.29}$$

$$Z_L[2\cdot(n+1)\cdot f_0]_{n>1} = 0 \tag{2.30}$$

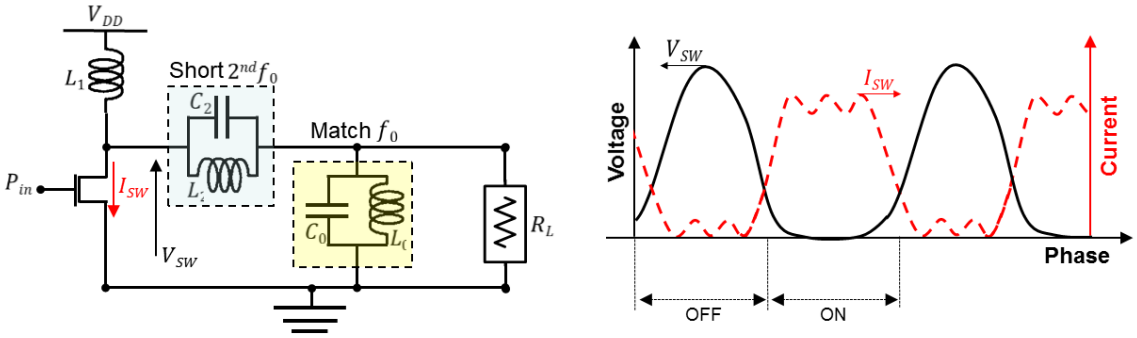
where:

f_0: Fundamental frequency

n: Harmonics number

Z_{opt}: Optimum load impedance at fundamental frequency

The circuit schematic and the ideal waveforms are presented in Fig. 2.17



(a) (b)

Figure 2.17: (a) Circuit topology of inverse class-F PAs; (b) ideal current and voltage waveforms of inverse class-F PAs.

2.4.3 Harmonically tuned power amplifier (HTPA) classes

In the previous Section, the ideal impedance termination conditions for different classes of operation were presented. These conditions mainly limit the power amplifier bandwidth. Nevertheless, in the HT-PAs, these conditions are relaxed to expand the bandwidth of operation of the design. This class includes:

1. **Class-F power amplifier:**

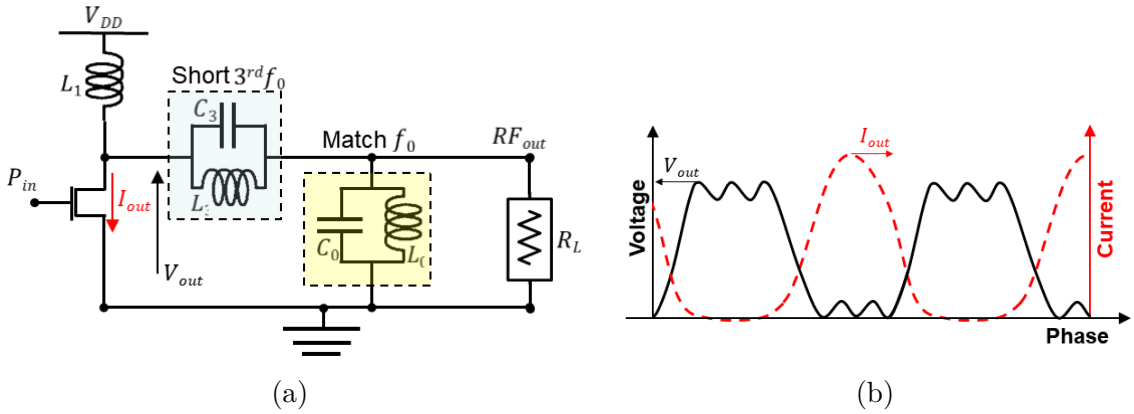
   This class of operation achieves a high efficiency. The optimum impedance for this class should fulfill the following conditions based on [37]:

$$Z_L[f_0] = Z_{opt} \tag{2.31}$$

$$Z_L[2n \cdot f]_{n>1} = 0 \tag{2.32}$$

$$Z_L[2{\cdot}(n+1) \cdot f_0]_{n>1} = \infty \tag{2.33}$$

   The circuit schematic and ideal waveforms of the class-F power amplifier are presented in Fig. 2.18



(a) (b)

Figure 2.18: (a) Circuit topology of class-F PAs; (b) ideal current and voltage waveforms of class-F PAs.

2. **Class-J power amplifier:**

   This class was basically developed based on class-B amplifiers. It was introduced by [37]. This class has high performance in terms of efficiency and linearity with a simple matching network. The main advantages of class-J are a complex impedance presented at fundamental and reactive termination for second harmonics, that can be physically realized using the device output capacitance. [42] presents the form of the fundamental and second harmonics value of the class-J.

3. **Tuned load power amplifier:**

   The concept of this class is close to the approach in class-J. In this class, the optimum fundamental impedance can be defined as a complex impedance which includes real part and inductive part, where the second harmonics are defined as a region instead of a specific value in the reactance area of the Smith chart. The third harmonics are defined as well as a safe region in capacitance area of Smith chart. This approach gives the RF-designer more flexibility to design a broadband power amplifier with high efficiency and linearity.

2.5 Power, efficiency and bandwidth limitation in power amplifiers

This Section presents the challenges which prevent power amplifiers from achieving their aims in terms of output power, efficiency, and bandwidth. They can be summarized by the following three points.

2.5.1 Transistor technology

Besides the previously discussed comparison of the common semiconductors in Section 2.1, Fig. 2.19 compares the most widely used semiconductors in the transistor domain. The power density of the GaN-HEMT technology is almost four times higher than the Si-LDMOS one at the expense of technology price, which is approximately four times higher than the LDMOS

technology, as shown in Fig. 2.19. Additionally, the GaN technology has a very low drain-source capacitor value which is almost 50 % less than the LDMOS technology which results in a larger bandwidth design.

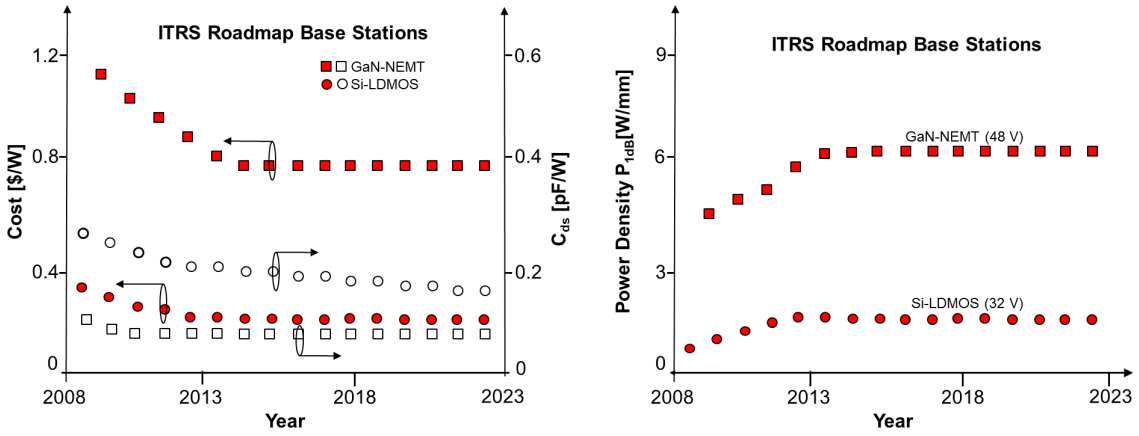


Figure 2.19: (a) Cost and C_{ds} for GaN and LDMOS technology; (b) power density of GaN-HEMT and Si-LDMOS.

2.5.2 Transistor size

Generally, small transistors can be represented as having high impedance R and low parasitic capacitor C compared to big transistors. The high ohmic load of small transistors leads to simple wideband matching networks, which work with a very high reflection coefficient. Unlike with large transistors, which increase the complexity of the matching networks with additional losses over the same defined bandwidth. Table 2.3 presents the simulation results of the reflection coefficient values of four different sized transistors, 10, 25, 45 and 120 W transistors from Wolfspeed Inc. across 1.0 - 2.5 GHz. This simulation has been carried out based on the Bode-Fano criterion. The results show that the 120 W device has a reflection coefficient of -10 dB compared to the -20 dB for the smaller size of transistor 45 W over 1.0 - 2.5 GHz.

Table 2.3: Reflection coefficient based on Bode-Fano criterion over 1.0 - 2.5 GHz.

Transistor	CGH40010	CGH40025	CGH40045	CGH40120
$\lvert \Gamma \rvert$	-40	-30	-18	-10

2.5.3 Bode-Fano limit analysis

Research conducted by Bode and Fano [43, 44] has led to a theoretical limit which describes the matching-bandwidth trade-off that can ideally be implemented with a lossless matching network for a given load impedance. A simple output impedance model of the transistor usually consists of a shunt R - C circuit, as shown in Fig. 2.20.

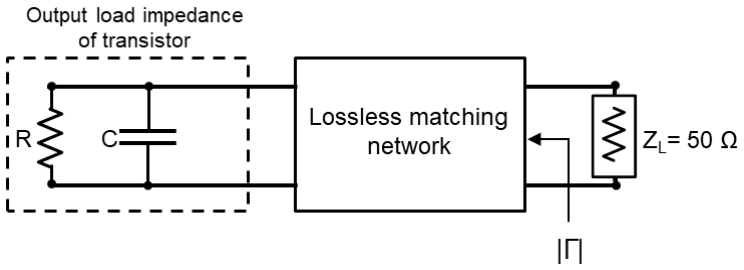


Figure 2.20: Simplified lumped circuit model of the output impedance of a transistor.

Using the output impedance model of the transistor shown in Fig. 2.20, the fundamental limitation is determined:

$$\int_0^\infty \frac{1}{|\,\Gamma\,|} d\omega \leq \frac{\pi}{R \cdot C} \tag{2.34}$$

Solving Eq. 2.34 for the reflection coefficient | Γ | leads to:

$$\Delta\omega ln \frac{1}{|\,\Gamma\,|} \leq \frac{\pi}{R \cdot C} \tag{2.35}$$

where:
$\triangle\omega$: Bandwidth
Γ: Reflection coefficient
$R - C$: Simple model of output impedance of transistor

As a result of this equation, the reflection coefficient |Γ| that can ideally be obtained for a given load impedance over a particular bandwidth can be calculated. Moreover, the bandwidth of the network is mainly related to the reflection coefficient |Γ| value, as shown in Fig. 2.21. | Γ_{min} | is defined as the minimum possible reflection coefficient for a given bandwidth. Increasing the |Γ| results in increasing the bandwidth of the matching network at the cost of loss and efficiency, as shown in Fig 2.21. This analysis concludes that the wideband power amplifier can be designed using a matching network with a high reflection coefficient compared to narrowband design.

Moreover, the quality factor of the output load impedance circuit of the transistor can be expressed as:

$$Q_c = \frac{\pi}{R \cdot C \cdot \omega_0} \tag{2.36}$$

Based on this equation, the quality factor of the output impedance of transistor is also a crucial factor regarding the achievable bandwidth. Larger transistors with low R and high C are obviously more challenging to match than smaller transistors.

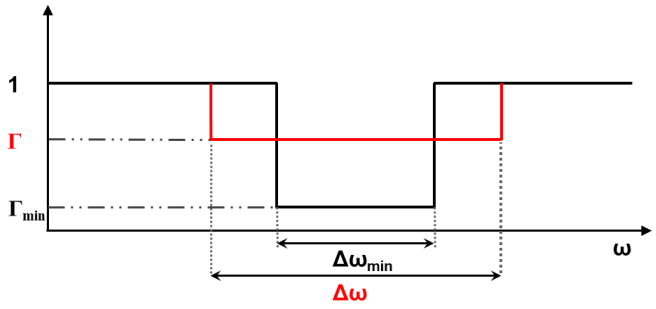


Figure 2.21: Relation between reflection coefficient and bandwidth, Γ_{min} assumed for minimum bandwidth, Γ assumed for wider bandwidth.

2.5.4 Effects of transistor knee voltage

The real current and voltage curves of FET transistor are presented in Fig. 2.22. It is clear that the device needs a threshold voltage, knee voltage (V_{knee}), to operate, which causes a limiting voltage swing on load impedance line. This is why the output power and efficiency are lower than the ideal presented study in textbooks.

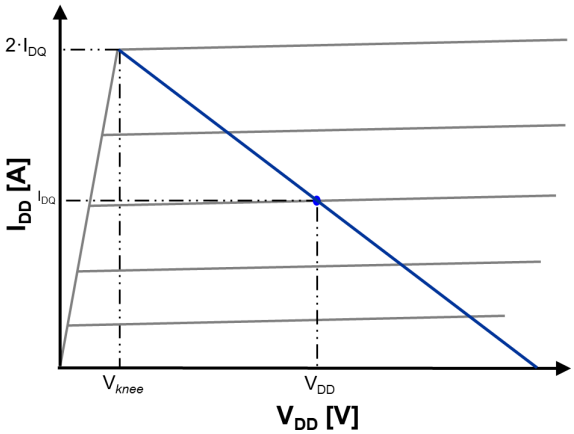


Figure 2.22: Drain current versus drain voltage observing the knee voltage of the transistor.

The following equations mathematically represent the impact of V_{knee} to the optimum load impedance, output power, and efficiency for a class-A PA. This influence is mainly related to the value of knee voltage ratio to the DC-supply voltage.

$$R_{opt,load-knee} = \frac{V_{DD} - V_{knee}}{2 \cdot I_{DD}} \tag{2.37}$$

$$P_{out,knee} = \frac{1}{2} \cdot (V_{DD} - V_{knee}) \cdot I_{DD} \tag{2.38}$$

Additional power is dissipated in the transistor and given by:

$$P_{diss,real}[W] = P_{diss} - P_{out,knee} = P_{DC} - (P_{out} + P_{out,knee})[W] \tag{2.39}$$

The knee output power certainly has an impact on the efficiency performance of the power amplifier, which is shown as follows:

$$\eta_{knee}[\%] = \frac{P_{out,knee}}{P_{DC}} = \frac{\frac{1}{2}\cdot(V_{DD} - V_{knee}) \cdot I_{DD}}{V_{DD}\cdot I_{DD}} = \frac{1}{2} \cdot (1 - \frac{V_{knee}}{V_{DD}}) \tag{2.40}$$

If the knee voltage to DC-Supply voltage is 10 %, the drain efficiency is 10 % less than the ideal case.

2.6 Power amplifier matching network topologies

After presenting the physical and the electrical concept of the transistor, the next important approach is the matching network topology. A matching network is used mainly between source and load impedance to reduce the voltage standing wave ratio (VSWR), as both of these do not have the same characteristic impedance in order to ensure a low loss transmitted signal with low reflected signal to the source and load terminations.

In this dissertation, the extracted optimum source-/load-impedances of the transistor should be matched to the source and load impedances of the system that is in most cases (50 Ω). In general, matching networks topologies rely on the desired bandwidth of the PA. They are simple as long as the desired PA works in narrowband, and they become more and more complex by increasing the bandwidth of operation. Fig. 2.23 presents the inductive and capacitive regions on the Smith chart. It also presents the influence of adding a series/ parallel coil or capacitor at single frequency point for arbitrary load impedance. Nevertheless, the main goal of this dissertation is to match wideband source-/load-impedances of a transistor to 50 Ω.

Some fundamental equations are presented before introducing the most common matching network topologies. The reflection coefficient can be expressed in Eq. 2.41.:

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{2.41}$$

where:

Γ: Reflection coefficient

Z: Impedance value [Ω]

Z_0: Characteristic impedance value [Ω]

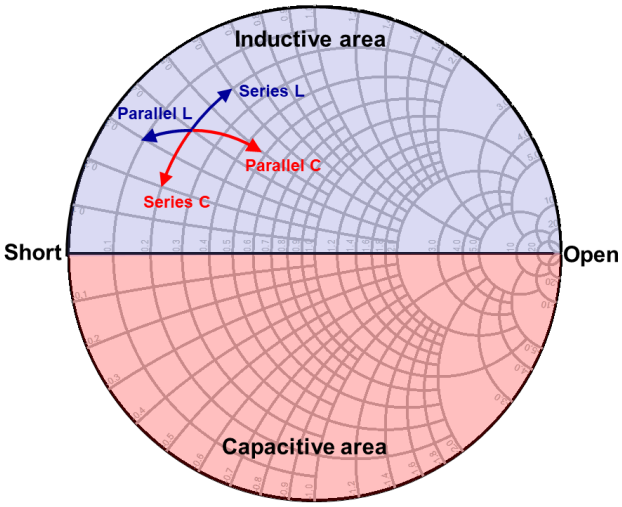


Figure 2.23: Capacitive and inductive regions in the Smith chart, impacts of adding coil and capacitor in parallel and series circuit in the Smith chart. Blue traces and region refer to the inductive area, whereas the red traces and region refer to the capacitive area.

The reflection coefficient can also be defined based on the voltage standing wave ratio:

$$\Gamma = \frac{VSWR - 1}{VSWR + 1} \tag{2.42}$$

The matching network can be designed using one of the following elements:

- Lumped elements are used up to 1.0 GHz, and it can be used even with modern microwave integrated circuit technology into millimeter-wave region.
- Distributed elements are recommended for microwave and high frequency range.

2.6.1 Narrowband matching network topologies

The narrowband matching network can be designed using single or higher orders of filter. Low-pass filter is the most used filter in designing the matching network. It is also called a ladder topology matching network. The number of orders depends on how sharp the cut-off frequency should be, as shown in Fig. 2.24. Moreover, increasing the order of the filter can expand the bandwidth of operation of the filter with a cost of losses and decreasing the efficiency of power amplifiers.

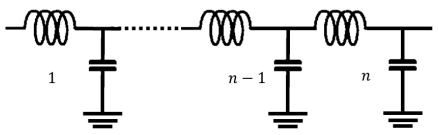
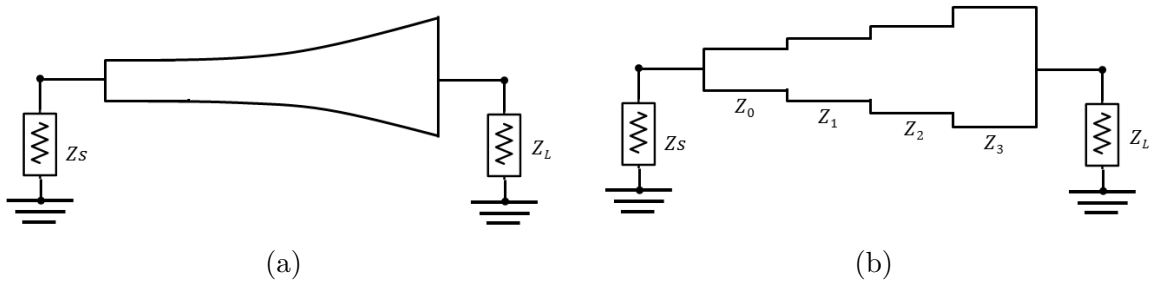


Figure 2.24: Schematic of the matching network using typical ladder topology.

2.6.2 Wideband matching network topologies

The following approaches are the most used concepts to design a wideband matching network:

- **Tapered transformer:** consisting of many types with the most common types of tapered transformers being triangular taper, exponential taper, and Klopfenstein taper. These topologies are seldom used in the design of wideband matching networks for power amplifiers, due to the difficulty in tuning and modifying the topology. Instead, a multi-section transformer with different width and length is used. This topology can be tuned and modified to fulfil the optimum transformation ratio. Fig. 2.25 shows the comparison between the taper transformer and multi-section transformer schematic. Increasing the number of sections and the total length results in expanding the bandwidth of the transformer. Adding multiple transformation sections in series is similar to lossy wideband matching topology and results in low efficient power amplifier.



(a) (b)

Figure 2.25: Schematic comparison between multi-section transformer and tapered transformer.

- **Twisted-wire pair transformer:** used in a lot of applications, including matching network and baluns. This transformer is used to overcome the lossy wideband matching network, especially in the VHF and UHF band and below [45, 46], for decades bandwidth PA designs. Unfortunately, the widely used semi-rigid coaxial transmission lines and especially ferrite cores are typically not suitable to the microwave range. This approach involves two transformer techniques:

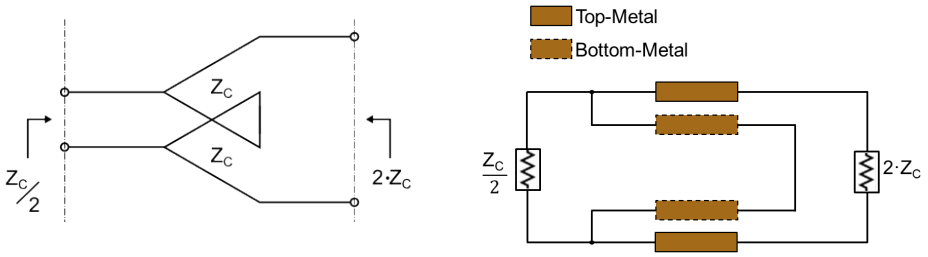
1. **Guanella transformer:** the main concept of this transformer is coiling transmission lines to form a choke that would suppress the undesired mode from unbalanced to balanced matching applications [47, 48].

2. **Ruthroffs transformer:** transmitting energy by transverse transmission line mode. This transformer gives wider bandwidths with lower insertion loss [49].

3. **Planar transmission line transformer:** using traditional transformers to realize an impedance transformation between the input port and one or more output ports [47, 48, 49] is limited in terms of cut-off frequency, either because of losses in the material or the physical dimensions limiting the options for mounting the component. Planar transmission line transformer is therefore the preferred solution in terms of complexity,

cost, bandwidth capability, and insertion loss [50, 51, 52]. It has been recently developed based on the previous two techniques, such as the planar Guanella transformer [50, 53], to expand the bandwidth of operation up double octave to decade bandwidths with a very low insertion loss. This transformer works as well up to Ka- or even K-band frequencies. This transformer is used in this dissertation to overcome the bandwidth limit and to be used in the design of highly efficient ultra-wideband power amplifiers, such as [Paper C] and [Paper D]. More details on the theoretical and practical concept of the planar transformer will be presented.

The planar transmission line transformer should consider all parameter influences, such as dielectric losses, length, width, and coupling. The transformer consists of two transmission lines with characteristic impedance Z_C connected in parallel at the transformer input plane and in series at the transformer output plane. Consequently, the impedance seen at the input plane is the half of the characteristic impedance ($Z_C/2$). The impedance seen at the output plane is double of the characteristic impedance ($2 \cdot Z_C$), as shown in Fig. 2.26. In this case, the resulting transformation ratio is 4:1. The two-layer schematic, including coupled microstrip lines (MSL) and via connection, is depicted in Fig. 2.26(b).



(a) (b)

Figure 2.26: (a) Concept of broadside-coupled planar transformer; (b) schematic of the planar transformer.

For high bandwidth, the characteristic impedance ratio of even-/odd-mode of the broadside coupled suspended MSL is critical and should be high to ensure a tight coupling. Thus, the distance between bottom MSL and ground shield is an important factor. The greater the distance to the ground shield, the greater the Z_{even} is and an efficient broadband transformation is possible. A shielded stripline assumption is intended to illustrate this concept. Fig. 2.27(a) and (b) depict the electric field lines for even-/odd-mode for two broadside coupled shielded striplines ($\varepsilon_1 = \varepsilon_2 = 1$). The Eq. 2.45 and Eq. 2.46 represent the even mode and odd mode characteristic impedance of broadside coupled suspended MSL ($\varepsilon_1 = 1 < \varepsilon_2$) which are derived from the shielded stripline model [54].

$$Z_{0,e} = \frac{Z^a_{0,e}}{\sqrt{\varepsilon_{r,e}}} \tag{2.43}$$

$$Z_{0,o} = \frac{Z^a_{0,o}}{\sqrt{\varepsilon_{r,o}}} \tag{2.44}$$

where:

$Z_{0,e}$: Even mode impedance of the air-filled stripline model

$Z_{0,o}$: Odd mode impedance of the air-filled stripline model

$\varepsilon_{r,e}$: Effective relative permittivity for even mode

$\varepsilon_{r,o}$: Effective relative permittivity for odd mode

The coupling factor between two transmission lines is given in Eq. 2.45

$$C = 20 \cdot log \frac{(1 - c^2 \cdot cos\beta l)^{\frac{1}{2}}}{c \cdot sin\beta l} \tag{2.45}$$

where:

βl : Electric length of the transmission line

c : Presents the impedance ratio as follows

$$c = \frac{Z_{0,e} - Z_{0,o}}{Z_{0,e} + Z_{0,o}} \tag{2.46}$$

The coupling, Eq. 2.45, can be simplified by the assumption that $\beta l = \frac{\pi}{2}$. This leads to the fact that the coupling only depends on the impedance ratio c, which should be close to unity [50] to have a tight coupling. The large even-mode impedance has therefore to be realized using a sufficiently large distance for the ground shield of the broadside-coupled suspended MSL.

Fig. 2.27(c) depicts the simulation results for the even-/odd-mode impedance of a two coupled suspended MSL with a width of 3.1 mm depending on the distance of the ground shield. The Figure illustrates that increasing the distance results in increasing the even characteristic impedance; nevertheless, the cavity cannot be infinite. Therefore, a reasonable distance which ensures a high even mode impedance should be used.

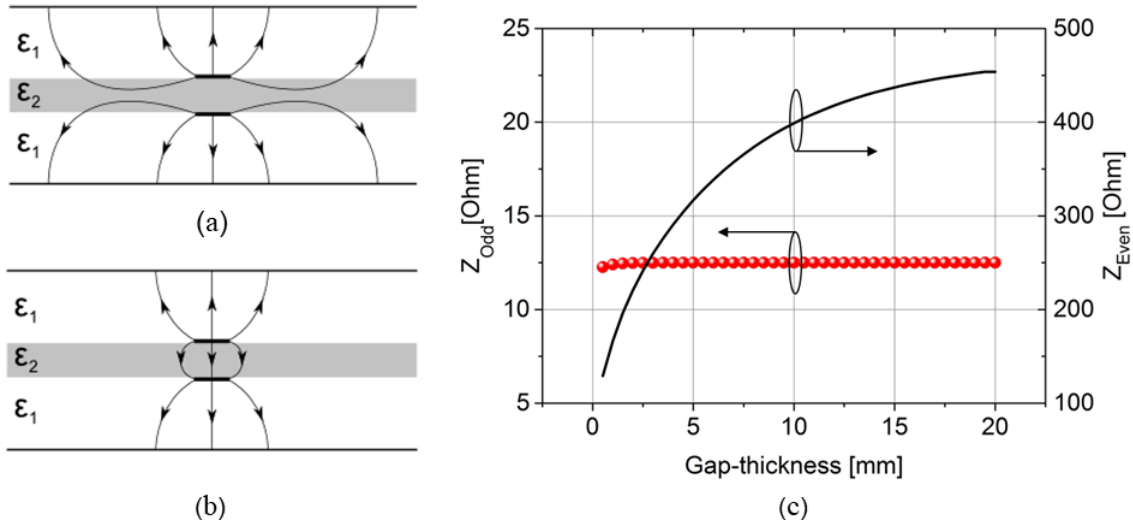


Figure 2.27: (a) Electrical field lines even mode; (b) electrical field odd mode for shielded broadside-coupled lines; (c) even and odd-mode impedance versus shield distance.

2.7 Broadband power amplifier techniques

This Section presents an overview of all techniques which are used to design a broadband power amplifier. It presents in detail the approach of harmonically tuned power amplifiers.

2.7.1 Traveling wave power amplifiers (TWA)

This technique is also called Distributed Amplifier. The influence of input-/output-capacitances of the transistors, which limits the bandwidth of matching networks, was solved using this approach, where the input and output capacitances of several transistors are combined into the artificial transmission-line structure as shown in Fig. 2.28

The main advantages of this technique are:

- Simple circuit topology.
- An achievable wideband power amplifier. Multi-Octave and even multi-decade TWAs have been designed [55, 56].

The disadvantages of this technique are:

- Low PAE performance, due to the low output power [56].
- A high number of active devices required to achieve the same gain as a single device, which results in high costs and large size.
- Large size of the whole design.
- High manufacturing costs.

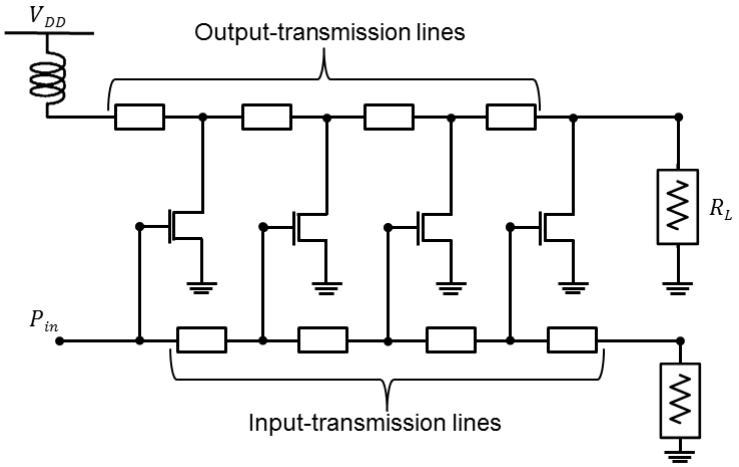


Figure 2.28: Circuit topology of the traveling wave amplifier.

2.7.2 Lossy matched power amplifiers

This technique uses resistors within input-/output-matching networks to ensure flat gain over a wide bandwidth [57]. The resistors increase the impedance levels and result in wideband operation. Fig. 2.29 presents the schematic of the lossy matched power amplifier. The main advantage of this technique is that the PAE is at least four-times higher than the four stages TWA [57].

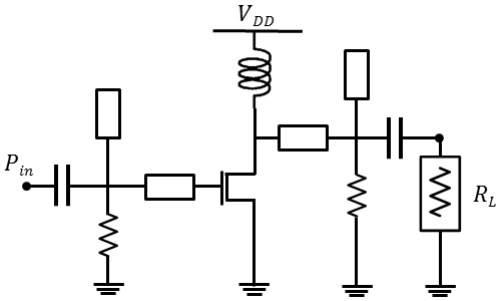


Figure 2.29: Circuit topology of the lossy matched power amplifier.

2.7.3 Feedback power amplifiers

In this technique, negative feedback is applied to the matching topology by connecting a feedback resistor R_{fb} between the gate and drain of the transistor [58]. This technique stabilizes the device and makes the input and output impedances much closer to the desired $50\,\Omega$ [59]. The resistor controls the gain and bandwidth of the power amplifier. The feedback coils L_{fb} and L_2 can be optimized to extend the amplifier bandwidth [60]. L_1, C_1 and C_2 are used to achieve a good input and output return loss [59]. The feedback power amplifier is better than the TWA in terms of complexity and power-added efficiency. However, the main disadvantage is its low output power, due to a loss associated with the feedback resistor.

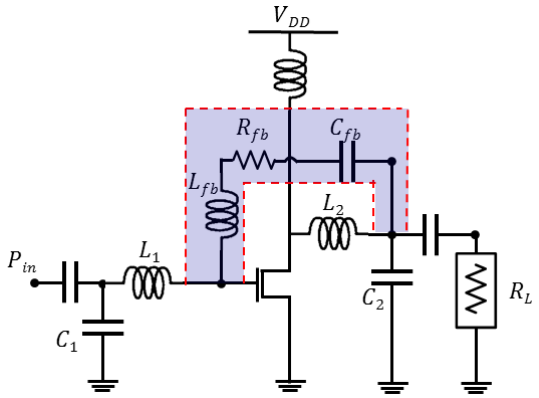


Figure 2.30: Circuit topology of the feedback power amplifier.

2.7.4 Resistive harmonic termination of power amplifiers

This technique is mainly based on optimization of the fundamental impedance, while all higher harmonics are terminated as resistive impedance. This technique can achieve a multi-octave bandwidth of operation but with a low PAE performance. Many designs have used this technique. In [61], a decade bandwidth [0.4 - 4.1] GHz power amplifier with a gain ranged between 10 to 15 dB, and PAE values of 40 % - 60 %, is introduced.

2.7.5 Wideband switched-mode power amplifiers

Switch-mode power amplifier had previously been presented as a candidate, that can provide high efficiency. The resistive harmonic termination technique can achieve a wideband power amplifier, but with a low efficiency due to not matching the higher harmonics. Using switch mode PA or harmonically tuned power amplifier technique can clearly increase the efficiency performance of the power amplifier. The most reported wideband power amplifier is the switched mode class power amplifier. In [11], a wideband class-E PA with a bandwidth of 1.2 - 2.0 GHz is presented with a gain of 1 ∓ 12 dB, and PAE between 67 % - 83 %.

2.7.6 Continuous mode power amplifiers

This approach can achieve a wideband power amplifier with a high and constant efficiency over a continuous range of fundamental and harmonic terminations. The continuous modes of operation have been researched for class-B/J [62], class-F [63], and inverse class-F PAs .

Transferring mode technique for designing a high efficiency wideband PA is introduced in [12]. The matching network matches the fundamental optimum load impedances and ensures proper tuning of the second and third harmonics, allowing the PA to operate between inverse class-F and class-F modes [41].

2.7.7 Harmonically tuned wideband power amplifiers

This technique has been used in many designs [10, 17, 15], as well as in this dissertation. For this reason, more details regarding this technique are presented in Chapter 3 in order to highlight this approach. [Paper A] has used this technique to design a power amplifier with

maximum available power-added efficiency and maximum output power across a wideband frequency range. This approach is based on extracting the optimum fundamental and second harmonic impedances from source-/load-pull setup, as presented in Section 3.2.1. The next step is to design a suitable wideband matching network based on the extracted optimum load impedances of the fundamental and second harmonics. This step is presented in more detail in Section 3.2.2.

3 Efficient Wideband Power Amplifier Designs

In harmonically tuned power amplifiers, the performance depends on presenting a very precise combination of fundamental and harmonic impedances to the intrinsic node of the device, along with an input signal drive level and bias point combination which set the switching duty cycle. In this chapter, an innovative approach to designing an ultra-wideband and highly efficient power amplifier is presented. The operation bandwidth of all designs is defined to be located in the most common wireless communication standards bandwidth, in the range of $0.4-3.0\,\mathrm{GHz}$. Moreover, the relation between bandwidth, efficiency, and linearity is presented from a practical perspective. The aim of this dissertation is to improve the PA efficiency by minimizing the influence of in-band harmonics on power-added efficiency and to significantly increase the bandwidth of operation. Four designs based on GaN-HEMT from Wolfspeed Inc. with various bandwidth and output power are presented in Table 1.1 in Chapter 1.

Alongside the presented approaches in Section 2.6, several approaches to designing a broadband matching network are presented in [64].

To design the proper matching network, there are two main techniques:

1. The numerical technique required for some approaches to achieve the proper matching network. This technique is of value for narrowband matching networks.

2. The real frequency technique is used to design broadband matching networks. This technique is mainly based on bilinear reflection behavior versus lumped and distributed element variables.

In this dissertation, both techniques were used to achieve a broadband, lossless (two-ports) matching network (equalizer). Moreover, a novel approach to design ultra-wideband matching network is proposed and used in second, third and fourth design in this chapter. This approach is Adapted approach of harmonically tuned ultra-wideband power amplifier. This approach has been used for the first time and is presented in this dissertation. The main target of this approach is to solve the in-band problem of designing wideband power amplifier. The core of this approach is to split the defined operation frequency range of the desired PA into mainly sub-bands:

- The low sub-band: All harmonics of the low sub-band are located in high sub-band of the desired PA. Following the approach discussed in Section 2.7.7 to design the matching network, the load impedance at the second harmonic of the low sub-band corresponds to a low ohmic range, which does not correspond to the fundamental impedance termination needed for the high sub-band, to allow broadband operation. Nevertheless, based on the transistor's characteristics, the low frequency has a higher gain compared to the high frequency range. The optimum fundamental load impedances of the low

sub-band are therefore slightly modified without causing a high degradation in performance. This results in reducing the impact of the harmonics on the efficiency, and producing a flatter gain over a wide bandwidth of operation.

- Regarding the high sub-band, the approach discussed in Section 2.7.7 has been used. Where the harmonics should only rely on the safe region close to unity reflection coefficient.

Second, third and fourth designs in this dissertation, which correspond to [Paper B] [Paper C] and [Paper D] respectively, rely on this approach.

3.1 General steps for designing broadband PAs

This Section highlights the main common factors for designing a broadband power amplifier, such as the general flowchart, the source-/load-pull setup and the measurement setup technique.

3.1.1 Power amplifier design flowchart

All steps for designing a power amplifier are presented in the flowchart, as shown in Fig. 3.1.

The first step is to define the main goals of the desired power amplifier in terms of bandwidth, output power, gain, efficiency, linearity, etc. Choosing the proper transistor is a very important factor to fulfill these aims. The transistor characterization must be clearly analyzed in terms of maximum available gain and dissipated power to define the optimum quiescent point of the transistor, before determining the optimum source-/load-impedances. This can be realized using source-/load-pull setup. The specified impedances depend mainly on the frequencies. A continuous curve (locus) for optimum source-impedance/load-impedance is subsequently formed. The determined impedances are mainly related to the purpose of the design. If the main goal is to design a high linear power amplifier, the optimum source-/load-impedances are not similar to the design PA with a maximum available PAE or output power. Furthermore, a trade-off in choosing the optimum impedances is possible, when many goals are simultaneously required from the designed PA.

The next step is to match the extracted impedances to 50 Ω. This step is initially accomplished using ideal lumped elements (LEs) for both source-/load-sides of the transistor. These circuits present the ideal input matching network (IMN) and output matching network (OMN) respectively. If the ideal IMN and OMN have achieved a lossless insertion loss and high absolute value of the return loss, the ideal design should be transformed to real design using real lumped elements and transmission lines (TLs). This step usually causes a slight deviation between the ideal and real circuits of the matching network. Moreover, an additional circuit must be involved in the IMN topology to avoid the transistor oscillating, which causes extra losses as well. The optimization tool must support a compensation of these deviations. Moreover, using this tool cannot be arbitrary. It is restricted by the transmission line's width, length, thickness and other factors. Advanced Design System (ADS) software is a powerful tool to meet the defined goals.

The next step is to design appropriate biasing circuits. Before the fabrication step, an electromagnetic (EM) simulation must be done to verify the schematic simulation results, as shown in Fig. 3.1. If there is a big deviation, the layout of the matching network (MN), especially the OMN, should be modified to minimize this deviation. After accomplishing those steps, the PA can be produced and measured. A slight deviation between measurement and simulation results is acceptable, but if the deviation is large, the fabricated design can be post-tuned and re-measured.

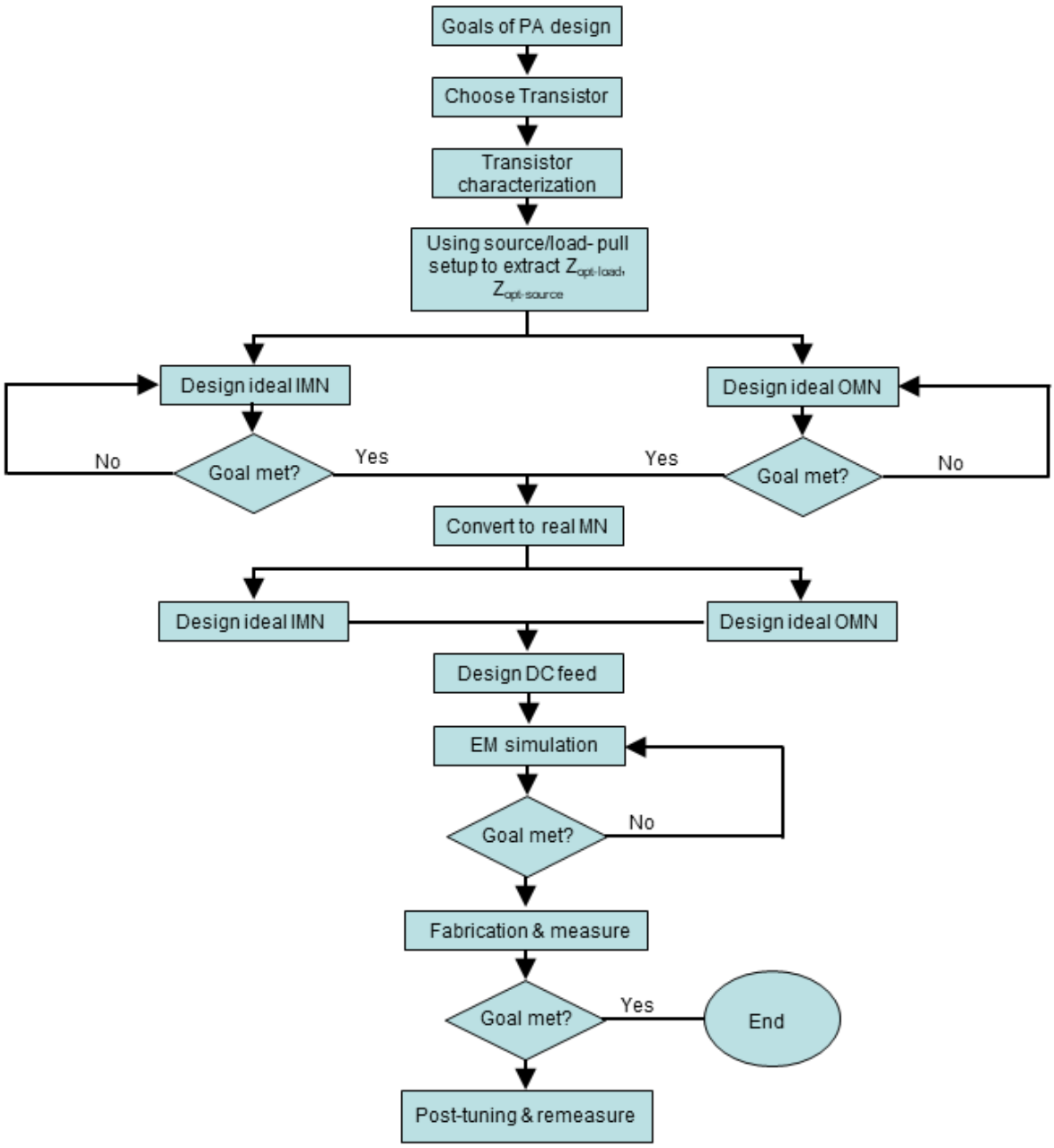


Figure 3.1: General steps for designing a power amplifier.

3.1.2 Source-/load-pull setup technique

Load-pull is a substantial technique in the design testing model validation process of ampli-

fier development. It is also used in test validation of various system modules. There are many methods to perform load-pull. These methods are required for the non-50 Ω measurements. There is a measurement setup tool using a tuner which is quite a precise way to determine the optimum source-/load-impedances in cost and complexity. Nevertheless, if the nonlinear device has a precise model, there are now many other simulation setup tools which provide a precise load-pull simulation. Advanced Design System (ADS) provides a sufficient load-pull simulation tool to extract the optimum source-/load-impedances of the non-linear device based on the required goals, such as output power, PAE, intermodulation, etc. For each goal, there are different optimum load impedance contours. This tool is used for individual frequency across the desired band.

Nevertheless, the PAE and output power contours are located close to each other at the maximum operating range, whereas at lower output power the optimum load impedance of the required output power is far from the optimum load impedance for maximum PAE, as shown in Fig. 3.2. The blue contours present the output power level with a 0.5 dB step, whereas the red contours show the PAE with a 5 % step at 2.0 GHz for a CG40025F device. A certain tolerance is acceptable in the design to balance the goals. In other words, a range of load impedance can be applied to the transistor to design a broadband PA, and this approach is also utilized to design the ultra-wideband PA in this dissertation.

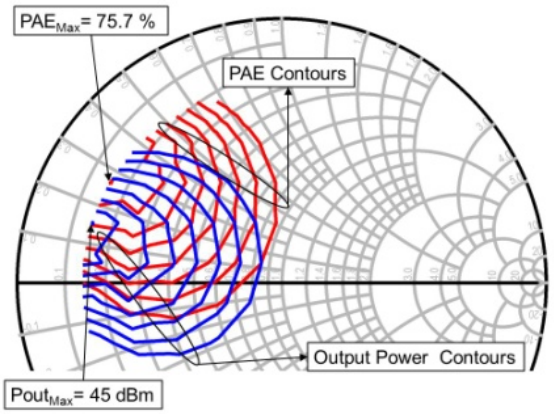


Figure 3.2: Optimum load contours of the CG40025F transistor @ 2.0 GHz for output power (red solid line) and power-added efficiency (blue solid line).

3.1.3 General small-/large-signal measurement setup

The measurement setup of all designed power amplifiers is presented at the beginning of this chapter to avoid any repetition. The small-signal measurement setup is presented in Fig. 3.3. The attenuator is used to save the vector network analyzer (VNA) from the high output power which is delivered from the DUT. The used attenuator value is basically related to the gain of the DUT. Moreover, the general large-signal measurement setup is presented in Fig. 3.4. The only change between all designs is the DUT, pre-drivers and the frequency range.

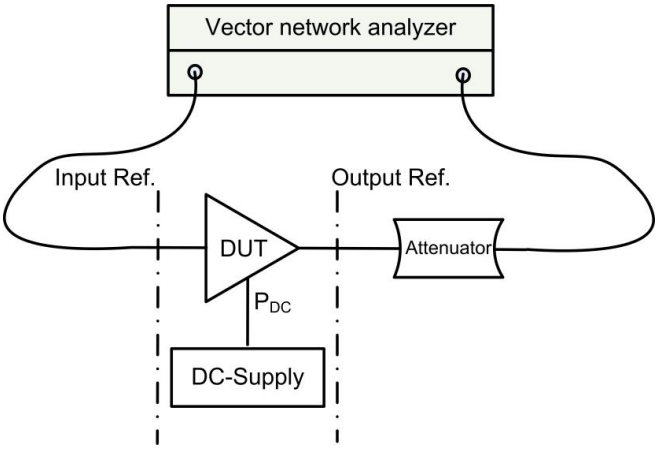


Figure 3.3: General used small-signal measurements setup in this dissertation.

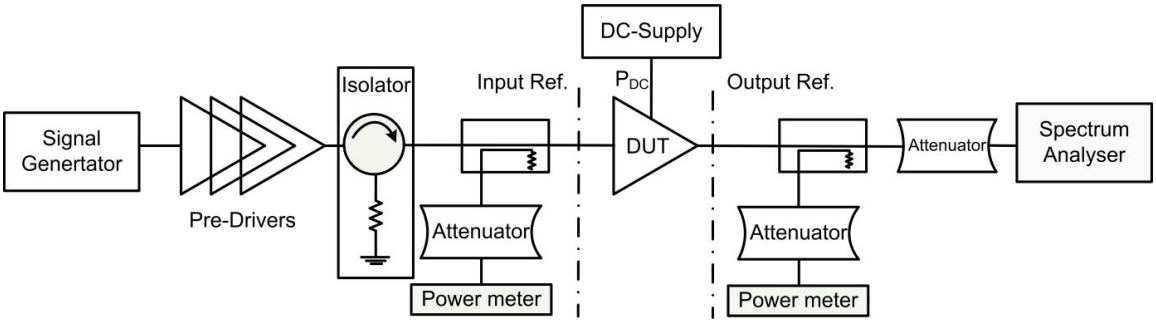


Figure 3.4: General used large-signal measurements setup in this dissertation.

3.1.4 Transistor characterization

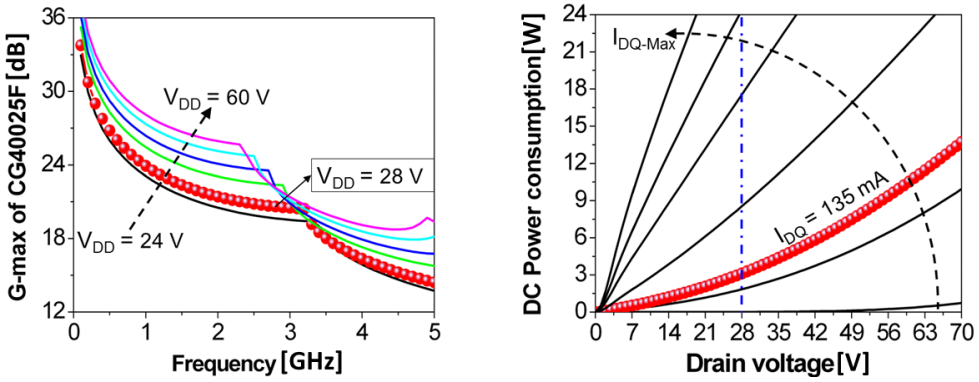
Transistor technology is the most important factor to define how efficient the device is in terms of output power, efficiency, and cost. GaN-HEMT technology was used in this dissertation, because of the positive specifications presented, as shown in Section 2.2. Commercially packaged high power devices (Wolfspeed CG40025F and CG40120F) are adopted to design all wideband power amplifiers for various purposes and different approaches in this dissertation. The most important specifications of the devices are presented in the Table 3.1.

Table 3.1: Used GaN-HEMT devices features.

Wolfspeed device	P_{SAT} [W]	C_{DS} [pF]	C_{GS} [pF]	Small-Signal Gain @ 2.0 GHz [dB]
CG40025F	30	2.6	9	15
CG40120P	120	9.1	35.3	15

Fig. 3.5 shows the maximum available gain (MAG) of CG40025F versus frequency for several drain voltages of a drain current $I_{DQ} = 125\,\text{mA}$. As shown in Fig. 3.5(a), increasing the drain voltage increases the MAG and the maximum output power ($P_{out-max}$). However, the useful frequency band was reduced. In addition, the dissipated power increases, as shown in Fig. 3.5(b). In view of these trade-offs, the appropriate chosen DC-quiescent points, which ensure high gain over the desired bandwidth with less power consumption, is $V_{DD} = 28\,\text{V}$ and

$I_{DQ} = 125$ mA. Furthermore, defining the desired bandwidth was also based on the MAG. The Miller effect of the transistor is increased by frequency. Specifically, the negative feedback from drain to gate due to the C_{DG} capacitor of the FET transistor results in decreasing the MAG of the device. At the lower frequency, the device has almost the double gain compared to the high frequency range. Choosing the bandwidth of operation is therefore limited. The device maximum available gain is reduced smoothly in the bandwidth range of 1.0 - 3.0 GHz compared to the rest of the bandwidth.



(a) (b)

Figure 3.5: (a) MAG of CG40025F at various V_{DD} and I_{DQ}=125 mA; (b) DC-power consumption versus various biasing. Red symbols refers to chosen operation point V_{DD} = 28 V & I_{DQ} = 125 mA.

The relation between the drain current and drain voltage of the device is presented in Fig. 3.6. The Figure also defines the various regions based on the main target of the design. In this dissertation, the main target is to get the best available efficiency, which is why the chosen operation point is located in the best efficiency region with the cost of linearity performance.

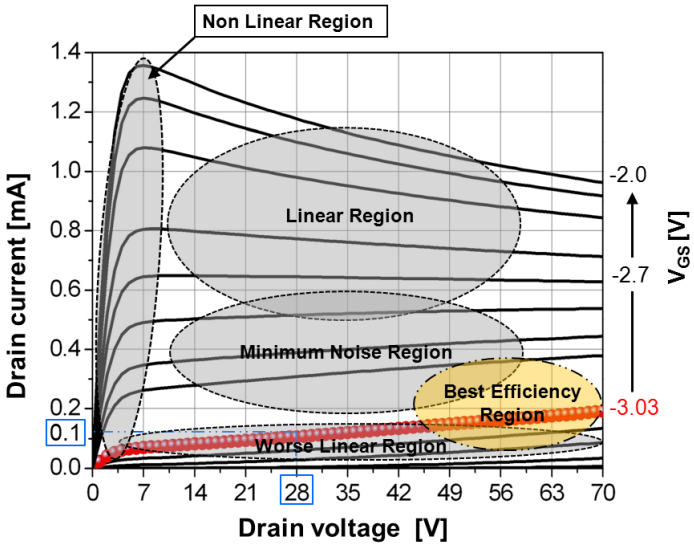


Figure 3.6: Region of operation of the GaN-HEMT devices.

3.2 25 Watt L and S band class-E PA

As already described in Chapter 2, high efficiency saturated PAs are important to obtain small and low cost transmitters for wireless communications systems. A lot of effort has been invested in reaching the highest possible efficiency performance in designing PAs. For this reason, several classes, such as class-D, class-E, class-F, class-F^{-1} and class-J have been used in most works of the state-of-the-art table, which is presented in Chapter 1, Table 1.1. The main requirement in such classes is to reduce the overlap angle between the transistor current and voltage waveforms, thus minimizing the dissipated power and ensuring the highest efficiency performance, as presented in Chapter 2.

The main aim here is to design a broadband power amplifier, operating in 1.7 - 2.3 GHz, with maximum available efficiency and a saturated output power of 25 W. CGH40025F transistor by Wolfspeed Inc. was used. The data sheet of the device, [65], presents a saturated output power of 30 W with a 62 % drain efficiency. Based on the required specifications of this design, class-E design is the best chosen class to achieve a high PAE power amplifier due to its simple structure and availability of minimum overlaps between the current and voltage curve in the time domain, as presented in Section 2.3.

To achieve the main goals of this design, many criteria were considered, including choosing the bias point of the transistor based on Section 3.1.4, impact of higher harmonics on both sides of the device (source/load), stability and DC blocks. Designing the aimed PA requires careful consideration of the parasitic influences associated with the device. More specifically, the most important parasitic is the output capacitance (C_{DS}) and the parasitic of the package. The first step in designing the PA is to determine the optimum source-/load-impedances of the nonlinear device in order to match them to the universal termination standard 50 Ω. Harmonic impedance matching is another important aspect in the design of a highly efficient PA.

3.2.1 Load-pull setup

The effect of the harmonics in source-/load-impedances on output power and efficiency was analyzed and considered during the design process to increase efficiency over the desired band. Based on [19], only up to second harmonic impedances were considered during the load-pull analysis, whereas the influence of all harmonic source impedances and third load harmonic impedance were omitted due to their minor effect compared to the complexity introduced into the design of the matching networks. The optimum source-/load-impedances were extracted as follows:

1. Extracting the optimum fundamental source-/load-impedances of the device by short-circuiting all harmonics, where the device operates as class-B with an efficiency up to 78 %, as presented in Chapter 2.

2. Determining the second harmonic source-/load-impendence influences on the efficiency by fixing the extracted fundamental source-/load-impedances. The second harmonic source impedance has less influence compared to the second harmonic load impedance impact, as shown in Fig. 3.7(a), (b) respectively. The Figure illustrates the PAE versus

the second harmonic source phase sweep at unity magnitude in Fig. 3.7(a), whereas Fig. 3.7(b) shows the influence of second harmonic load phase sweep at various magnitudes. The Figure illustrates the PAE versus the phase variation of second harmonic and magnitude at the center frequency (2.0 GHz). It is noticed that the PAE was rather independent of the second harmonic phase with the exception of the region (170° - 300°). In this region, the efficiency performance of the active device was dramatically degraded. However, the magnitude influence of the second harmonic reflection coefficient, which is illustrated in the same figure, had less influence on the performance of the PA than the phase of the reflection coefficient. Nevertheless, the third load harmonic phase influence is checked across the desired frequency band in Fig. 3.7(c), and it can be concluded that it has a minor influence on the PA performance. Consequently, Fig. 3.8 illustrates the drain efficiency variation by reforming the second harmonics load impedances contours at center frequency 2.0 GHz, whereas the third harmonic was adjusted as an open circuit at this analysis. The Figure shows that the maximum range of the drain efficiency was located at the border of the Smith chart, where the magnitude of the reflection coefficient (Γ_{2f0}) was unity and the phase ranged between 170°- 300°. To sum up, by maintaining a high magnitude of the second harmonic load reflection coefficient and simultaneously avoiding operation at critical phase zones, near short-circuit termination, will result in high efficiency performance of the PA over the desired bandwidth.

3. Post-optimizing the fundamental load impedance further by fixing the extracted fundamental source impedance value and the second harmonic load impedances at the optimum range. The efficiency performance can be improved by up to 10 % compared to the first step alone, using the steps mentioned above. This analysis has been performed for every single frequency across the desired band. The extracted optimum source-/load-impedances are presented in Fig. 3.10.

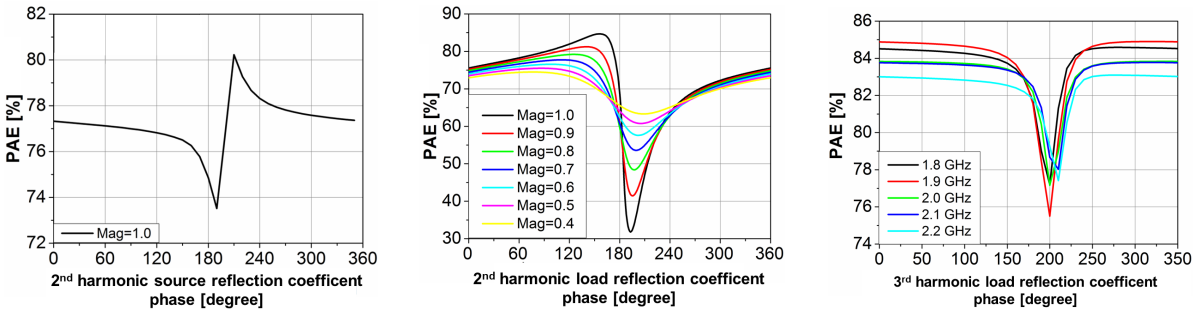


Figure 3.7: (a) Second harmonic source impedance impact; (b) second harmonic load impedance influences at various magnitude; (c) third harmonic load impact with unity magnitude @ 2.0 GHz.

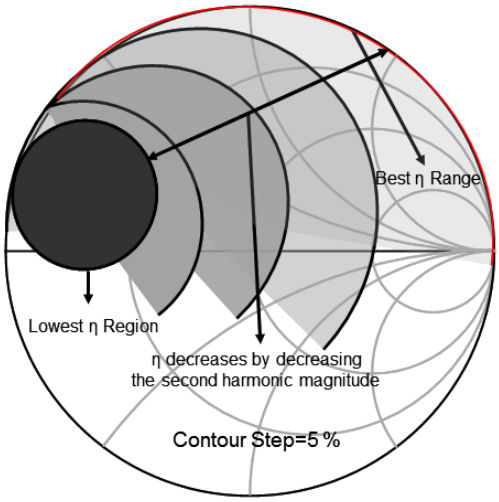


Figure 3.8: Simulated load-pull contours of the second harmonic impedance at center frequency $f_0 = 2.0$ GHz.

The drain side of the transistor can be approximated by an ideal current source with a parallel RC circuit, where the resistor presents the source resistance corresponding to the PA load line (R_{DS}), and the capacitor presents a total drain-source capacitance (C_{DS}), whereas the gate side of the device can be approximated by a voltage source with a series R_{GS}- C_{GS} network across the desired bandwidth, as shown in Fig. 3.9. This method simplifies the chosen matching network topology. The aim of the matching network is to resonate out the transistor input-/output-capacitances over the bandwidth. The active device's internal current source will then see approximately a purely resistive impedance equal over the bandwidth, thus producing a wideband PA frequency response.

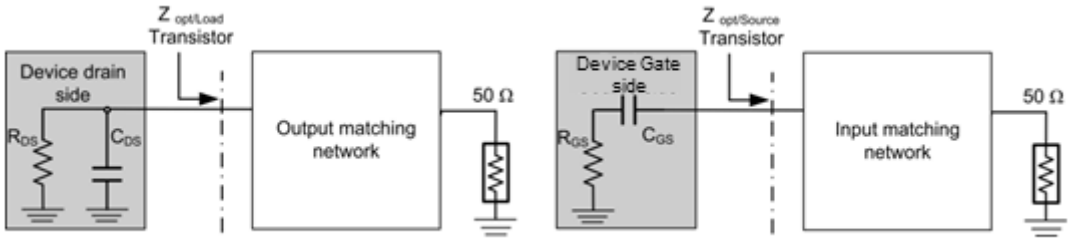


Figure 3.9: Simplifying the optimum source-/load-impedances of the transistor across the desired bandwidth.

3.2.2 Matching network realization

To design the input and output matching network, a lossless with high return loss and low loaded Q matching network (MN) is required. Chebyshev low-pass filter is the most efficient filter used to design such MNs. The optimum packaged source impedances of the

device across the desired bandwidth are shown in Fig. 3.10. The real part of the optimum source impedance is varied between 1.8 to 3.0 Ω, and the imaginary part is also varied slightly between -2.0 to 2.0 Ω. The task of the input matching network (IMN) is to transform the 2.5 Ω (middle value of the real part optimum source impedance) to 50 Ω (20:1) with low transmission loss, and high return loss. For this purpose, a two stage L-type network was used. The ideal (input matching network) IMN was converted to transmission lines TL_i, i= 1...5 , as shown in Fig. 3.11, which was post-optimized to provide the extracted optimum source impedance at the input of the device. Fig. 3.10, the identified circle, shows the realized reflection coefficient response (symbols) of the IMN, fulfilling the optimum source impedance (solid line).

An important factor regarding the design of the IMN was to obtain an unconditionally stable transistor operation which is represented by a stability factor larger than unity over the whole frequency spectrum. For this purpose, the IMN has been slightly modified in order to stabilize the PA without causing a degradation of the gain across the bandwidth. A series resistor R_{s1} was therefore added at the input of the amplifier and bypassed by a capacitor C_{s1} to ensure an unconditionally stable design. Further improvement in the PA stability at the low frequency band can be achieved by reducing the gain at this band. Thus, an additional shunt RC network (R_{s2} series with C_{s2}) and a resistor R_g were added in order to increase the low frequency stability, as shown in Fig. 3.11.

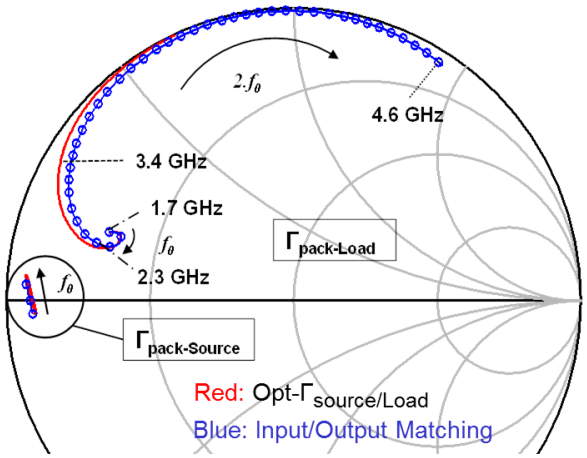
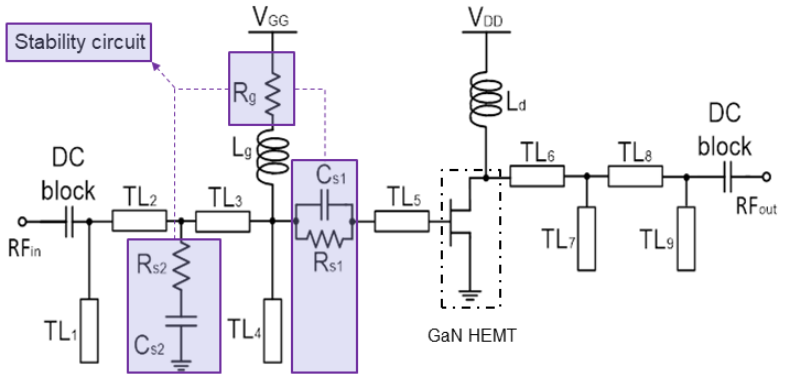


Figure 3.10: Optimum fundamental source-/load- and 2^{nd} harmonic load reflection coefficient of the OMN over 1.7 - 4.6 GHz (red solid), realized coefficient simulations (blue symbols).

The main goal of the output matching network (OMN) is to transform the extracted optimum fundamental and second harmonic load impedances, shown in Fig. 3.10 (solid lines), to 50 Ω across the bandwidth. The OMN consists of a two-stage low-pass filter. The synthesized ideal network was realized using TL_i, i=6...9. In this design, the inductors were replaced by high-impedance transmission lines TL_2, TL_3, TL_6, and TL_8, while the capacitors were realized by low-impedance TL_1, TL_4, TL_7, and TL_9, as shown in Fig. 3.11. The reflection

coefficient of the realized network (symbols) was matched to the optimum packaged load impedances (solid lines) as shown in Fig. 3.10. In both input-/output-MNs, the first open stubs TL_4, and TL_7, which are close to the device gate-/drain-terminations respectively, were clearly wide in order to compensate the parasitic effects of C_{GS} and C_{DS} of the device respectively. Fig. 3.11 shows the complete schematic of the whole design involving the input-/output-matching networks with the stability circuit and DC networks.



Line	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7	TL_8	TL_9
Length [mm]	14.1	6.7	8.1	12.0	1.0	5.5	13	23.2	2.5
Width [mm]	0.9	1.2	4.0	3.5	2.0	1.45	4.0	2.7	0.2

Figure 3.11: Circuit topology the designed PA; lines dimensions of the circuit.

3.2.3 Transistor de-embedding method

In order to study the waveforms of the voltage and current at the intrinsic drain plane, the package of the device and the C_{DS} were de-embedded using ADS tool, where the die transistor sees purely resistive impedances across the desired bandwidth.

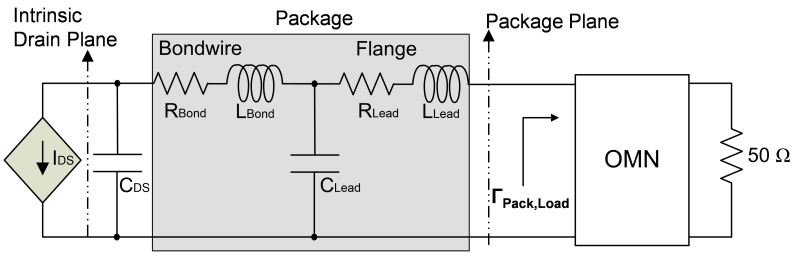


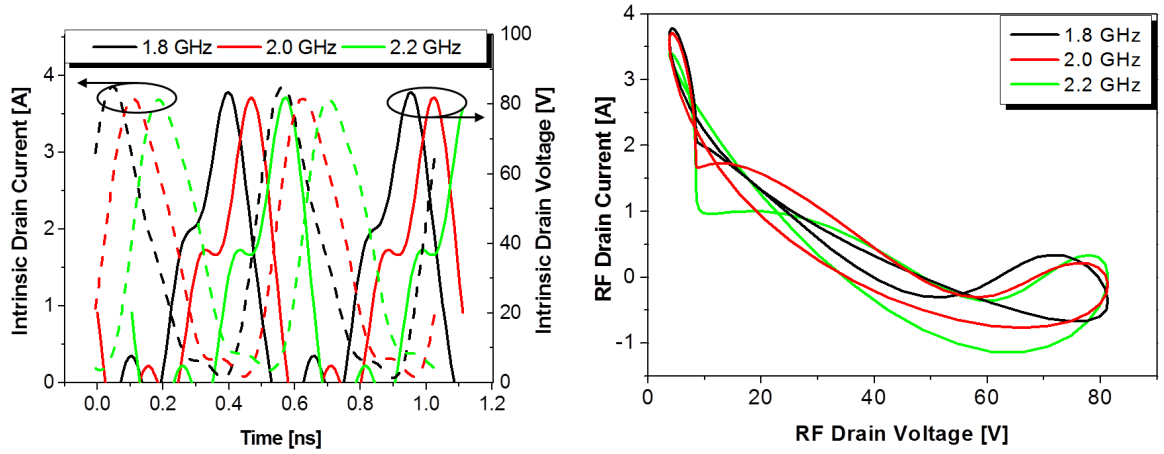
Figure 3.12: Block diagram of the output side of the device with equivalent circuit illustrating the parasitic elements for negative image de-embedding technique.

Fig. 3.12 shows the equivalent circuit of the drain source capacitance, bondwires, and the flange which was normalized to 30 Ω of the selected device. Moreover, Table 3.2 presents the absolute value of the de-embedded equivalent circuit.

Table 3.2: Values of the de-embedded components.

Component	C_{DS} [pF]	L_{Bond} [PH]	R_{Bond} [Ω]	C_{lead} [PF]	L_{lead}[pH]	R_{lead} [Ω]
Value	2.5	146	0.17	0.96	10	0.68

The waveforms are shown in Fig. 3.13 and correspond to the simulated PAE at three frequencies (1.8, 2.0, and 2.3 GHz) of the desired band. The investigation of the waveforms confirms that the voltage/current overlap is minimized and thus, results in high efficiency operation across the band.



(a) (b)

Figure 3.13: (a) De-embedded intrinsic drain waveform of the RF-drain current and voltage from ADS simulation at various frequencies with PAE of 77 %; (b) RF-load line curve at various frequencies.

3.2.4 Experimental characterization

The PA was implemented on a Rogers 4003c substrate with ε_r of 3.55 and a thickness of 0.508 mm. Fig. 3.14 shows the prototype of the design which has a size of 4 cm × 8 cm. It includes the biasing circuit, DC-blocks, input-/output-matching network, as well as a stability circuit. The implemented broadband PA has been characterized by small-, large-, and modulated-signal measurements to evaluate its performance. The setup of measurement has therefore been prepared based on the presented approach in Section 3.1.3 for small-/large-signal measurement characterization. Preliminary experimental results showed a good agreement with the simulated data over the design band.

- **Small-Signal performance**

Fig. 3.15 shows the comparison between the simulated and measured small-signal gain and the return loss of the fabricated PA. The measured return loss was in agreement with the simulated results $S_{11} \leq$ -10 dB across the bandwidth. The measured gain of the designed PA was subsequent to the simulated gain with a minimum value of 15 dB over the 1.75 - 2.25 GHz band.

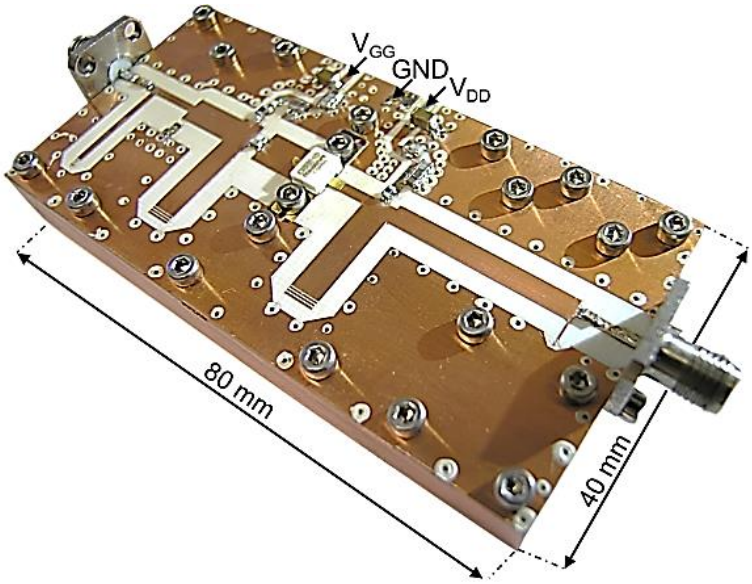


Figure 3.14: Prototype of the fabricated PA.

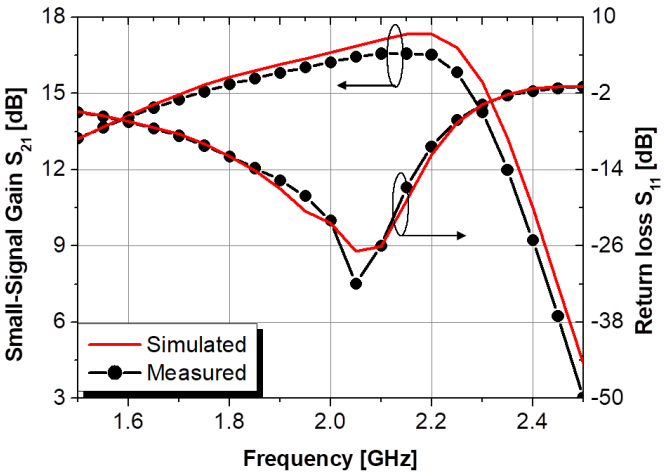


Figure 3.15: Small-Signal gain and return loss of the realized PA; simulated (solid lines) and measured (symbols) at V_{DD} = 36 V, I_{DQ} = 135 mA.

- **Large-Signal performance**

The measurements were performed at drain bias voltage of 36 V with I_{DS} of 135 mA. Fig. 3.16(a) reports the comparison between simulated and measured output power and drain efficiency versus frequency. The Figure illustrates a saturated output power ranging from 43.5 dBm to 45 dBm across 1.7 - 2.3 GHz (44.5 - 45 dBm across 1.7 - 2.2 GHz), with an obtained minimum drain efficiency of 73 %. Fig. 3.16(b) shows the large-signal gain as well as the PAE performance at various frequency points in the desired band. The saturated PAE ranged between 70 % - 76 % at 3 dB compression point, whereas the large-signal gain was almost 12 dB across the band.

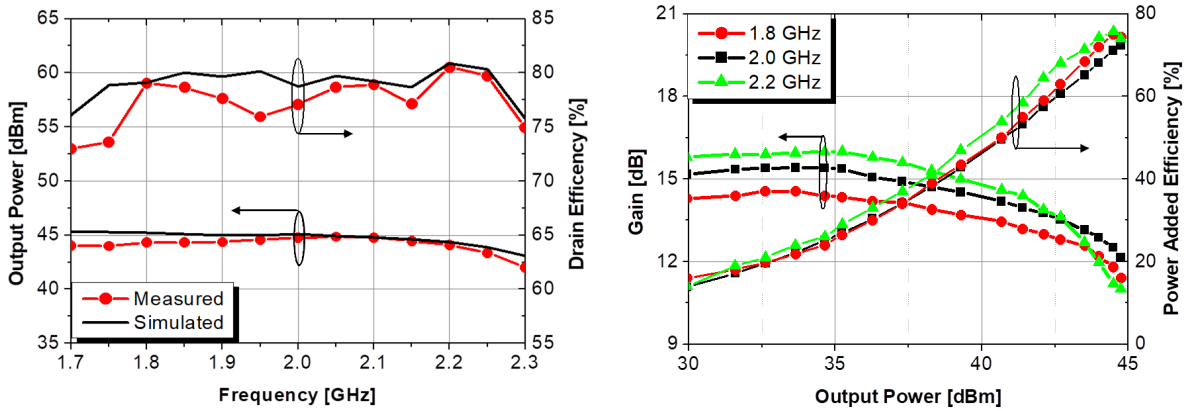


Figure 3.16: (a) Comparison between simulated (solid lines) and measured (symbols) output power and drain efficiency across the bandwidth at V_{DD} = 36 V, I_{DQ} = 135 mA @ 3dB compression point; (b) measured large-signal gain and power-added efficiency performance versus the output power sweep at V_{DD}= 36 V, I_{DQ}= 135 mA at various frequencies 1.8, 2.0, and 2.2 GHz.

Fig. 3.17 illustrates the measured output power, gain, and efficiency with respect to the input power at 1.8, 2.1, and 2.2 GHz. The gain compression point was around 33 dBm input power, while the average drain efficiency was 73 %.

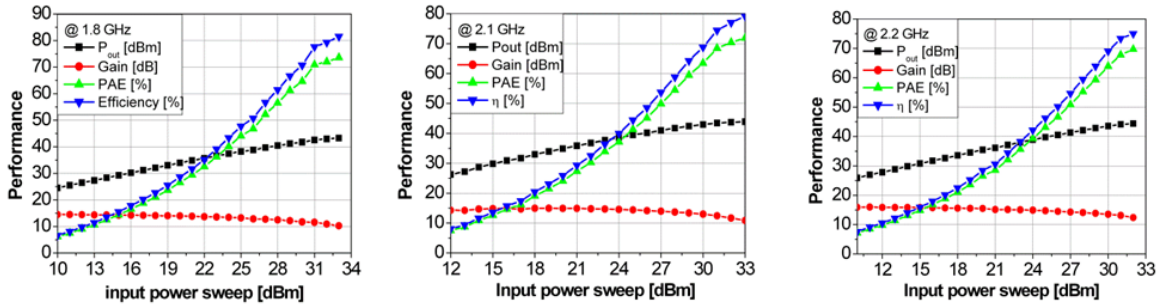


Figure 3.17: Measured performance @ 1.8, 2.1 and 2.2 GHz .

The drain efficiency and PAE were evaluated at 6 dB output back-off power (OBO) for the modern wireless communication standards, as shown in Fig. 3.18. The average drain efficiency was 42 % with a 40 % PAE across the whole bandwidth, which proves that this design can also be used for the modern wireless communication standards, due to the high efficiency at OBO level.

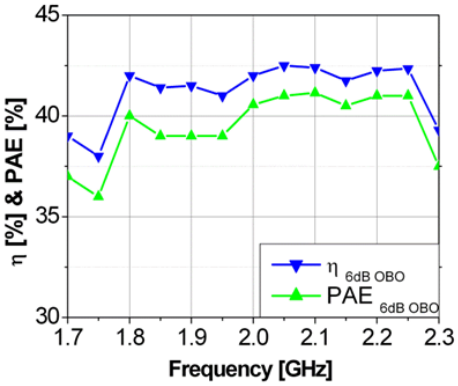


Figure 3.18: Measured drain efficiency and PAE @ 6dB OBO.

- **Linearity measurement**

In order to evaluate the inherent linearity, a 10 MHz long term evolution (LTE) signal with 7.3 dB peak to average power ratio (PAPR) was used at a center frequency of 1.8 GHz. The measurements were performed using a predistortion in the RF domain (RFPD). The main concept of this system is presented in [66]. Table 3.3 summarizes the average performance of output power and the PAE from this measurement. The measured output spectrum, before and after linearization of the LTE signal is shown in Fig. 3.19. These results prove that RFPD can be used to sufficiently linearize the PA to meet the standards of modern wireless communication systems.

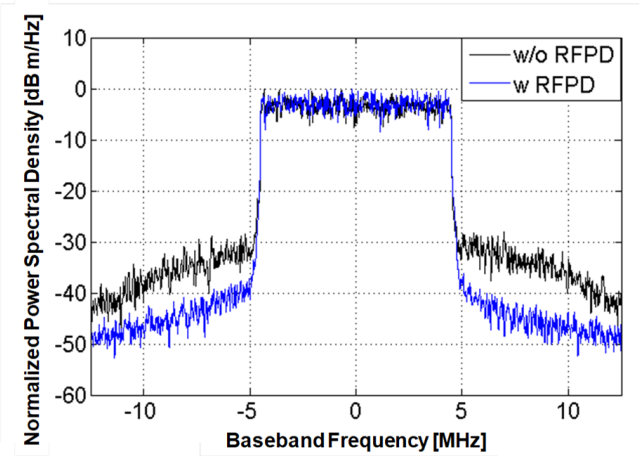


Figure 3.19: Measured output spectrum of a 10 MHz LTE signal @ 1.8 GHz before and after linearization using RFPD.

Table 3.3: Average of output power, PAE and ACLR @ 1.8 GHz for 10 MHz LTE signal.

	Pout [dBm]		PAE [%]		ACLR [dBc]	
LTE @ 1.8 GHz	W/O	W	W/O	W	W/O	W
	33.36	35.58	35.9	38.2	-34.1	-44

The summary of the desired power amplifier is presented in the Table 3.4. The minimum measured output power was 44 dBm with 11 dB gain and 73 % efficiency.

Table 3.4: Summary of 25 Watt L and S band class-E PA performance.

f [GHz]	P_{Out} [dBm]	Gain [dB]	Efficiency [%]
1.7	44	11	73
1.8	44.2	11.5	78
1.9	44.8	11.75	77.5
2.0	45	12	77.5
2.1	44.5	11.75	79
2.2	44	11.5	80.5
2.3	43.5	11	75

3.3 20 Watt harmonically tuned PA with 84 % bandwidth

Based on the achieved results in the previous design, the potential of extending the bandwidth to cover additional wireless communication standards has been increased. Section 3.1.4 presents the characterization results of the nonlinear device used, and it is concluded that the transistor bandwidth has a maximum available gain of more than 12 dB and up to 3.0 GHz.

The main aim here is to utilize the characterization of transistor advantages to design a highly efficient ultra-wideband power amplifier operating in the frequency range 1.1 – 2.7 GHz with a minimum output power of 20 W and large-signal gain of more than 10 dB. In-band harmonics occur due to the design's ultra-wideband operation. Despite this, the harmonics in this design are perfectly matched. This is in order to ensure that the performance is highly efficient. The design being introduced here is called a Harmonically tuned power amplifier (HTPA).

In comparison to the state-of-the-art results, there are several other broadband PAs operating within the same bandwidth range, as illustrated in Table 1.1, However, these operate either with an output power level of 10 W with high power-added efficiency (PAE) [12], or with a narrower bandwidth and a similar PAE [Paper A]. According to [12] and [Paper A], both methodologies were developed together to obtain the maximum available PAE with a minimum saturated output power of 20 W over 1.1 - 2.7 GHz bandwidth in accordance with Bode-Fano criteria [67]. This design achieves a state-of-the-art performance compared to recently published results, as shown in Table 1.1. It particularly exhibits the highest broadband efficiency with a distributed matching network structure reported so far.

3.3.1 Extracting approach of optimum source-/load-impedances

Designing the intended HTPA requires careful consideration of the influence of the harmonics, which are located in-band for some frequencies, as shown in Fig. 3.20. An individual impedance termination analysis for each harmonic of the targeted frequency band has therefore been carried out. The same characterized reliable model of CGH40025F in Section 3.1.4 by Wolfspeed has been used [65]. Essentially, the extraction of the optimum source-/load-impedances of the device over the whole bandwidth was carried out through the steps presented in Section 3.2.1. Moreover, an additional step has been used in this design to overcome the in-band problem. An adapted method has been used to reduce the influence of the second in-band harmonic impedance and called adapted harmonically ultra-wideband power amplifier approach. Generally, by decreasing the frequency, the maximum available gain of FET devices increases. Utilizing this fact, the desired bandwidth was split into two sub-bands for extraction of optimum load impedances, as shown in Fig. 3.20.

1. Lower sub-band F_{L0} = [1.1 - 1.4] GHz.
2. Higher sub-band F_{H0} = [1.5 - 2.8] GHz.

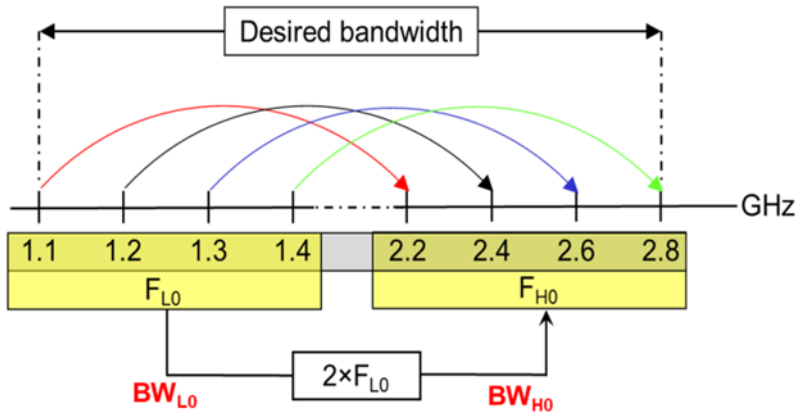


Figure 3.20: Presenting the bandwidth of the desired PA including the in-band harmonics.

- **For Lower sub-band:**

The optimum load impedances (Z_{opt}) of the low F_{L0} band have been slightly modified and called Z_{M-opt}. This results in ~0.5 to 1 dBm less power delivered towards the load with improved PAE, as shown in Fig. 3.21(a). This approach expands the safe region of the second harmonic impedance. In other words, reducing the magnitude and sweeping the phase of the second harmonic load impedance at Z_{M-opt} has less impact on the maximum available PAE of the PA in the range of 58 % - 75 % compared to Z_{opt}. This is why any tolerance during production or any overlap in fundamental and second harmonic impedances cannot cause a strong deviation in the total PA performance.

- **For higher sub-band:**

The optimum load impedances (Z_{opt}) of the high frequency band F_{H0} have not been modified, and the second harmonic impedance is defined based on Section 3.2.1 by maintaining a high magnitude of the second harmonic load reflection coefficient. Simultaneously, avoiding operating at critical phase zones, near short-circuit termination, results in highly efficient performance of the PA over the desired bandwidth, as presented in [Paper A].

This technique has solved the main problem of overlapping between the harmonics and the fundamental optimum load impedances in-band. The final extracted optimum load impedances across the desired bandwidth are shown in Fig. 3.21(b).

3.3.2 Matching network realization

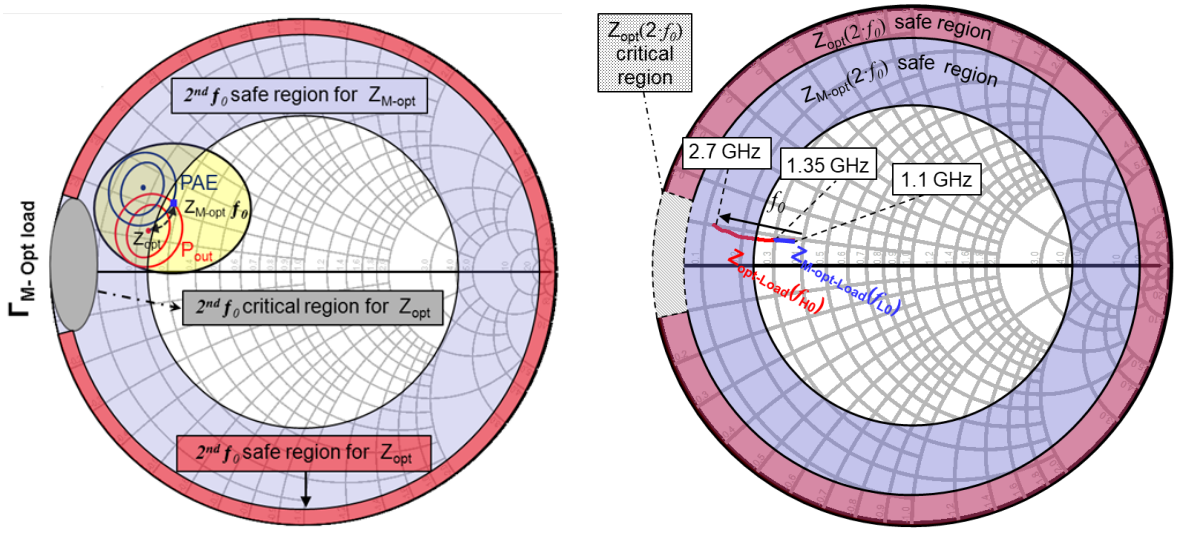
The design of the input-/output-matching networks was accomplished in three steps to minimize the deviation between the simulation, momentum and measurement results:

- Calculating the inverse of the conjugate value of the optimum load impedance, a load line of 18.35 Ω and a transistor output capacitance of 2.65 pF can be estimated. The output matching network (OMN) should be designed to match the estimated optimum

load impedance, as shown in Fig. 3.21(b), to 50 Ω across the 1.1 – 2.7 GHz bandwidth.

- Chebyshev has been chosen to match the optimum source-/load-impedances, because it presents a good response with less order compared to Butterworth or Bessel filters. Nevertheless, the high order of the filter results in higher complexity, coupling, and more deviation between the simulated and measured results.
- The order of the Chebyshev filter was reduced with a lossless network. A simpler filter can be therefore used ensuring a reliable response.

Fig. 3.22 presents the ideal, realized OMN, where the inductors have been replaced with high impedance transmission lines TL_1, TL_4, TL_5. The capacitors were realized by low-impedance TL_2, TL_3. During this conversion, the topology was simplified as shown in realized OMN. The Figure also presents the simulated and measured reflection coefficient of the OMN up to the maximum second harmonic frequency of 5.4 GHz. The second harmonic load reflection coefficient has a minimum magnitude of 0.5 in the simulation which is located in the expanded safe region of the transistor after modifying Z_{opt}.



(a) (b)

Figure 3.21: (a) Adapted $\Gamma_{M-Opt-load}$ related to the max. P_{Out} and PAE at 1.1 GHz, safe and critical regions of the second harmonic impedance; (b) optimum fundamental load impedances ($Z_{M-opt-load}$) (blue solid lines), ($Z_{opt-load}$) (red solid lines) over 1.1 - 2.7 GHz, safe and critical regions of 2^{nd} harmonic load impedance for ($Z_{opt-load}$) and ($Z_{M-opt-load}$), red and blue regions respectively.

Moreover, Fig. 3.23 presents the transmission and the reflection results of the S-parameter for the simulated (schematic, momentum) and realized OMN. The SMA connector was de-embedded before comparing results. The Figure presents a perfect agreement between the schematic and the momentum simulation results, while the agreement with the fabricated filter has slightly deviated at only high frequency range. This deviation in insertion loss was observed at 2.2 GHz and was increased by increasing the frequency, due to the combination of

less reflection coefficient in the ports of the OMN up 2.1 GHz compared to the low frequency range.

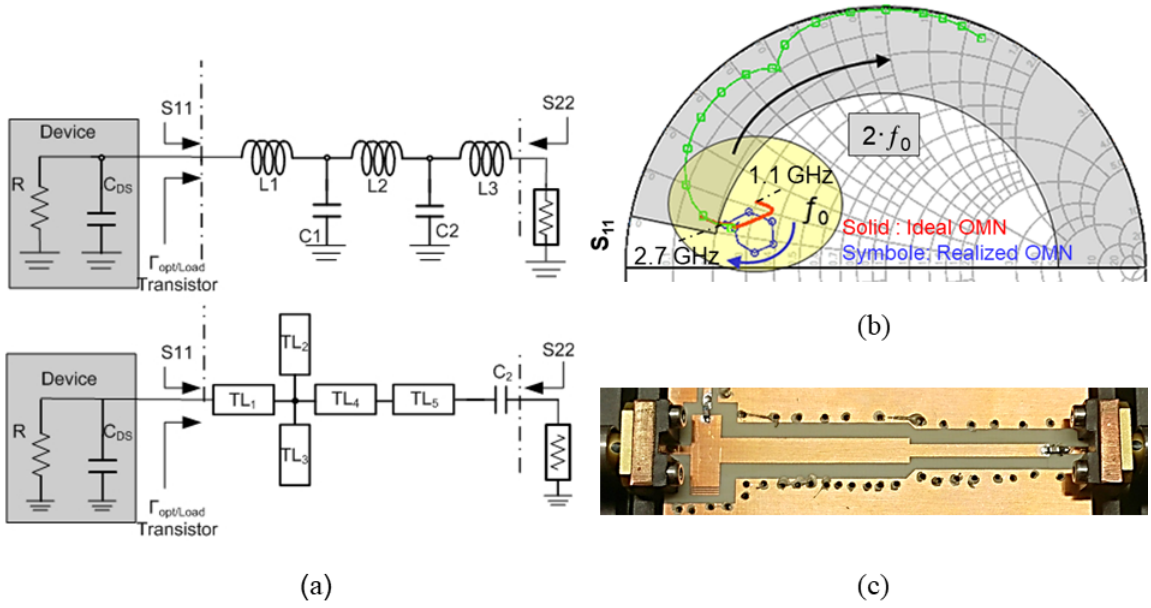


Figure 3.22: (a) Equivalent circuit of the transistor with the ideal-/real-matching network; (b) ideal fundamental OMN (red solid lines), realized matching fundamental (blue symbols) and second harmonic realized matching curves (green symbols); (C) prototype of the fabricated OMN.

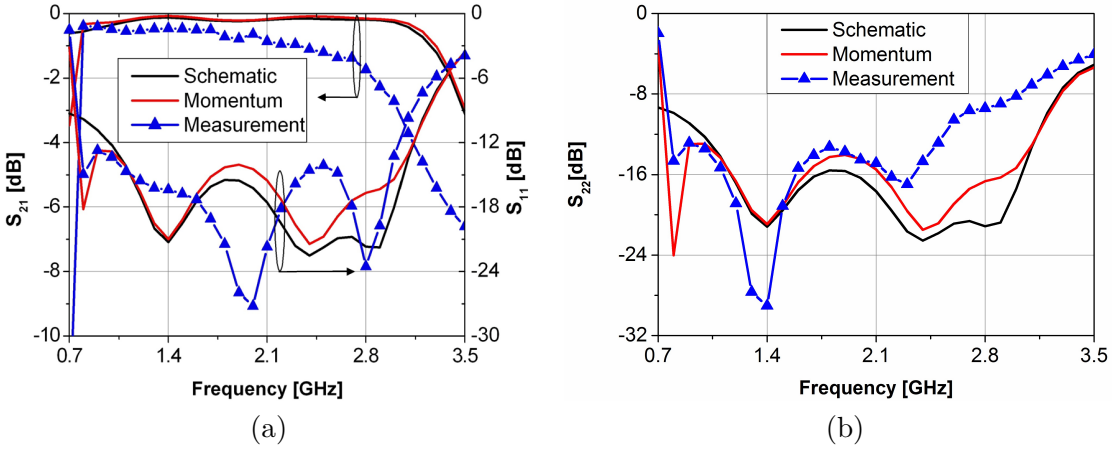
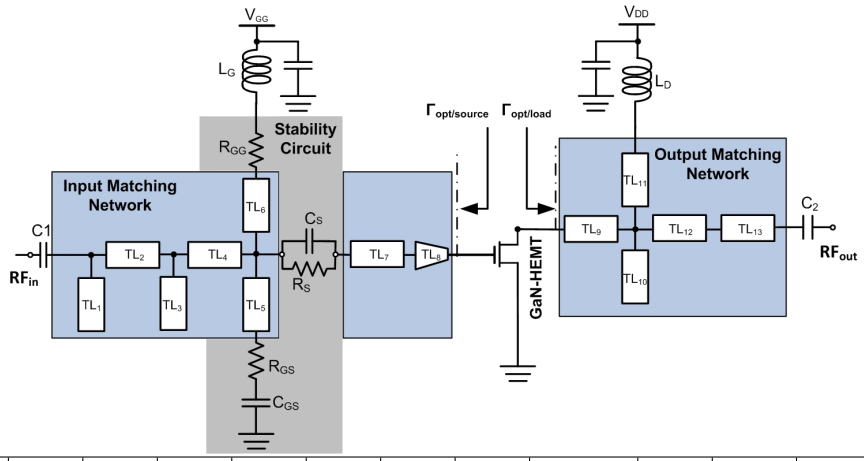


Figure 3.23: (a) Simulation, momentum, measurements comparison of output matching network through (S_{21}) and return loss (S_{11}); (b) return loss of (S_{22}).

An analogous procedure has been used for the input matching network (IMN). A stability circuit composed by a capacitor $C_S = 5.6$ pF and a resistor $R_{GS} = 39\ \Omega$ in parallel should be included, resulting in some extra losses in the input matching filter. The final schematic of the design, including the input-/output-matching, stability and biasing circuits, is presented in the Fig. 3.24.

To verify the designed PA, the final circuit has been implemented twice on a Rogers 4003c

substrate with ε_r of 3.55, and thickness of 0.508 mm. The first one was fabricated to measure the through and reflection coefficient of the total circuit, including the IMN, stability circuit and the OMN without the active device.



Line	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7	TL_8	TL_9	TL_{10}	TL_{11}	TL_{12}	TL_{13}
Length [mm]	5.8	10.3	10.8	16.3	3.3	3.3	6.3	2.5	4.5	5.5	5.3	29.5	19.5
Width [mm]	2.0	1.4	2.0	3.3	4.0	4.0	7.0	7 to 1.5	1.5	4.5	4.5	4.0	2.0

Figure 3.24: Circuit topology the designed PA; lines dimensions of the circuit.

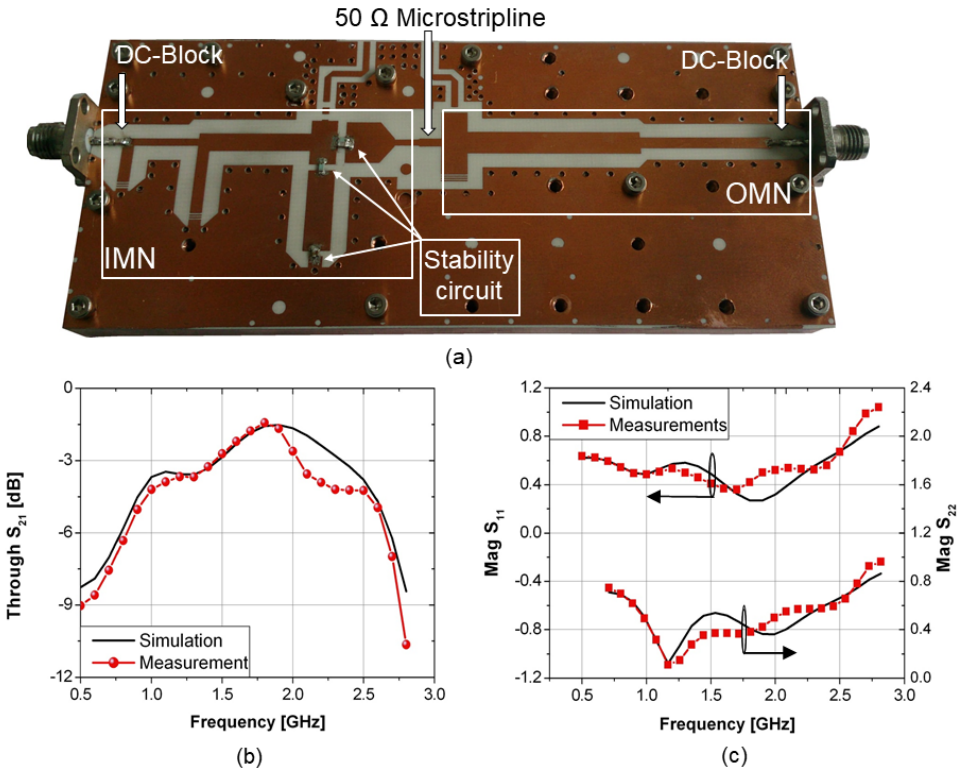


Figure 3.25: (a) Prototype of the through fabricated design; (b) and (c) simulation measurement comparison of through and Mag S_{11}, S_{22}.

Instead of using the transistor, a 50 Ω microstrip line was used as shown in Fig. 3.25. The comparative results are shown in Fig. 3.25. The through measurement result (S_{21}) has a good agreement across the bandwidth. However, a small deviation has been observed at high frequency range 2.0 - 2.4 GHz between the simulated and measured circuit, due to the output matching deviation. The other one was implemented with the CGH40025F transistor and same substrate. Fig. 3.26 shows the prototype of the design, including biasing, stability, input and output matching network circuits.

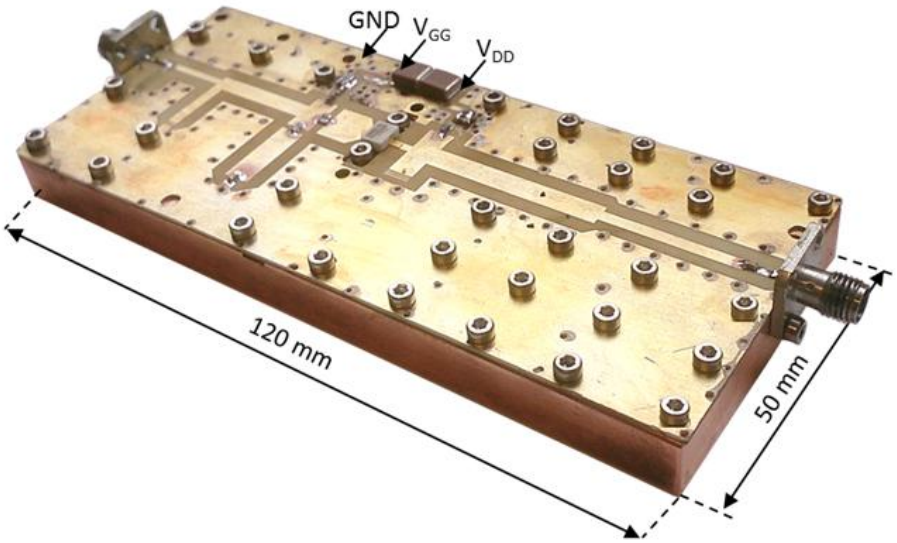


Figure 3.26: Prototype of the fabricated PA.

3.3.3 Experimental characterization

The designed PA has been characterized through small-/ large-signal measurements to evaluate its performance. Measurements were performed at drain bias voltage of 28 V with I_{DS} of 135 mA. Preliminary experimental results showed good agreement with the simulated results over the design band.

- **Small-Signal performance**

The MAG of the prototype was evaluated after measuring the small-signal gain of the PA and compared to the MAG of the simulated PA and the device to verify the simulated PA, as shown in Fig. 3.27. A comparison between the simulated and measured small-signal gain is presented in Fig. 3.28, as well as the return loss of the fabricated PA. The measured return loss was in agreement with the simulated gain with a minimum value of 12 dB over the 1.1 - 2.7 GHz.

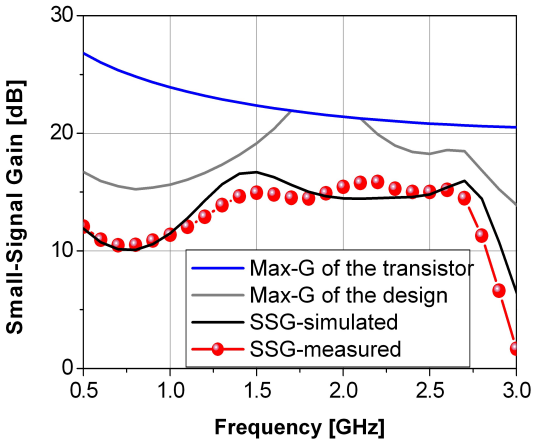


Figure 3.27: Comparison between simulated and measured MAG of the PA (blue, gray solid line respectively); simulated and measured small-signal gain of the PA (black solid line and red symbols respectively).

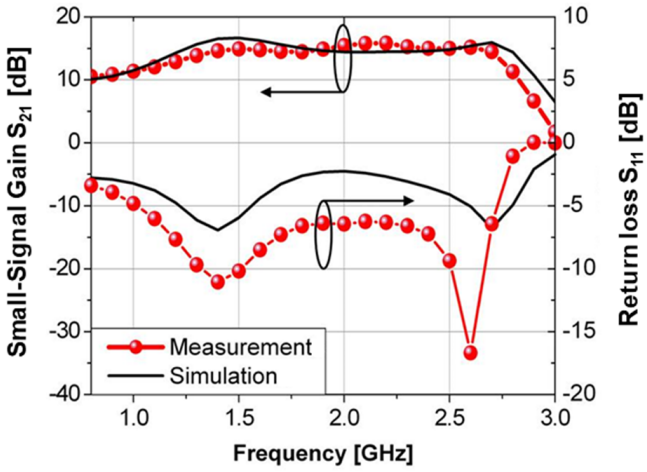


Figure 3.28: Comparison of small-signal gain and return loss of the realized PA at $V_{DD} = 28\,V$, $I_{DQ} = 135\,mA$.

- **Large-Signal performance**

Large-Signal measurements were performed based on the large-signal setup which is presented in Section 3.1.3. A continuous wave (CW) input signal was generated by a microwave generator (Agilent E4438C), boosted by a microwave driver amplifier from Mini-Circuits Inc., and the output relevant power was measured by a calibrated power meter (Agilent N1912A). Fig. 3.29 presents a comparison between the simulated and measured output power and the drain efficiency as a function of the frequency. The measured results were in good agreement with the simulation. A saturated output power ranging from 43 dBm to 45 dBm across 1.1 - 2.7 GHz with a minimum drain efficiency of 65 % was obtained. Moreover, a saturated PAE between 59 % - 72 % at 3 dB compression was measured and the large-signal gain was 10.5 ±1 dB across the band.

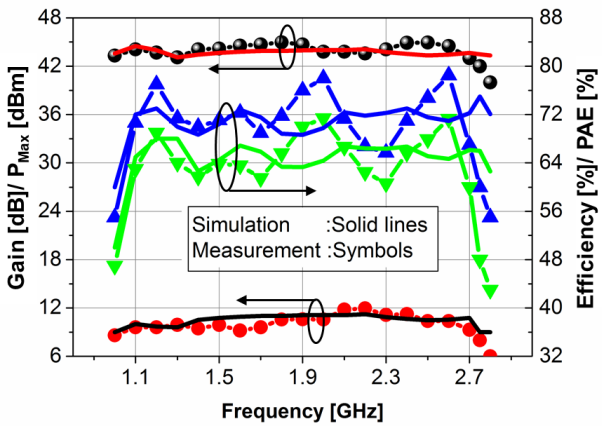


Figure 3.29: Comparison between simulated (solid lines) and measured (symbols) maximum output power, gain, drain efficiency and power-added efficiency across the bandwidth at V_{DD} = 28 V, I_{DQ} = 135 mA.

Finally, Fig. 3.30 illustrates the measured output power, gain, and efficiency with respect to the input power. The input power was varied from 0 dBm to 35 dBm with 1 dB step and at 1.1, 1.9, and 2.7 GHz. The gain compression point was around 34 dBm input power, while the average drain efficiency was 66 %.

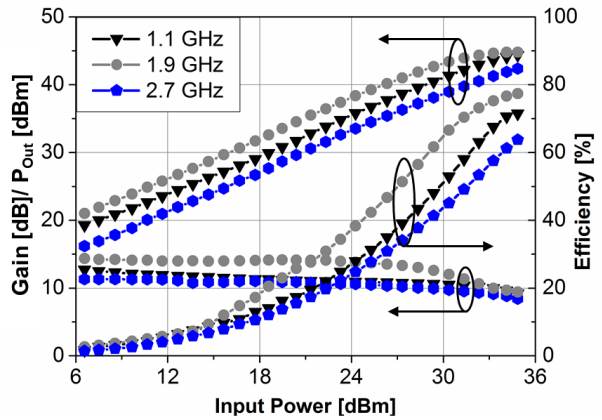


Figure 3.30: Measured power amplifier performance across the input power at various frequencies 1.1, 1.9 and 2.7 GHz, V_{DD}= 28 V, I_{DQ}= 135 mA.

Table 3.5 summarizes the performance of the 20 Watt ultra-wideband PA over the design band.

Table 3.5: Summary of ultra-wideband highly efficient 20 Watt harmonically tuned PA performance.

f [GHz]	P_{Out} [dBm]	Gain [dB]	Efficiency [%]
1.1	44.5	10	70
1.3	43	10.7	70.5
1.5	44.5	10.6	71.5
1.7	45	10.5	69
1.9	45	11.4	76
2.1	43.2	11.7	71.5
2.3	43.7	11.6	66
2.5	45	11	74
2.7	42.5	9.5	67

3.4 Multi-Octave 20 Watt PA using planar transmission line transformer

The main aim here is to design highly efficient multi-octave bandwidth PA with a 20 W output power. The desired design frequency band ranges between 0.5 to 2.7 GHz. This band covers all modern mobile communication standards and a higher band of digital video broadcasting-terrestrial (DVB-T). However, the in-band problem is the most critical issue in these designs, as shown in Fig. 3.31. A harmonic matching concept is presented in connection with a simple implementation approach. The fundamental load impedances of the low frequencies are slightly de-tuned out of their optimum values to reduce the in-band harmonics influence in output power and power-added efficiency, as done in [Paper B]. Furthermore, a broadside coupled transformer is used for the first time as a key-element of the matching network. This takes advantage of the ultra-wideband impedance transforming characteristics. Combining both concepts results in ultra-wideband matching circuits that are easy in realization and low-loss at the same time.

The bandwidth is split into three bands, low frequency band (F_{L0}), middle frequency band (F_{M0}) and high frequency band (F_{H0}). Up to 4^{th} harmonic is located in-band of operation of the desired PA for the low frequency band. Therefore, the extracted optimum load impedances are critical and should be carefully defined to reduce the influences of the in-band problem.

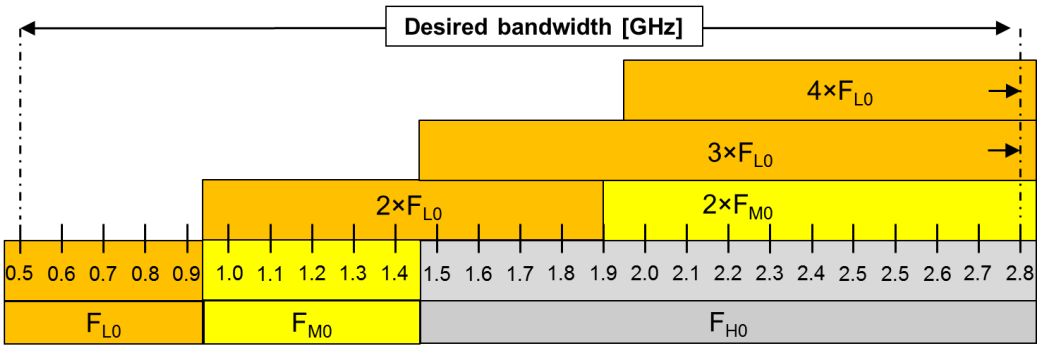


Figure 3.31: In-band problem for designing multi-octave power amplifier.

A 25 W packaged transistor by Wolfspeed has also been implemented. The optimum source-/load-impedances were extracted based on the provided large-signal module of the transistor from Wolfspeed Inc. The minimum output power of this amplifier was 43 dBm with very high efficiency over the whole bandwidth. In this design, the planar broadside coupler has been used on the outside of the matching network. The biasing has been chosen based on the study in Section 3.1.4 with a V_{DD}= 28 V and drain bias current of 135 mA. The fractional bandwidth of this design is 137.5 % at 1.6 GHz. It is more than the fractional bandwidth designed in Section 3.3 (84.2 % at 1.9 GHz), thus resulting in additional complexity in the matching network design.

3.4.1 Extracting approach of source-/load-impedances

The optimum source-/load-impedances contours for individual fundamental frequencies (f_0) can be obtained using a source-/load-pull technique for the PAE and P_{out} across the desired band. However, the current harmonic matching techniques are limited in bandwidth. Generally, the influence of harmonics can be reduced by forcing the harmonics load impedances (Z_{opt}), at their frequencies, to lie close to the border of the Smith chart. as presented in Section 3.2.1.

Fig. 3.32 shows the simulated optimum load impedance locus "Z_{opt} (f_0) region" and the phase of Z_{opt} for the second harmonic at 0.6 GHz for a reflection coefficient magnitude $|\Gamma| = 1$. It can be seen that the PAE was practically independent of the second harmonic phase with the exception of the region (150° - 220°), where the PAE presents a dramatic decrease, as shown in the inner plot of Fig. 3.32. The corresponding region in the Smith chart is called here "Z_{opt} ($N \cdot f_0$) critical region".

To extract the optimum load impedances of the transistor, a similar approach in [Paper B] was used, where the desired bandwidth was split into three sub-bandwidths:

- Lower sub-band F_{L0} = [0.5 – 0.95] GHz.
- Middle sub-band F_{M0} = [1.0 – 1.3] GHz.
- Upper sub-band F_{H0} = [1.35 – 2.7] GHz.

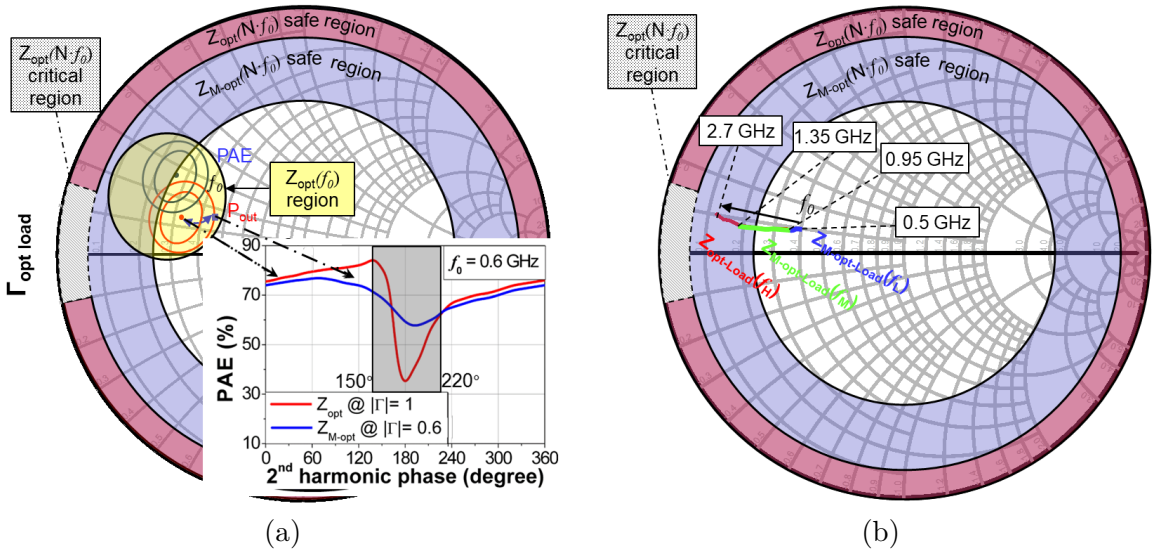
For the F_{H0}, harmonics lie out-of-band and their influence can be minimized by simply enforcing harmonics load impedance to lie at the "$Z_{opt}(N \cdot f_0)$ safe region".

On the other hand, for the F_{L0} and F_{M0} , the harmonics lie in-band, namely at the sub-band [1.0 – 2.7] GHz and their influence cannot be minimized following the described procedure in Section 3.2.1. The approach in [Paper B] has therefore been used. What was proposed here was to modify Z_{opt} for this band to an impedance $Z_{M.opt}$ with the aim of reducing the in-band harmonics influence. The innovative procedure described in the following was undertaken at the cost of minor degradations in the overall PAE and P_{out}.

It starts by determining the PAE and P_{out} impedance contours for the fundamental frequencies and then defines a locus in the Smith chart for the entire band, for which $P_{out-max}$-$P_{out} \leq 0.5$ dBm and the PAE $\geq$ 60 %. In other words, a mismatch was intentionally accepted at F_{L0} and F_{M0} to satisfy these relaxed requirements. Then, Z_{M-opt} and a new locus "Z_{M-opt}(N · f_0) safe region" were determined taking into account that the transistors have a lower gain at higher frequencies than at lower frequencies, as shown in Fig. 3.5 for the transistor used. This allowed for obtaining Z_{M-opt} , still lying in the same optimum safe region. Fig. 3.32(a) presents an example of impedance contours for $P_{out-max}$ and PAE at 0.6 GHz and the aforementioned loci. It shows how the optimum load impedance was slightly modified from $P_{out-max}$ to 0.5 dB less power with high PAE. The obtained Z_{M-opt} minimized the second harmonic influence and expanded the locus for the second harmonic. Fig. 3.32 shows the PAE versus the second harmonic impedance phase of Z_{M-opt} at 0.6 GHz for a reflection coefficient magnitude $|\Gamma| = 0.6$. This procedure was individually used for all frequencies across the F_{L0}. Hence, Fig. 3.33(b) presents the optimum fundamental load impedances for

the device across the desired bandwidth (solid continuous curve). It has three colors to refer to each sub-band F_{L0}, F_{M0}, and F_{H0} (blue, green and red respectively).

The optimum source impedances were determined without considering the higher harmonics, due to their minor influence in the transistor performance, as presented in Section 3.2.1.



(a) (b)

Figure 3.32: (a) $Z_{Opt}(f_0)$ region for max. P_{Out} and PAE, Z_{Opt} (Nf_0) and Z_{Opt-M} (Nf_0) safe regions, Z_{Opt}(Nf_0) critical region; PAE versus 2^{nd} harmonic phase impedance sweep for Z_{opt} @ $\Gamma = 1$ for Z_{M-opt} @ $\Gamma = 0.6$, both PAEs @ 0.6 GHz; (b) extracted optimum load impedances across F_{L0}, F_{M0}, and F_{H0}(blue, green and red solid line respectively) and harmonics safe/ critical regions.

3.4.2 Matching network realization

The design approach of the output matching network is split into two steps:

- A planar broadside coupled transmission line transformer was used for the first time as a main part of the output matching network. The theoretical concept of the transformer is presented in Section 2.6.2 as the key element of the output matching network, leading to significant circuitry simplification and loss reduction. The planar transformer has a (4:1) transformation ratio. The measured insertion of the transformer alone was less than 0.5 dB over the 0.3 – 6.0 GHz band [50].

- A pre-matching network is required between the transistor and the transformer to resonate out the drain source capacitance and match the real part of the transistor impedance to the impedance of the transformer input. The pre-matching network consists of a one-stage low-pass filter.

In Fig. 3.33, the circle, square, triangle, and cross curves present the reflection coefficients of the designed OMN for the fundamental, in-band second harmonic, in-band third harmonic, and out-of-band harmonics, respectively.

The input matching network (IMN) transformed the real part, 10 Ω mean values, of the optimum source impedance to 50 Ω. A two-stage L-type network Chebyshev low-pass filter was used in the IMN. The synthesized ideal input and pre-matching output networks were realized using TLi, i=1,2,3,...11. In this design, the inductors were replaced by high-impedance transmission lines TL_1, TL_3, TL_5, TL_7, TL_8, TL_9 and TL_{11}, while the capacitors were realized by low-impedance TL_2, TL_4 and TL_6, as shown in Fig. 3.34. Finally, the whole design was post-optimized after using the real components in the simulation environment to improve the total performance of PA. The reflection coefficient of the realized network (symbols) matched to the optimum packaged load impedances (solid lines) as shown in Fig. 3.33.

Fig. 3.34 shows the final schematic of the desired PA including the stability circuit to ensure a stability factor higher than unity over the whole frequency spectrum. The stability circuit consisted of a resistor R_S bypassed by capacitor C_S to improve the stability at high frequency. Whereas for low frequency, series resistor R_{GS} with capacitor C_{GS} and resistor R_G were added in IMN, as shown in Fig. 3.34. The Figure also includes a table with the length and width of each microstrip line of the schematic.

The PA was implemented on a Rogers 4003c substrate 5 cm × 11 cm in size. The circuit was mounted in a metal case of h = 2 cm in height to ensure sufficient height for the back cavity under the broadside coupled lines of the Guanella transformer. This guarantees high Z_{even} impedance, as shown in Fig. 3.35.

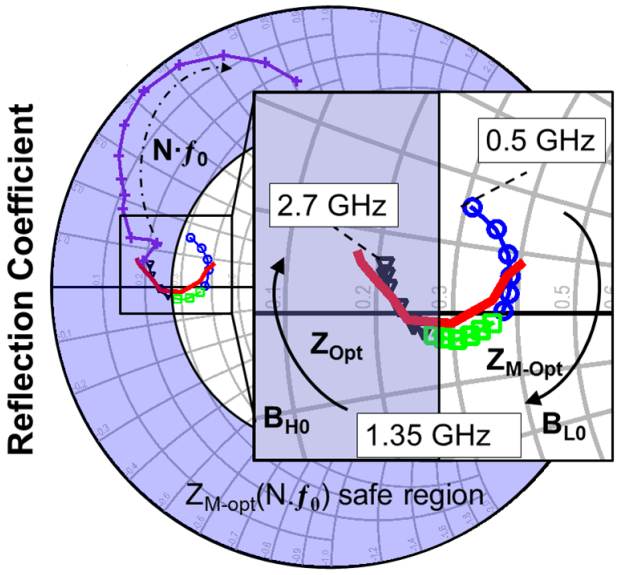
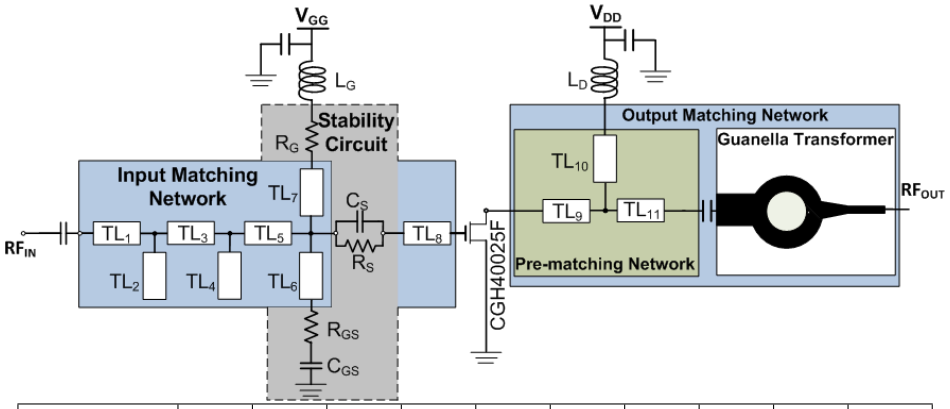


Figure 3.33: Ideal fundamental OMN (red solid lines), realized matching network across F_{L0}, F_{M0}, and F_{H0} (blue, green and red symbols respectively); harmonic matching is located in the safe region (purple area).



Line	TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7	TL_8	TL_9	TL_{10}
Length [mm]	3.0	4.4	17.3	7.0	15.2	1.0	2.5	14.0	2.5	5.9
Width [mm]	1.12	1.6	1.4	2.5	2.2	4.4	1.8	4.0	3.2	1.0

Figure 3.34: Circuit topology the designed PA; lines dimensions of the circuit.

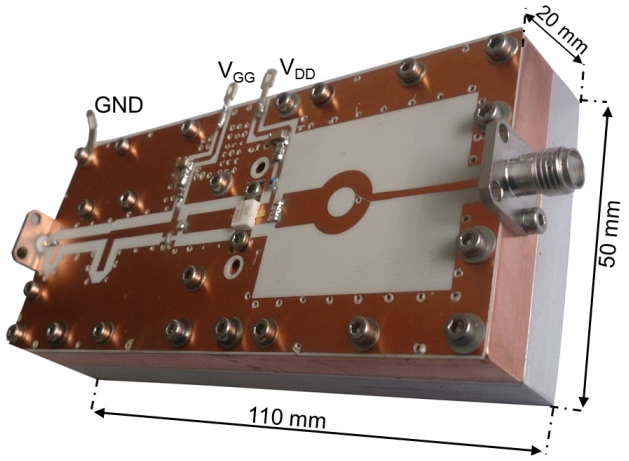


Figure 3.35: Prototype of the fabricated PA using planar transformer in OMN.

3.4.3 Experimental characterization

The PA was characterized for small- and large-signal conditions for a drain bias voltage of 28 V with I_{DQ} = 125 mA.

- **Small-Signal performance**

Comparisons between simulated and measured results over the frequency are presented in Fig. 3.36 for the fabricated PA. The measured return loss was in fair agreement with simulated results across the entire frequency band. The measured gain followed the simulated gain with a minimum value of 12.5 dB. Moreover, the Figure also presents the return loss of the realized PA, which has a good agreement with the simulation result.

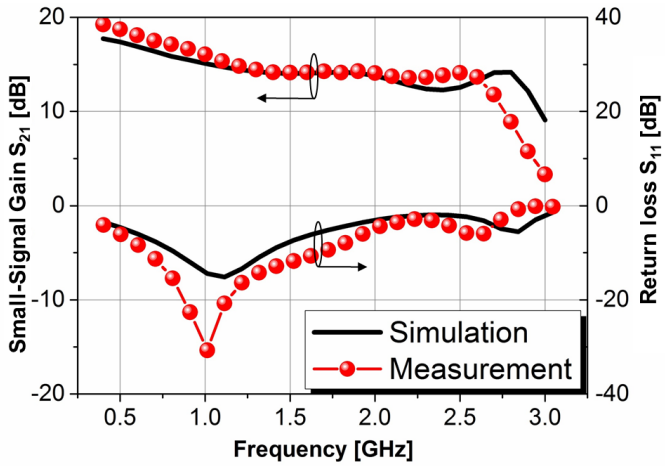


Figure 3.36: Comparison of small-signal gain (S_{21}) and return loss (S_{11}) between simulation (solid) and measurement (symbol) results for V_{DD} = 28 V / I_{DQ} = 125 mA.

- **Large-Signal performance**

Fig. 3.37 presents large-signal comparisons between simulated and measured results. A saturated output power ranging from 43 dBm to 45 dBm with drain efficiency from 56 % to 70 % and a gain of 10.2±1.6 dB has been obtained across 0.5 - 2.7 GHz for an input power of 34 dBm. The PAE over the band was between 50 % - 65 % at the 3 dB compression point.

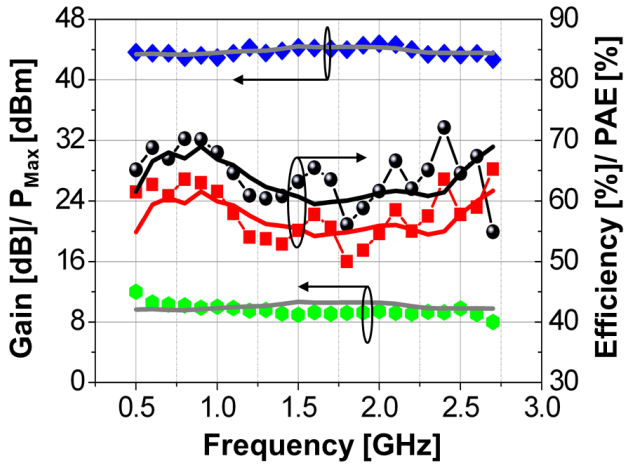


Figure 3.37: Comparison of large-signal performance between simulation (solid) and measurement (symbol) results for V_{DD} = 28 V / I_{DQ} = 125 mA.

Finally, Fig. 3.38 presents measured results versus the input power at 0.5, 1.6 and 2.7 GHz. At these three frequencies, the output power saturates at about 45 dBm with the drain efficiency around 67 %.

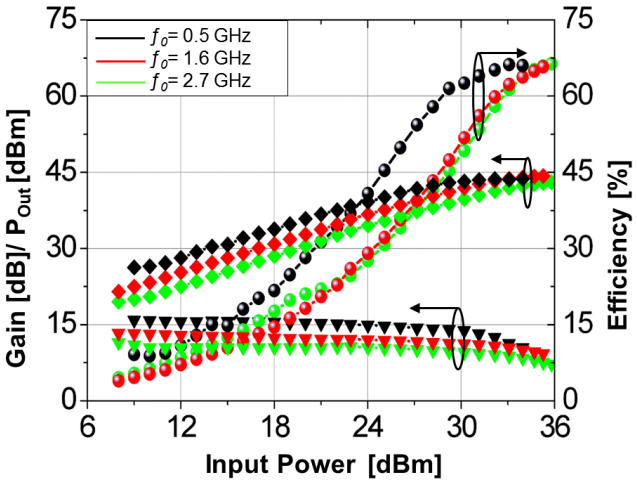


Figure 3.38: Large-Signal performance versus input power for 0.5, 1.6, and 2.7 GHz.

3.4.4 Conclusion

An innovative approach to reducing the influence of in-band harmonics on the power-added efficiency in power amplifiers has been presented. Moreover, the use of a planar transformer based on broadside coupled TLs as the key element for the realization of the output matching network has been explored for the first time. An output power of more than 20 W has been obtained with a minimum measured PAE higher than 50 % over the 0.5 - 2.7 GHz band. The achieved results open a new perspective for the development of high power and high efficiency decade bandwidth power amplifiers, which will be presented in the following designs. Table 3.6 summarizes the performance of the design.

Table 3.6: Summary of Multi-octave GaN 20 Watt PA performance using planar transformer in OMN.

f [GHz]	P_{Out} [dBm]	Gain [dB]	Efficiency [%]
0.5	44.2	11.8	65
0.7	44	11	67
0.9	44	10.5	70
1.1	44.2	10	64
1.3	44.3	10	61
1.5	44.4	9.6	63
1.7	44.3	9.7	63
1.9	44.7	10	57
2.1	44.8	9.6	66.5
2.3	43.7	9.8	65
2.5	43.5	10.3	64
2.7	43	8.6	56

3.5 Multi-Octave 100 W PA using planar transmission line transformer

The main aim here is to design highly efficient multi-octave power amplifier with a 100 W output power over 0.6 - 2.7 GHz using planar transmission line transformer. Based on a previously successful design in [Paper C], which used the approach of adapting optimum load impedances and planar transformer on the output side of the matching network, this design will use the same approach in extracting the optimum source-/load-impedances to minimize the impact of the harmonics and solve the in-band problem. Using a planar transformer on the input and output side of the transistor simplifies the matching structure. Another challenge in this design is that a large transistor size is used to obtain high power. Therefore, the optimum source-/load-impedances are too small, leading to complexities in pre-matching networks between the planar transformer and the transistor.

3.5.1 Design approach

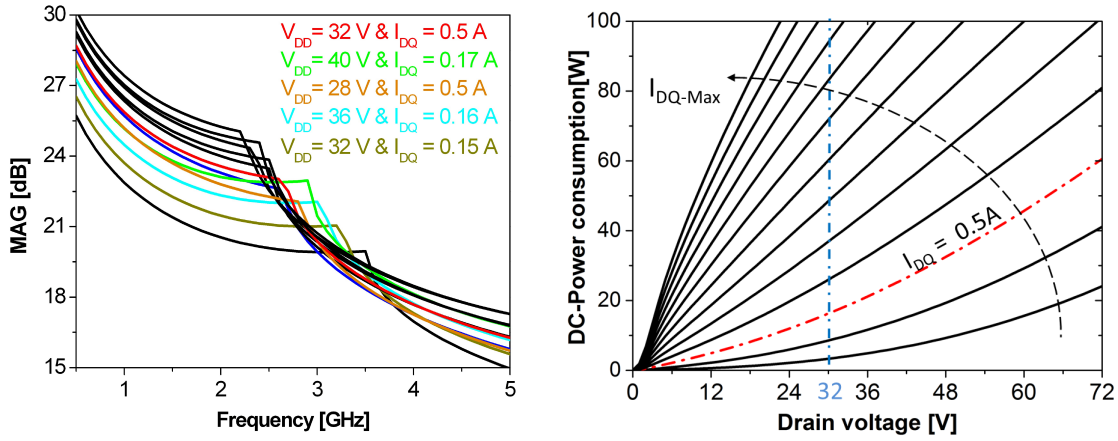
Designing efficient PAs for multi-octave bandwidth with a high output power presents intrinsic challenges. Large periphery devices are required to obtain high power; hence the bandwidth is restricted because of the high device capacitances (C_{DS}, C_{GS}), as shown in Table 4.1. In this respect, the high breakdown voltage and high output power density of GaN-HEMT devices have significant advantages in terms of power and bandwidth, as presented in Section 2.1. A CGH40120F by Wolfspeed Inc. has therefore been used. This device is based on a 400 nm gate length GaN technology which can handle a high breakdown voltage up to 85 V. The optimum operating point for maximum transconductance is stated at $\mathrm{V}_{DD} = 28\,\mathrm{V}$ and $\mathrm{I}_{DQ} = 1\,\mathrm{A}$. At this operating point the simulated extrinsic transit frequency is about $f_T = 8.5\,\mathrm{GHz}$ with a maximum oscillation frequency of $f_{MAX} = 18\,\mathrm{GHz}$, which makes the device suitable for mobile communication systems.

The bandwidth of the designed PA was defined based on the requirements of the wireless communication standards, power-bandwidth limitations of the device and, finally, the bandwidth of the implemented MNs. In Section 3.1.4, only the CG40025F was characterized. Therefore, Fig. 3.39 characterizes CGH40120F and illustrates the maximum available gain (MAG) and maximum stable gain (MSG) of the device versus frequency at various drain voltages and quiescent currents.

Increasing the drain voltage results in a raised MAG and output power. However, the usable frequency band decreases and the dissipated power of the device increases. Therefore, a compromise between these factors has been considered with a drain biasing of $\mathrm{V}_{DD} = 32\,\mathrm{V}$ and $\mathrm{I}_{DQ} = 0.5\,\mathrm{A}$, where a high MAG with a low DC-power consumption was available up to 2.7 GHz.

In this context, source-/load-pull simulations, using the accurate large-signal transistor model from Wolfspeed Inc., have been performed. The effect of the harmonics in source-/load-impedances on output power and efficiency was analyzed and taken into consideration to enhance the efficiency over the desired band. Based on [18], only up to the second load harmonic impedances should be considered during the load-pull analysis, whereas the influ-

ences of second source harmonic and third load harmonic were omitted, due to their minor effect compared to the complexity introduced to the design of the matching networks.



(a) (b)

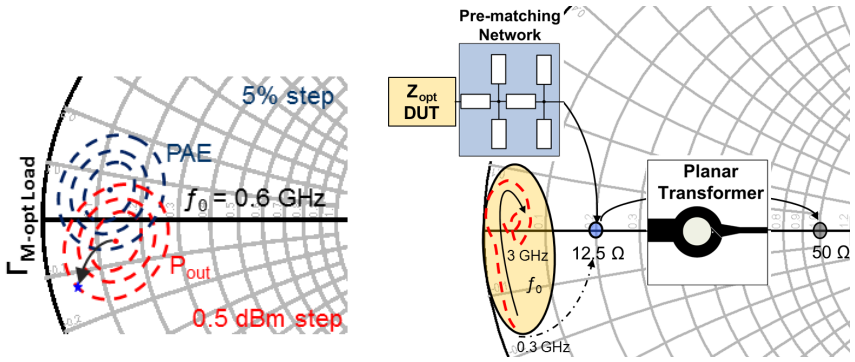
Figure 3.39: (a) MAG of CGH40120F at various bias conditions; (b) dissipated power versus various biasing.

However, the in-band harmonics are the bottleneck of this work, as presented in the previous design, in Fig. 3.31. This problem can be solved using the design approach which was used in [Paper C], where the advantage of the high MAG of the device at low frequency range was utilized to intentionally modify the optimum fundamental load impedances of the low frequency band (f_{L0}) and middle frequency band (f_{M0}) from their optimum value, though the same safe optimum range, ensuring a 100 W output power. In other words, a mismatch was purposely chosen for the fundamental impedance at f_{L0} andf_{M0} band. Consequently, lower gain was available and the impact of higher harmonics ($H \cdot f_0$) was minimized. Fig. 3.40(a) shows an example of modifying the optimum load impedance of 0.6 GHz. As such, the high gain response at f_{L0} andf_{M0} band decreased and resulted in a more flat gain within bandwidth of operation. Finally, the extracted optimum load impedances are presented in Fig. 3.40(b).

In addition, the optimum source-/load-impedances of large periphery devices were low and requiring broadband impedance transformations from 50 Ω to a low complex load. In this respect, the designed matching network topology should consist of two main parts. The first one transforms the 50 Ω impedance plane to 12.5 Ω. This transformation was achieved using a broadside coupled (4:1) transformer. The second one matched the broadside coupled transformer low impedance plane to the extracted optimum complex impedances of the device Z_{opt}, as shown in Fig. 3.40(b).

The use of the broadside coupled transformer has been designed based on the presented approach in Chapter 2. Two topologies were simulated, implemented and measured. The first one (Top. I) was based on a previously presented structure [50], whereas, the second one (Top. II) was modified using a tapered ground plane instead of a microstrip line in Top.I for a smooth transition instead of a microstrip line as in [50]. It ensures a high transmission coefficient and lower parasitic impact, as shown in Fig. 3.41. The top metallization is the

same for both structures. The Figure also presents the prototype of the transformer. It was fabricated using a Rogers 4003c substrate with a total size of 2.4 cm × 3.75 cm, smaller than Top. I.



(a) (b)

Figure 3.40: (a) Load impedance locus at 0.6 GHz; (b) optimum fundamental impedances $Z_{opt-load}$ of the transistor, pre-matching network topology to match $Z_{opt-load}$ to 12.5 Ω and broadside coupled transformer to match it to 50 Ω.

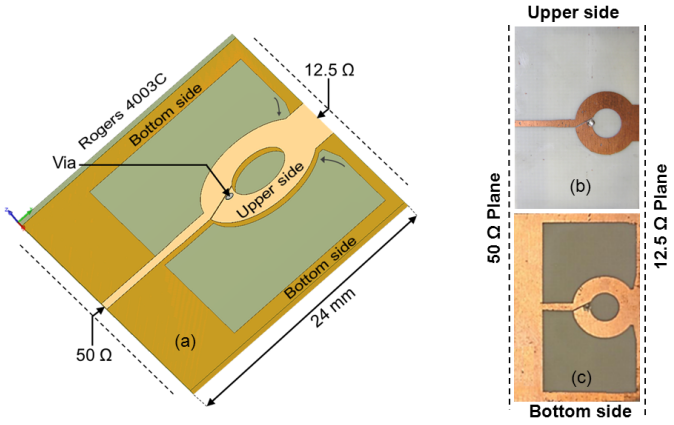


Figure 3.41: (a) Transformer model; (b) upper and (c) bottom side of the transformer Top. II.

A comparison of the measurement results of the two topologies is presented in Fig. 3.42. There was a good agreement between measurement and simulation of both topologies. Top. II observed a more flat and better IL compared to Top. I with a value of less than 0.5 dB and a RL of 15 dB over a decade bandwidth 0.4 - 4.0 GHz, as shown in Fig. 3.42.

Based on this study, the desired bandwidth of the PA was defined over 0.6 - 2.6 GHz. The transformer was used on both sides of the device. The measured results of the transformer were imported, de-embedded and used as a reference plane for the pre-matching networks.

The main aim of the pre-matching network is to match the complex extracted optimum source-/load-impedances of the transistor to the transformer de-embedded low impedance plane. Therefore, a multi-stage Chebyshev low-pass filter consisting of two stages L-type

network was used. Moreover, a stability factor higher than unity was considered to avoid oscillation of the PA by choosing an appropriate stability circuit.

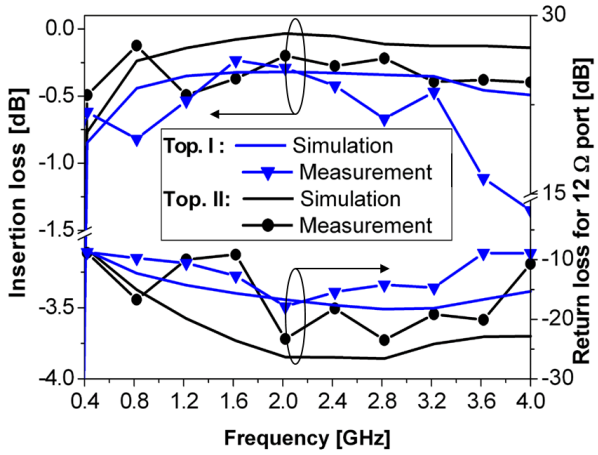


Figure 3.42: Insertion loss and return loss of 12.5 Ω plane comparison between simulation and measurement results of Top. I and Top. II.

The PA was implemented on a Rogers 4003c substrate with 6 cm × 16 cm in size and with a heat sink height of 2 cm (1 cm is the height of cavity below the input-/output-transformers). The total circuit without the active device was evaluated using a 50 Ω microstrip line instead of the transistor. The forward transmission (S_{21}) measurement results showed a good agreement with the simulation (schematic and momentum) across the desired bandwidth with a minimum value of -4.5 dB, as shown in Fig. 3.43. These losses were basically related to the R_{GS} resistor which was used to stabilize the designed PA, and the mismatch, due to the replacement of the transistor with a 50 Ω microstrip line.

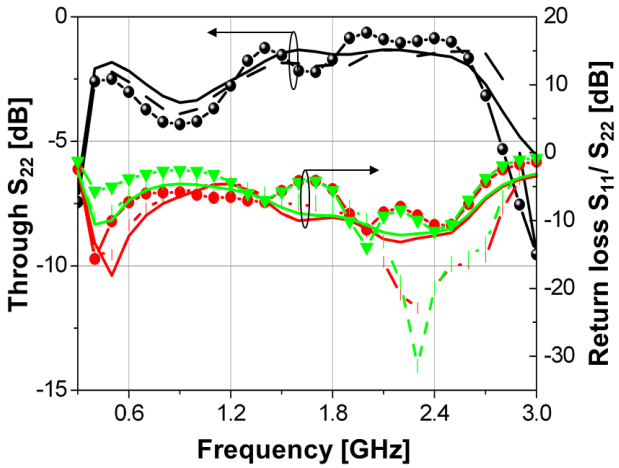


Figure 3.43: Through and return loss comparison of the whole design using 50 Ω microstrip line instead of the active device between simulated schematic (solid line), momentum (dashed line) and measured (symbols) results.

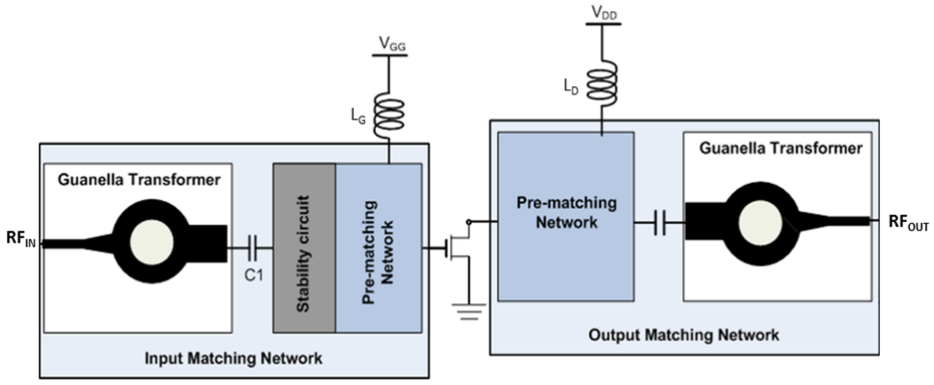


Figure 3.44: Circuit topology the designed PA.

The final prototype of the PA involving the transistor is shown in Fig. 3.45.

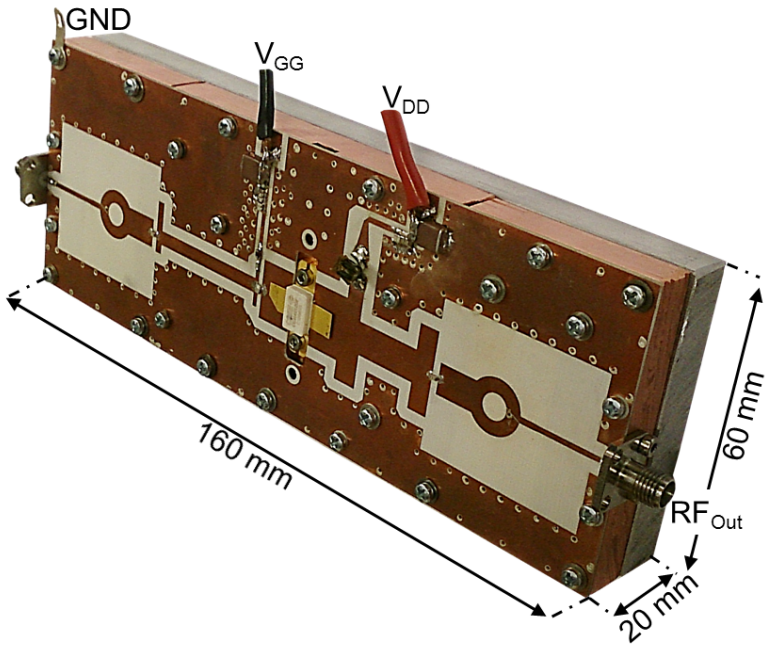


Figure 3.45: Prototype of the fabricated PA using planar transformer in IMN and OMN.

3.5.2 Experimental characterization

The implemented broadband PA has been characterized by small- and large-signal measurements to evaluate its performance. Measurements were performed at a drain bias voltage of 32 V and quiescent current of 0.5 A. Preliminary experimental results showed a good agreement with the simulated data over the design band.

- **Small-Signal measurements**

The comparison between the simulated and measured small-signal gain is presented in Fig. 3.46, as long with the input reflection of the fabricated PA. The measured return loss was in agree-

ment with simulated results across the bandwidth, whereas the measured gain of the designed PA was subsequent to the simulated gain with a minimum value of 12 dB across 0.6 - 2.6 GHz.

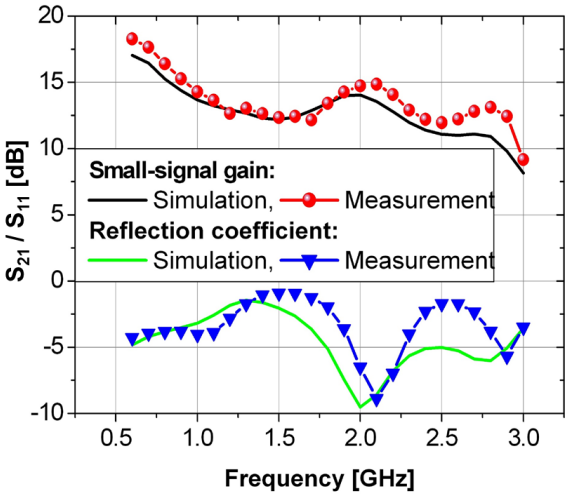


Figure 3.46: Comparison between simulated and measured small-signal gain, reflection coefficient performance at V_{DD} = 32 V and I_{DQ} = 0.5 A.

- **Large-Signal measurements**

Fig. 3.47 shows the measurement setup in lab, where a continuous wave (CW) input signal generated by microwave signal generator (Agilent E4438C) boosted by two drivers. The first driver was from Mini-Circuits Inc. (Pre-PA-1), whereas the other driver was the design [Paper C] (Pre-PA-2), as shown in Fig. 3.47. The output relevant power was measured by a calibrated power meter (Agilent N1912A).

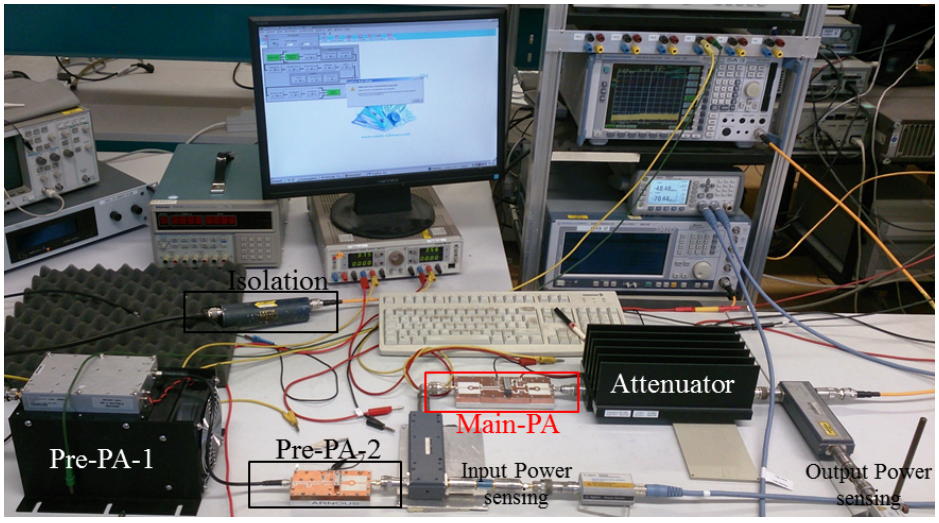


Figure 3.47: Measurements setup in lab.

Fig. 3.48 reports on the comparison between simulated and measured output power, power

gain, and drain efficiency as functions of the frequency. The measured results have a good agreement with the simulated ones with a maximum output power of 49.6 ± 1 dBm, average drain efficiency of 57 % and large-signal gain of 11.4 ± 2.4 dB across 0.6 - 2.6 GHz.

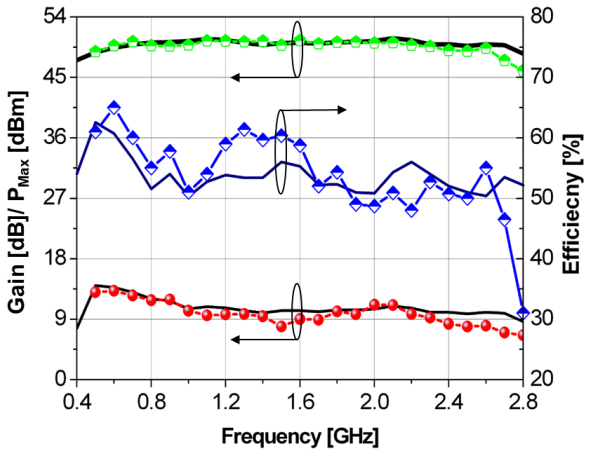
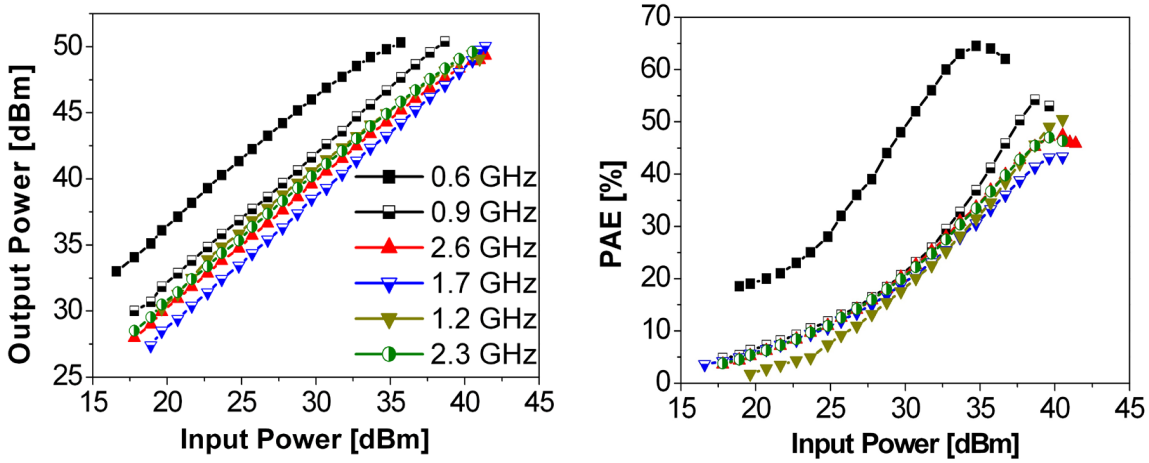


Figure 3.48: Comparison between simulated (solid lines) and measured (symbols) maximum P_{out}, power gain, drain efficiency across the bandwidth at V_{DD} = 32 V, $I_{DQ} = 0.5$ A.

Fig. 3.49 illustrates the measured saturated output power and the PAE with respect to the input power at various frequencies. The measured PAE was between 42 % - 64 %.



(a) (b)

Figure 3.49: Output power and power-added efficiency for various frequencies versus input power at V_{DD} = 32 V, I_{DQ} = 0.5 A.

Fig. 3.50 shows the measured 2^{nd} and 3^{rd} harmonic distortion power level relative to the fundamental frequency output power at various output power levels and different frequencies. The chosen frequencies were 0.7 GHz, its 2^{nd} and 3^{rd} harmonics are located in the desired

band, 1.4 GHz, its 2^{nd} harmonic is at the edge of the band and 3^{rd} harmonic is out of band, and finally 2.0 GHz, where the harmonics are out of band.

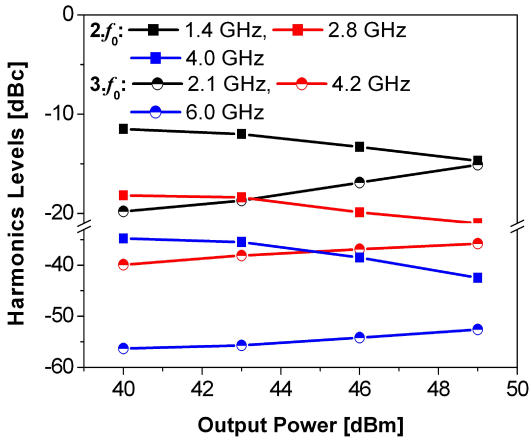


Figure 3.50: Measured 2^{nd}, 3^{rd} relative harmonics level versus output power at 0.7, 1.4 and 2.0 GHz fundamental frequencies at V_{DD} = 32 V, I_{DQ} = 0.5 A.

3.5.3 Conclusion

The design of high power, multi-octave, and high efficiency PA was presented. The bandwidth restriction was solved using an efficient ultra-wideband transmission line transformer. A ground tapered microstrip line was used to achieve flat and low insertion loss and high return loss. The transformer was integrated with the input and output matching networks. There was a good agreement between the measured results and the simulation, with a maximum output of 50.6 dBm, average drain efficiency higher than 50 % and gain 11.4 ± 2.4 dB. Table 3.7 summarizes the performance of the 100 Watt multi-octave PA using the planar transformer over the design band.

Table 3.7: Summary of multi-octave GaN 100 Watt PA performance using planar transformer in IMN and OMN.

f [GHz]	P_{Out} [dBm]	Gain [dB]	Efficiency [%]
0.6	49.5	13.8	65
0.8	49.5	11.7	55
1.0	49.6	11	53
1.2	50.3	10.5	58
1.4	50.3	10	59
1.6	50.4	9	57
1.8	50.1	11	54
2.0	50.2	11.25	49
2.2	49.8	10	48
2.4	49.2	9	52
2.6	48.6	9	55

4 Efficiency Enhancement of Wideband PAs using Modulation Techniques

As discussed in Chapter 1, most of the dissipated power in the RBS is consumed by the PA. This value will dramatically increase in the coming years as higher data rates and more complex modulation schemes of new communication standards (3G, 4G, 5G, and WiMAX) together with their rapid growth, see Fig. 4.1, will require higher output power from the PAs and a higher number of RBSs. The efficiency of PAs will thus have a high impact on the total energy consumption of RBSs. Furthermore, as highly efficient PAs reduce the need for large cooling setups and reduces the component failure, due to high transistor temperature, other parameters such as weight and reliability can be indirectly improved by improving PA efficiency.

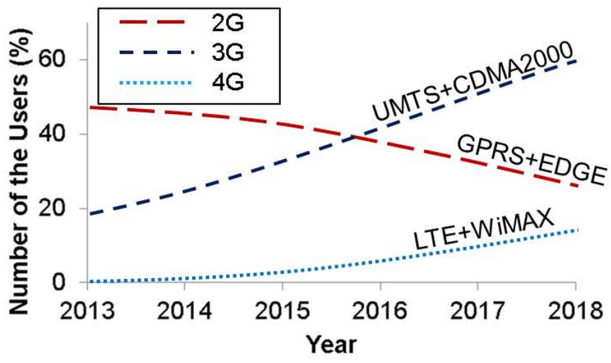


Figure 4.1: Statistic for the number of users in the modern mobile standards.

Today, improving the efficiency at back-off output power has become an important factor in evaluating the performance of radio base stations due to the emergence of new communication standard. Modulation schemes, such as orthogonal-frequency-division-multiplexing (OFDM), and quadrature amplitude modulation (QAM) are used in modern wireless communication systems to maximize the spectral efficiency [37]. These modulation schemes result in signals with large amplitude variations and peak to average power ratios (PAPRs) in the range of 6 - 12 dB [68, 69].

The modulation techniques used in new mobile communication standards employ complex schemes (Table 4.1), so the requirement for broadband and highly linear PAs with high OBO efficiency becomes one of the main challenges. As shown in Fig. 4.2 in comparison to GSM with 0 dB OBO on its probability density, new standards require 6 - 12 dB OBO power from the maximum output power of the PA. In this case, using a conventional PA topology, such as class-B results in an average efficiency of 15 % to 35 %, depending on the application.

This means 65 % to 85 % total power dissipation and 2 to 5 times more power dissipation than the 2G (GSM) application. By considering the RBS power consumption mentioned in the previous Section, the need for PAs with high back-off efficiency becomes more apparent. Fig. 4.2 also shows that the PDF of the GSM signal is ideally a Dirac delta function and it has been downsized for clarity. It also shows how the drain efficiency of an ideal class-B and class-A amplifier depends on output power.

Table 4.1: Wireless evolution of most common wireless standards.

Standard	Application	Freq. [GHz]	PAR [dB]	Modulation
GSM	2G	0.8, 1.8, 1,9	0	SC-GMSK
EDGE	2.75G	2.1	2	SC-8-PSK
UMTS	3G	2.1	5.5	WCDMA-QPSK
HSPA+	3.5G	2.1	6.5	WCDMA-16QAM
LTE	3.9G	2.6	8-10	QFDM-64QAM
LTE-A	4G	3.7	8-12	QFDM-64QAM
802.16E	WiMAX	2.3	12	QFDM-64QAM
LTE-A Pro	5G	0.7,3.5	-	QFDM-256QAM

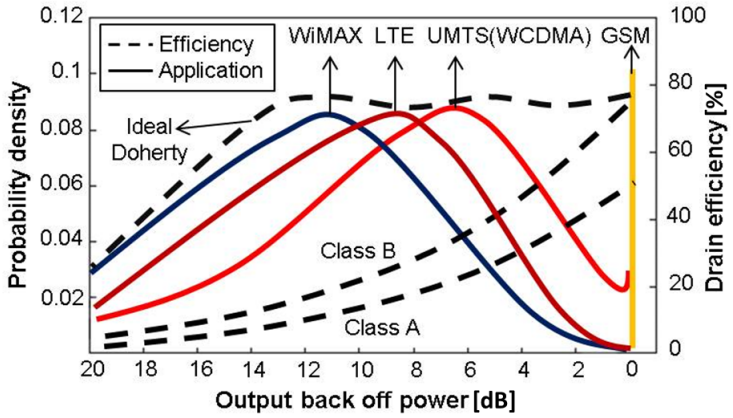


Figure 4.2: Probability density functions (PDFs) of a GSM, WCDMA and LTE signal.

In order to prevent strong signal distortion, these signals require the PA to operate at an average output power far below the saturation region and therefore at low efficiency levels. This is why various modulation techniques have been developed, as presented previously, to ensure high efficiency at various output power levels.

4.1 Modulation techniques

To enhance the PA efficiency at back-off region, various techniques, such as active load modulation (Doherty PA) [70, 71], Chireix Outphasing [72], dynamic supply modulation (DSM) [73, 74, 34] also known as envelope tracking and dynamic load modulation, and passive load modulation [75], have been proposed. These techniques are the most promising methods for improving efficiency at various OBO power levels. Nevertheless, many limitations must be faced during the design of such PAs. In most cases, the main issue lies in the PA

bandwidth. To keep the power and efficiency performance over a wide frequency range as high as possible is one of the most serious challenges in PA design. The following Section presents all techniques and highlights the pros and cons of each technique.

4.1.1 Dynamic supply modulation (DSM)

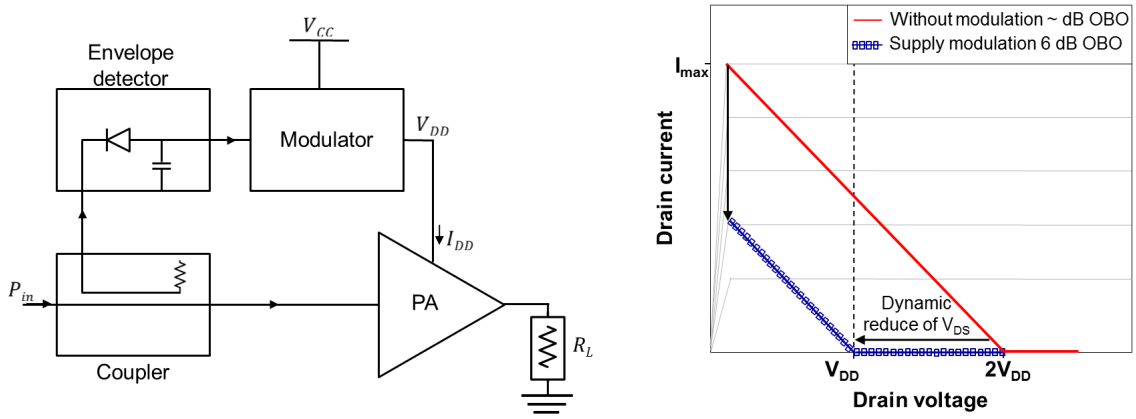
The main approach of supply modulation is presented in Fig. 4.3, where the supply voltage (V_{DD}) reduces when the PA works at back-off region, hence results in changing the load line of the transistor to the appropriate optimum load impedance at the back-off output power level to ensure a high efficiency performance.

Using an envelope power amplifier (EA) ensures a high drain efficiency performance even at a small output power level. Based on the control of the EA, the amplifier can be classified into two categories:

1. Envelope Elimination and Restoration (EER), first proposed by Kahn in 1952 [76].

2. Envelope Tracking (ET) [77].

   The bandwidth of these techniques is only limited by the bandwidth of the PA itself. In this case, this topology can be a good option for broadband design.



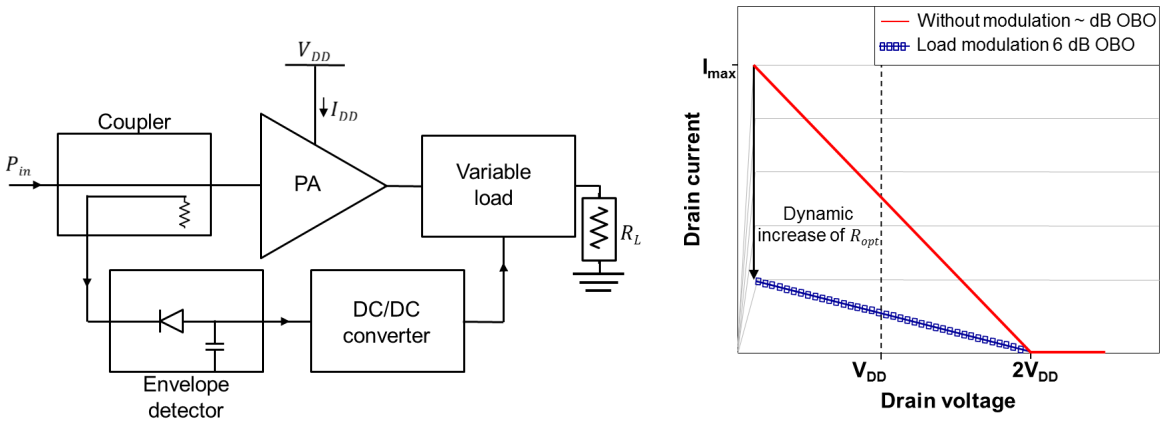
(a) (b)

Figure 4.3: (a) Schematic approach of EA; (b) load line of ideal class-B PA(solid line) and supply modulation load line (symbols).

A drawback of supply modulation is that the performance of any supply modulated PA depends significantly on the EA efficiency, bandwidth, peak power, dynamic range, etc. Moreover, this method requires efficient DC/DC converter as well as efficient envelope tracking amplification. In other words, the overall efficiency is seriously degraded by the supply modulator. However, the main issue of this technique is the maximum bitrate limitations faced by the supply modulator. The digital circuitry of the supply modulator must provide in most cases a bandwidth of up to 10 times the maximum bitrate [78], which can be a big source of complexity and cost increase for high data rate applications.

4.1.2 Dynamic load modulation (DLM)

The schematic approach of the dynamic load modulation is presented in Fig. 4.4(a). It can be used to improve the efficiency at various back-off output power level. The main concept is to change the load line slope using a reconfigurable matching network to match the optimum load at backed-off output power to 50 Ω to achieve high efficiency, as shown in Fig. 4.4(b).



(a) (b)

Figure 4.4: (a) Schematic of the load modulation circuit; (b) ideal class-B and load modulation load line with and without using the load modulation technique.

This kind of modulation can be achieved by using one of the following techniques.

4.1.2.1 Active load modulation technique

This technique consists of two or more amplifiers in order to vary the amplitude and phase balance between the output currents I_1, I_2 and I_n. The load impedances Z_1, Z_2 and Z_n can be modulated. The most common active dynamic load modulation techniques are the Doherty power amplifier, which was originally proposed by W. H. Doherty [71], and the outphasing power amplifier, which was originally proposed by H. Chireix [79].

1. **Doherty power amplifier**

   The Doherty power amplifier essentially relies on a constant phase between the sub-amplifier output signals. The load modulation is achieved by varying their amplitude relationship. The right amplitude relation can be obtained by using:

   - A single RF-driver.
   - An analog power splitter.
   - Proper sub-amplifier gate-bias.

   This makes the Doherty power amplifier the only technique of the efficiency enhancement techniques which does not require any additional drivers or control circuits. Fig. 4.5 shows the basic circuit topology of the Doherty PA. However, the main problem in such a design is the limited bandwidth. Other issues are the higher complexity and cost.

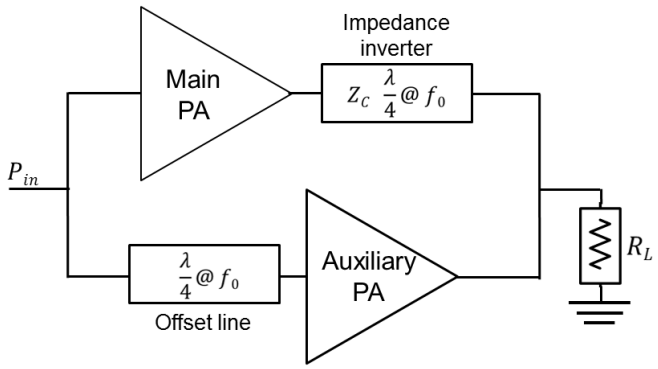


Figure 4.5: Schematic circuit of Doherty PA.

2. **Outphasing power amplifier**

   Outphasing methods rely on a constant voltage amplitude for all power amplifiers. The load modulation is achieved by varying the phases between currents as the signal envelope varies. Nevertheless, this technique demands the phase between the input signals be controlled quickly and accurately. It requires separate RF-driver for each sub-amplifier, thus making the implementation fairly complex. Fig. 4.6 illustrates the basic concept of outphasing PA.

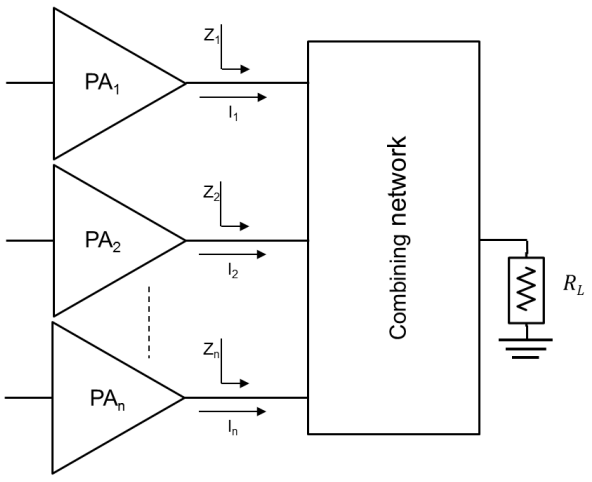


Figure 4.6: Schematic circuit outphasing PA.

4.1.2.2 Passive load modulation technique

Tunable passive component is an essential element for building tunable matching networks (TMNs). Fig. 4.7 presents the passive load modulation approach. The main advantage of

this approach is that it can be applied to both the input and output side of the transistor to get the maximum available efficiency enhancement at various output back-off power levels. The tunable component can be either the coil or the capacitor.

The tunability range of the coil is small and cannot handle a high output power level. The main tunable factors in the coil are shown in Eq. 4.1:

$$L = \mu_0 \cdot \mu_r \cdot \frac{N^2 \cdot A}{l} \tag{4.1}$$

where:
L: Inductance value [Henry]
μ_0: Permeability of free space $(4 \cdot \pi \cdot 10^{-7})$
N: Number of turns
A: Inner core area $(\pi \cdot r^2)$ $[m^2]$
l: Length of the coil $[m]$

Changing the number of turns or the inner core area, the length of the coil, or even the μ_r is not a simple parameter for tuning. The capacitor is considered as the best component to be tuned in passive load modulation techniques. The variable capacitor is called varactor. There are many varactor variants based on the technology used for tuning the capacitor. The main equation for the capacitor is presented in Chapter 2, Eq. 2.1.

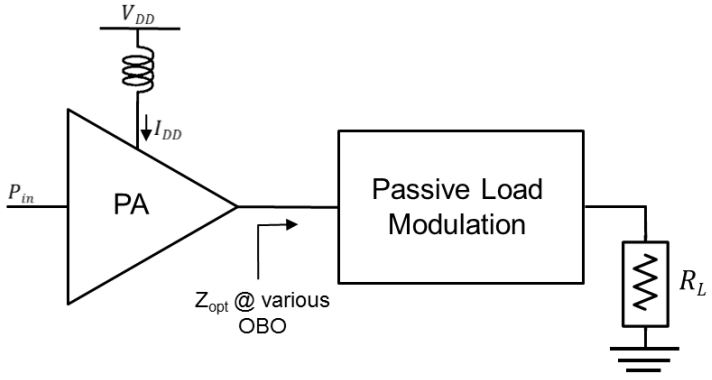


Figure 4.7: Simple circuit topology of passive load modulation power amplifier.

The varactor technology employed can be classified into three main categories:

- **Semiconductor-based varactor diodes:**

The varying method of the capacitance is based on changes in the depletion layer width in the semiconductor. The smaller the width of depletion region, the higher the capacitance value is based on the Eq. 2.1. The concept of the semiconductor and the equivalent circuit is presented in Fig. 4.8.

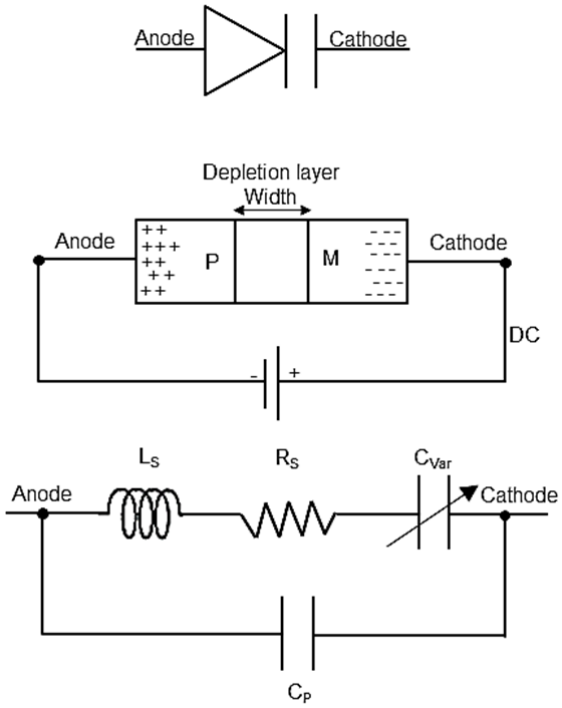


Figure 4.8: Semiconductor varactor symbol, concept and equivalent circuit.

Semiconductor-varactors show considerable advantages with respect to tuning voltage, tuning speed and tuning range. The major disadvantage of semiconductor-varactors is the lower breakdown voltage. Silicon and silicon-carbide (SiC) are used for designing varactors. Each material has its advantages and disadvantages. Moreover, another approach is introduced such as using the transistor in reverse mode to be used as variable capacitors, such as GaN transistors. This approach is not efficient from the cost point of view.

- **Micro-electro-mechanical systems (MEMS) varactors:**

The varying method of the capacitance is based on changing either the distance between two electrodes (d) for planar capacitors or effective electrode overlapping area (A) for comb-like structures or by a movable dielectric [80, 81]. The MEMS varactors have been widely used for tunable RF circuit design. The advantages of using MEMS technology can be mainly determined with low loss and high linearity; however, they also have a number of drawbacks, including high bias voltage, low power handling capability, slow tuning speed, as well as costly packaging requirements.

- **Barium-strontium-titanate (BST) ferroelectric based varactors:**

The varying method of the capacitance is based on changing the dielectric constant (permittivity) ε_r of the $Ba_{0.4}Sr_{0.6}TiO_3$ between two planar electrodes by sweeping the applied control voltage $\varepsilon_r(V_{CON})$ [82]. The BST based varactor consists of an Interdigital capacitor (IDC) as shown in Fig. 4.9. The length, gap, and width of the fingers are the main factors which determine the main value of the capacitors at $V_{CON} = 0$. In this approach, the tunability range is defined as the capacitance change normalized to the un-tuned capacitance.

The mathematical relationship between the bias voltage and the capacitance is expressed in Eq. 4.2.

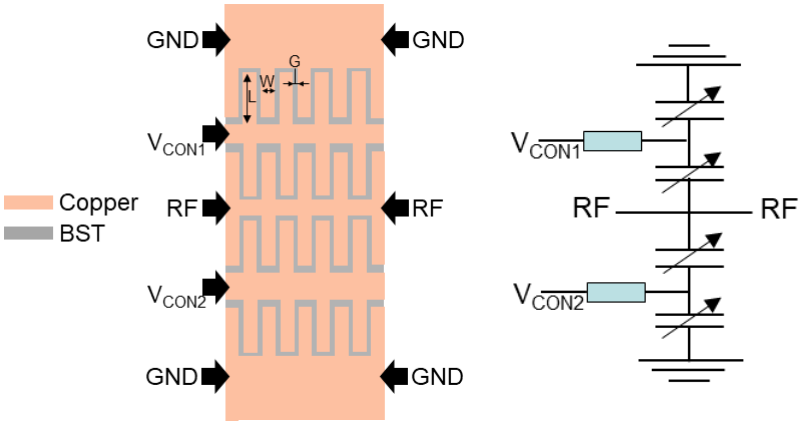


Figure 4.9: (a) Top view of IDC varactor pair and equivalent circuit.

$$\tau(V) = \frac{C(0) - C(V)}{C(0)} \tag{4.2}$$

where:
τ(V): Tunability range with respect to V
V: Applied control voltage of the BST
C(0): Tunable capacitance at V=0
C(V): Tunable capacitance respect to V

The gap between the IDC actually represents a trade-off between tunability and linearity. The fabrication and processing of BST as well as the realization of tunable components based on BST thick-films can be found in [83, 84]. The whole simulation, fabrication, and characterization of the BST alone have been done in the Institute for Microwave Engineering and Photonics at Darmstadt University, Germany. The substrate preparation of the BST based varactor has done at Karlsruhe Institute of Technology (KIT).

There are mainly two kinds of BST based varactors:

1. Thin-film BST based varactor.

2. Thick-film BST based varactor.

The main difference between the two approaches is related to power handling capability, tuning range, tuning voltages and linearity. Thick-film BST based varactors can provide a higher tunability range and linearity.

Table 4.2 compares the performance between the three varactor technologies.

Table 4.2: Comparison between varactor technologies.

Varactor type	Semicoductor	MEMS	BST
Tunability range	++	++	+/-
Quality factor	+/-	++	+/-
Biase voltage	medium	high	high
Tuning speed	fast	slow	medium
Power handling	low	low	high
Lineartiy	+/-	high	+/-

Fig. 4.10 summarizes the techniques which can be used to improve the efficiency at backed off output power.

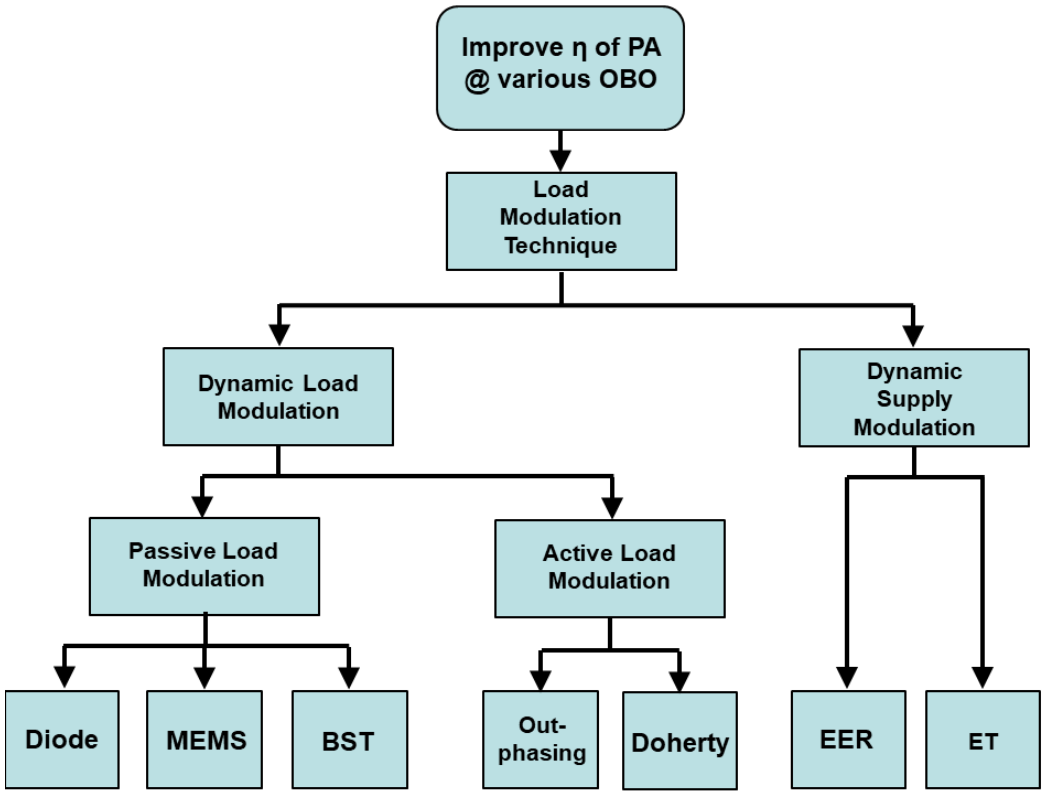


Figure 4.10: Block diagram of available modulation techniques and used technologies.

Most of the recent work which has been carried out in this domain was only developed for narrowband application, unlike here where the main focus is to expand the bandwidth alongside improving the efficiency at back-off power. In terms of cost, complexity and additional power consumption, the DLM technique using passive components seems to be more efficient and robuster than the DSM and Doherty amplifier in spite of challenges in the dynamic range of power detector and the required speed to follow the envelope variation. The main concept of the load modulation technique is to change the slope of the load line using reconfigurable matching networks to match the varied optimum load impedances based on the backed-off

output power level to 50 Ω to achieve high efficiency.

Passive load modulation can be realized by tunable matching networks (TMNs) using conventional passive components such as micro-electro-mechanical systems (MEMS) [81], semiconductors or ferroelectric based varactors [73]. Alternatively, a passive load modulation technique using barium-strontium-titanate (BST) varactors can be implemented [82]. Recently, thick-film BST components have demonstrated promising perspectives in terms of tunability with high power capability [85]. Generally, BST based TMN does not add any extra power consumption to the whole design due to the nA-range DC current leakage. The TMN, which presents different load impedances at various power levels, can be deployed to compensate the amplitude and phase distortions generated by the transistor [86]. The use of this promising technology opens new horizons for PA design with high efficiency at backed off power levels with low cost, low complexity, and low power consumption.

This Chapter presents two designs using the passive load modulation technique to improve the efficiency at various output-back-off (OBO) power levels, due to its advantages compared with other techniques:

- A broadband load modulated PA using lumped capacitors (CAP-PA).
- A broadband load modulated PA using Barium-Strontium-Titanate (BST-PA).

In this dissertation, two technologies of passive load modulation are presented. One is the semiconductor-based varactor diode and the second is Barium strontium titanate-based varactor.

4.2 Wideband PA using capacitors as modulation elements (CAP-PA)

This PA can be considered as a reference prototype to evaluate the performance of the other prototype. The tunability method of this design was realized by manually replacing the lumped components of the output matching network to match the varied optimum load impedances based on the backed-off output power level to 50 Ω to achieve high efficiency across the desired bandwidth.

4.2.1 Varactor-diode based matching networks

Using semiconductor technology to design a dynamically tunable matching network is quite widespread, because of the big commercial market, which uses this technology. The main challenge therefore is to choose the right varactor in terms of tunability range, power handling, linearity, power consumption, and fast response. The semiconductor varactor diode can be integrated with the distributed matching network in order to simplify the tuning range. The matching network of the PA can include a step or stub beside the tunable varactor in order to enhance the tunability range, as shown in Fig. 4.11.

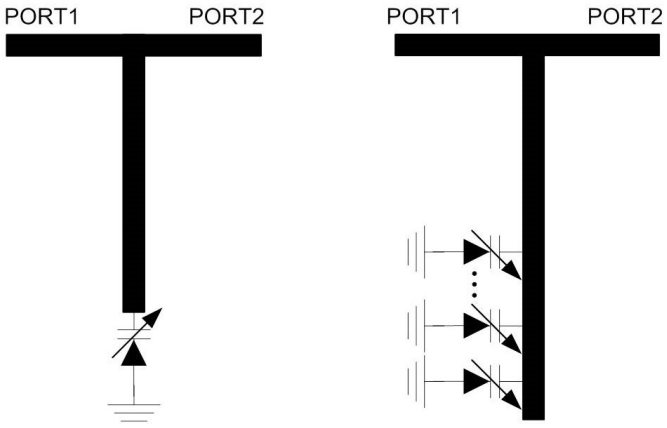
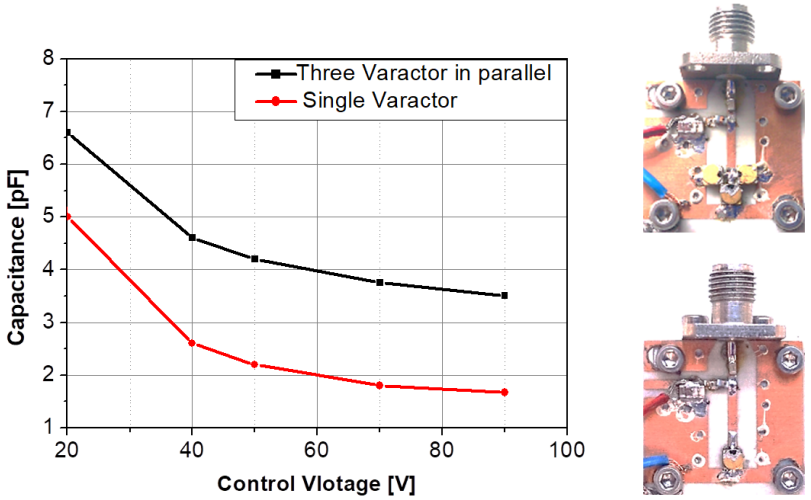


Figure 4.11: Tuning matching network topologies using semiconductor-based varactor diodes.

In this dissertation, a commercial silicon abrupt tuning varactor from Aeroflex Inc. (MRV40-90-H20) has been characterized [Paper E]. This varactor has a relatively high reverse voltage with 90 V, and device power dissipation of 250 mW at room temperature. Based on the Eq. 4.2, the more the tuning voltage, the more the tuning range of the capacitor. Moreover, to increase the capacitance value, more varactors can be connected in parallel. Fig. 4.12 illustrates the extracted capacitance value C_{Var} of single and three parallel varactors versus the control voltage V_{Con}. Ideally, the capacitance value of three parallel varactors should be three times that of the single varactor. However, the measurements show that the capacitance value of three parallel varactors is almost two times that of the single varactor, due to the parasitics and coupling between the varactors. Therefore, the tunability range of the single varactor (70 %) is higher than the three varactors in parallel (46 %).

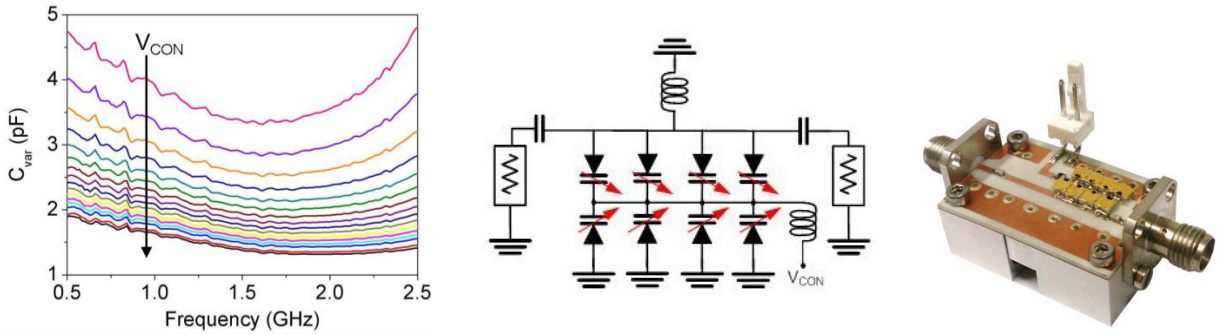


(a) (b)

Figure 4.12: (a) Capacitance value versus control voltage of single and three parallel varactors; (b) prototype of single and three parallel varactors fabricated circuit.

Furthermore, to improve the power handling performance of the varactors, an anti-series

topology has been designed and carried out. The schematic and a realized version of such a topology are shown in Fig. 4.13. This structure utilizes a series of varactors to improve breakdown voltage of the varactors and hence their power performance.



(a) (b) (c)

Figure 4.13: (a) Measured curve of the varactor capacitance versus control voltage and frequency for anti-series varactors topology; (b), (c) schematic and fabricated test fixture of 4×4 anti-series topology.

However, lumped capacitors are used in the reference prototype as modulation elements instead of the varactor-diode to have an accurate comparison between the two designs, due to the parasitics, coupling between the varactors, and not accurate models of the varactor-diode.

4.2.2 Source-/ load-pull analysis

To design the proposed PA, a 25 W GaN-HEMT packaged device (CGH40025F) [65] was selected as the active device. The first step in designing the PA was to characterize the transistor. The device was biased in class-AB mode with a drain voltage of $V_{DD} = 28$ V and a drain current of $I_{DQ} = 135$ mA.

A harmonic load-pull simulation setup was used to extract the optimum load impedances at the fundamental, second, and third harmonics of the transistor over the desired bandwidth at various output power levels. The extracted optimum load impedances should ensure a high PAE at various output power levels across the desired bandwidth.

The optimum output impedance varies with both power and frequency. When the power level drops from 44 dBm to 35 dBm, the desired impedance becomes more inductive as depicted in Fig. 4.14. In addition, the trajectory of the optimum load impedances at 1.8, 2.0, and 2.2 GHz at various output power levels are illustrated separately. Simultaneously, the real part of the optimum load impedance varies between 5 Ω and 14 Ω over the design band. Moreover, the Figure depicts the safe region of the second harmonic load impedances, where the PAE is reserved at maximum available value across the bandwidth at various output power levels. Consequently, load modulation of the output matching network is necessary to realize these different load impedances. The influence of the harmonics has been considered based on the presented analysis in Section 3.2.1.

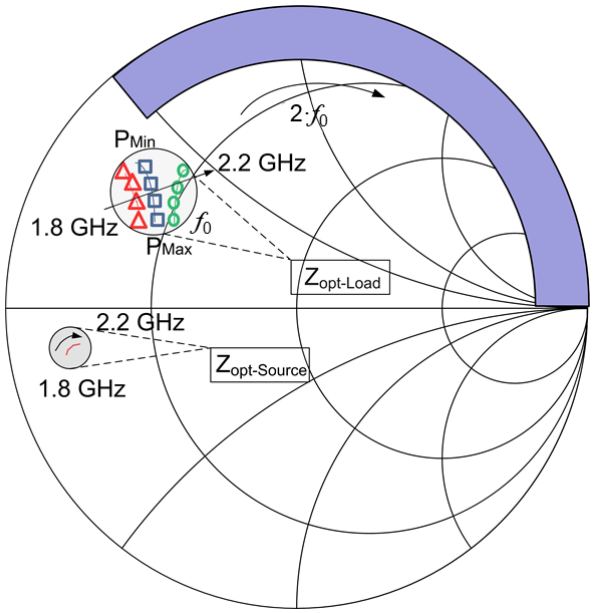


Figure 4.14: Optimum fundamental load impedances ($Z_{opt-Load}$) contours at 1.8, 2.0, and 2.2 GHz (triangles, squares, and circles respectively) at 44, 41, 38, and 35 dBm output power levels; 2^{nd} harmonic load impedances safe region (dark zone); optimum fundamental source impedances ($Z_{opt-Source}$) at maximum output power level (gray shaded circle) across the bandwidth.

To sum up this analysis, maintaining a high magnitude of the second harmonic load reflection coefficient and simultaneously avoiding operation at critical phase zones, near short-circuit termination, results in high efficiency performance of the PA over the desired bandwidth. The third and higher harmonics have not been considered during the design process due to their minor impacts. Finally, the optimum source impedances of the transistor were extracted in a similar analysis. Fig. 4.14 shows the optimum fundamental source impedances ($Z_{opt-Source}$) location range across the bandwidth.

4.2.3 Power amplifier realization

Based on the extracted impedances, the input matching network (IMN) was designed to ensure high and flat gain behavior over the whole bandwidth. The implemented IMN consists of stepped transmission lines and a single stub. An important factor regarding the design of the IMN was to obtain an unconditionally stable transistor operation, represented by stability factor K, which must be larger than unity over the whole frequency spectrum. Based on the study in Section 2.3, a series resistor was added at the input of the amplifier and bypassed by a capacitor to improve the stability at higher frequencies without causing a degradation of the gain across the bandwidth. Moreover, a parallel resistor was applied to the gate side to ensure the stability at lower frequency bands. Finally, an additional shunt RC network was added to the design to enhance the stability over the whole frequency spectrum. The goal of PA is to provide high efficiency at maximum output power and OBO levels across the desired band. Therefore, a TMN was required to change the load impedances according

to the output power levels. In this design, the OMN is tuned manually by replacing the capacitors according to the required output power level.

A multi-stage lowpass filter was used in the CAP-PA design. The OMN consists of three L-type matching networks in cascade, which is called a two-stage ladder matching network. The advantage of the ladder network over the π-topology network is that for higher impedance transformation ratios, the Q of a three-stage network is significantly lower and ensures a good matching across the bandwidth. However, this lower Q yields higher losses over the bandwidth. In this OMN, all lumped components were converted step by step to distributed components, with the exception of the two capacitors C_1 and C_2, as shown in Fig. 4.15 They were used to tune the PA to get the maximum available efficiency depending on the output power level.

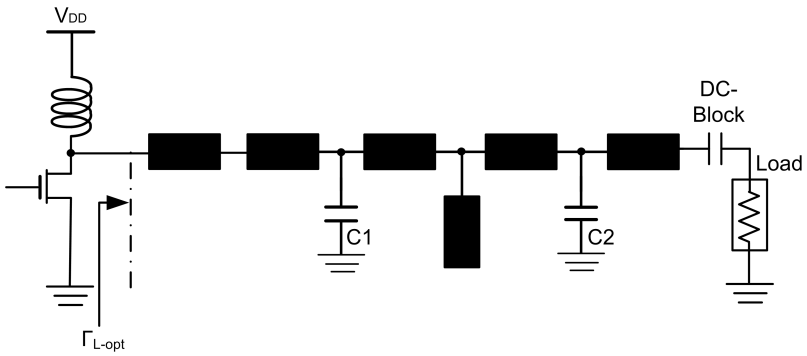


Figure 4.15: Circuit topology of the OMN of the CAP-PA.

Table 4.3 shows the required capacitance values at various output power levels. The table shows that C_1 can be fixed and converted to shunt stub based on simulation results. Nevertheless, it is more convenient to use a lumped component in order to further tune the design post production.

Table 4.3: Required capacitance values based on various output power levels over 1.8 - 2.2 GHz.

Pout [dBm]	**C_1 [pF]**	**C_2 [pF]**	**PAE [%]**	**efficiency [%]**
44	0.6	0.2	60 - 63	68 - 75
41	0.6	0.9	50 - 63.5	54 - 67
38	0.6	1.5	43 - 51	48 - 54
35	0.6	1.8	34 - 41	36 - 45
35	0.6	0.2	22 - 29	24 - 32

Based on these extracted values, the OMN was simulated and the reflection coefficient of the matching network at the drain reference plane was considered. Fig. 4.16 shows the reflection coefficient of the matching network by changing the capacitance values based on required output power from high to low level, respectively. The simulation results showed that the fundamental and the second harmonic response of the matching network were adjusted

in the safe region, as shown in Fig. 4.16. The large-signal simulation achieves 44 dBm as a maximum output power with efficiency between 68 % - 75 % using the appropriate capacitor values for maximum output power level. An enhancement in efficiency with almost 20 % at 9 dB output back-off power was simulated by setting the capacitances to the appropriate values at 35 dBm, as shown in Table 4.3.

The CAP-PA was realized on a Rogers 4003c ($\varepsilon_r = 3.55$) substrate with a thickness of 508 µm. Fig. 4.17 shows the prototype of the CAP-PA including the input-/output- matching network, stability circuit, and biasing circuit. The size of the realized PA is 8 cm × 5.5 cm.

The measurement results of this design are presented together with the next design in order to evaluate and compare the performance of the two designs.

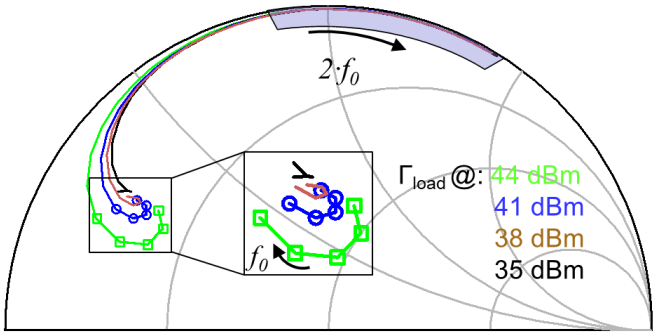


Figure 4.16: Γ_{Load} simulation results of the realized OMN changing capacitance values based on required output power levels at 44, 41, 38, and 35 dBm, (square, circle symbols, brown and black solid lines respectively) across [1.8 - 4.4] GHz; safe region of the second harmonic impedances.

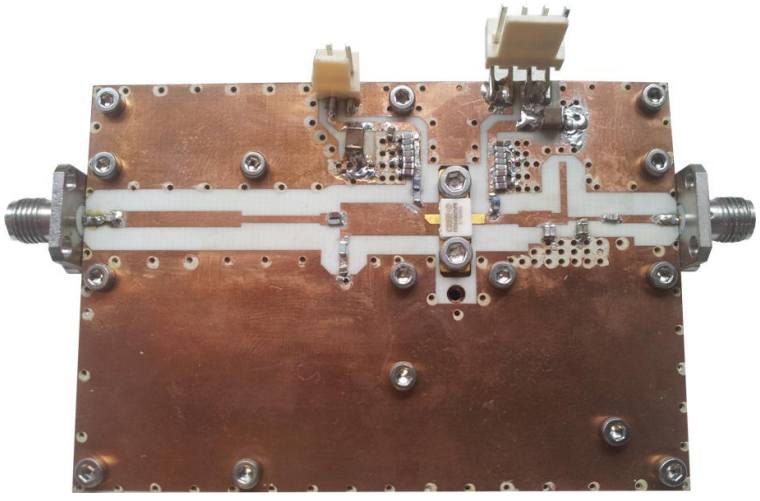


Figure 4.17: Prototype of the fabricated CAP-PA.

4.3 Wideband PA using barium-strontium-titanate based varactors (BST-PA)

The BST-PA tunability method was realized by changing the DC-control voltage of the BST-based varactor which resulted in changing the dielectric constant of the substrate. The main difference between the two designs is the tunability technique. The load was tuned electronically using BST-based varactors in this design. Fig. 4.18 presents the circuit topology of the BST based varactors.

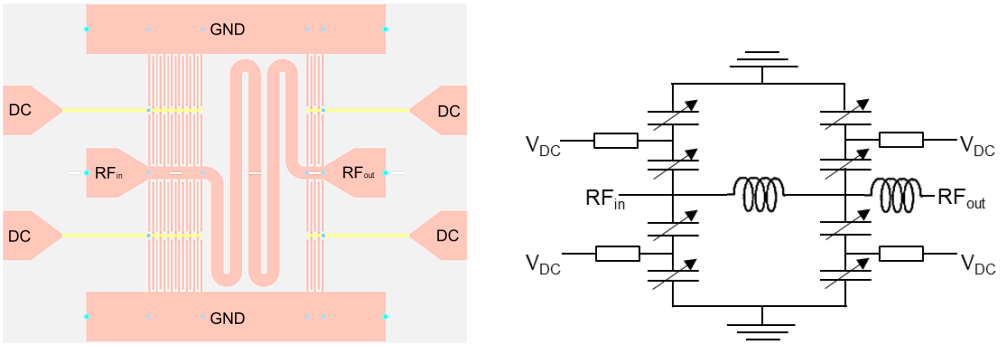


Figure 4.18: π-structure of BST based varactor tunable matching network using IDC.

BST has an E-field dependent dielectric constant, and hence allows the fabrication of electrically tunable interdigital capacitor varactors as depicted in Fig. 4.19. Moreover, BST has moderate insertion loss tan$\partial \approx 0.01$ in telecommunication frequency range and offers sufficient tunability τ(400 V) in the range of 40 % to 80 % depending on the technology and the tuning field applied. Here, the tunability is defined as capacitance change normalized to the un-tuned capacitance. The mathematical relationship between the bias voltage and the capacitance can be expressed based on Eq. 4.2 as follows:

$$C(V) = C(0) \cdot (1 - \tau(V))$$

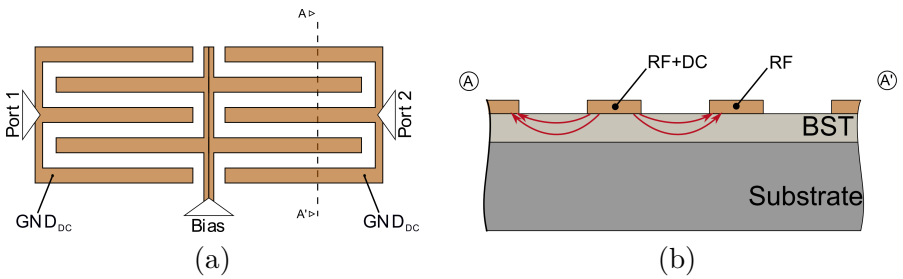


Figure 4.19: (a) Top view IDC varactor pair; (b) cross-section of the IDC with DC-bias-field penetrating the BST layer.

In this dissertation, the BST based varactor is also used as a part of the whole matching network of the PA. The matching network includes pre-matching to simplify the tunable

matching network and the BST based varactor, as shown in Fig. 4.20. More details about the design approach and the results will be presented later.

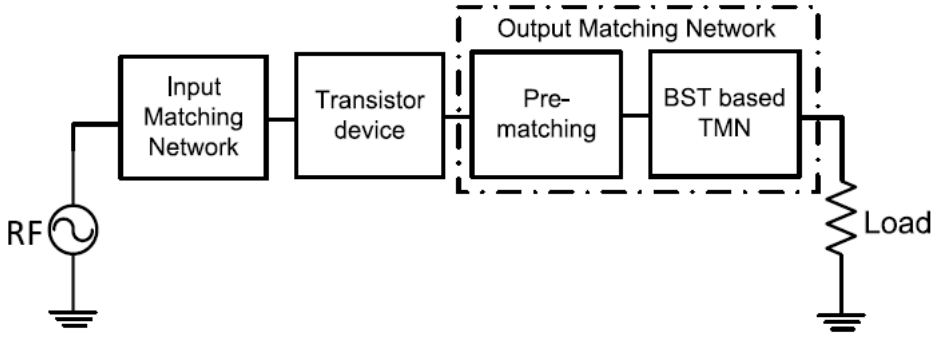


Figure 4.20: Block diagram of the power amplifier with implemented tunable matching network.

4.3.1 Characterization of BST-varactors

For the presented work, thick-film technology was chosen instead of thin-film technology, because of the better linearity performance. The production of BST, and the realization of tunable components based on BST thick-films was carried out in the Institute for Microwave Engineering and Photonics at Darmstadt University, Germany [83, 84]. The substrate preparation of the BST based varactor was carried out at the Karlsruhe Institute of Technology (KIT). The gaps of the IDC fingers were set to g = 15 µm, which is a compromise between linearity and tunability. The measured capacitance drop of IDC processed on top of a BST thick-film layer is depicted in Fig. 4.21. The Figure illustrates a measured tunability of $\tau(400\,\mathrm{V}) = 50\,\%$ which corresponds to an electrical field of 26 V/µm. Further increase in bias voltage can lead to higher tunability. However, it is limited by the breakdown voltage through the air, and can be extended further by passivation.

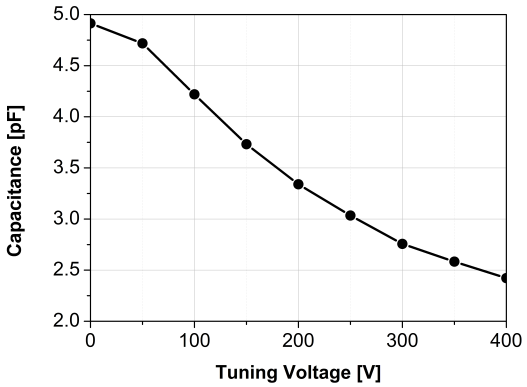
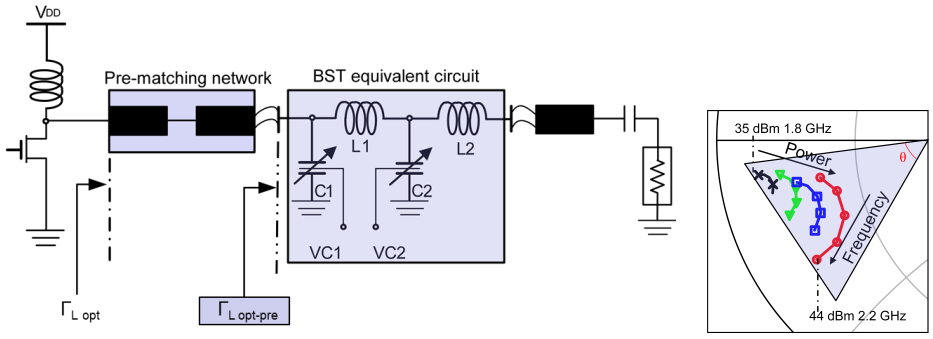


Figure 4.21: Tunability of an IDC with 15 µm finger gap.

4.3.2 BST-PA realization

Based on the extracted impedances in Section 4.2.2, the input matching network (IMN) was designed to ensure high and flat gain behavior over the whole bandwidth. Moreover, The IMN for this design had the same topology of the CAP-PA design to have a reasonable comparison between them. The goal of this PA is to provide high efficiency at maximum and OBO levels across the desired band. Therefore, a TMN was required to change the load impedances according to the output power levels. In this design, the OMN is tuned by adjusting the control voltage of the BST based TMN. The OMN considers just the fundamental load impedances, due to the limited tuning range in the BST as previously mentioned. The schematic of the OMN is presented in Fig. 4.22 and was realized through two steps. First, a fixed pre-matching network was required to overcome the tunability limitation of the BST and to realize a broadband matching network. The pre-matching network which consists of stepped transmission line Sections, shown in Fig. 4.22, was used to transform the low optimum load impedances of the transistor to the appropriate impedances for the BST based TMN. The Figure also shows the optimum load impedances of the pre-matching network ($Z_{opt-Pre}$) contours on the Smith chart at different output power levels of 44, 41, 38, and 35 dBm respectively over the desired band. Following that, the BST-based TMN structure should provide the required ($Z_{opt-Pre}$) over the design bandwidth, and transform them directly to 50 Ω. Fig. 4.22 illustrates the proposed circuit diagram of the TMN. The thick-film BST based TMN was controlled by changing the DC voltages of both shunt varactors to provide the appropriate pre-matched load impedances based on each output power level, as shown in Fig. 4.22. In this design, the required impedance area was relatively large as observed in Fig. 4.22. A high tuning control voltage range was therefore required to cover the whole required impedance range.



(a) (b)

Figure 4.22: (a) Circuit topology of the OMN of the BST-PA including pre-matching network and proposed circuit of the BST based TMN structure; (b) optimum pre-matching impedances ($Z_{Opt-Pre}$) values at various output power across the desired band.

- **Design and fabrication of the BST-based TMN**

Starting with the $Z_{opt-Pre}$ of the pre-matched PA as depicted in Fig. 4.22, a TMN was designed and fabricated on a functional layer of BST with a height of 3 µm. The mea-

sured tunability of the utilized material (Fe-F co-doped Ba0.4Sr0.6TiO3) exhibited tunability $\tau(400\,\mathrm{V}) = 50\,\%$ as mentioned previously. The design of the BST based TMN has been done in TU-Darmstadt with support from TU-Karlsruhe.

The thick-film technology in combination with high tuning voltages makes it possible to maintain the linearity of the whole design which was investigated in [85]. The detailed material properties and fabrication of the co-doped BST layers have been investigated and summarized in [87]. To overcome the limitation of breakdown through the air at high power and the high tuning voltage (higher than 400 V), the fabricated components were coated with a SU8 polymer photoresist, which sustains electrical fields larger than $400\,\mathrm{V/\mu m}$. Fig. 4.23(a) shows a photograph of the fabricated structure of the BST-based varactor along with its equivalent circuit. The initial values of the BST equivalent circuit at zero control voltage is shown in Table 4.4.

Fig. 4.23(b) shows the small-signal measurement results obtained at room temperature. The outer graph of the Figure shows the insertion loss extracted from generalized S-parameters at different tuning voltage levels [0 - 400] V. The inlay shows the input impedance on the Smith chart for different tuning values at different frequencies. Note that input impedances within the shaded areas can be continuously matched by varying the bias voltage between 0 V and 400 V. Detailed simulations and production processes can be found in [88]. The application of bias voltage progressively reduces the capacitance values down to 50 % of the initial value at a bias voltage of 400 V. For the small-signal measurements, voltages higher than 400 V were not applied to keep a safety margin since in large-signal operation the varactor has to face a combination of RF voltage and bias voltage. A further increase in bias-voltage subsequently leads to a slightly larger impedance transformation area than the one depicted in Fig. 4.23(b).

The broadband tunable PA was realized on a Rogers 4003c ($\varepsilon_r = 3.55$) substrate with a thickness of 508 µm. The size of the realized PA, shown in Fig. 4.24(a), is $8\,\mathrm{cm} \times 5.5\,\mathrm{cm}$. The substrate area around the TMN was gilded to ensure a stable contact between the BST and the rest of the output matching network. The TMN was bonded using gold bondwires as shown in Fig. 4.24(b). The influence of the bondwires was simulated to minimize its impact on the PA performance. The designed load modulated PA structure was completed using broadband bias tees with the same IMN and stability networks as in the CAP-PA design. The PA was finally optimized for high power and efficiency at maximum and 6 dB OBO power operations. The design was implemented to compare between BST-PA and CAP-PA performance.

Table 4.4: Initial values of the BST equivalent circuit.

$C_1(0)$ [pF]	$C_2(0)$ [pF]	L_1[nH]	L_2 [nH]
5.8	2.0	2.2	1.6

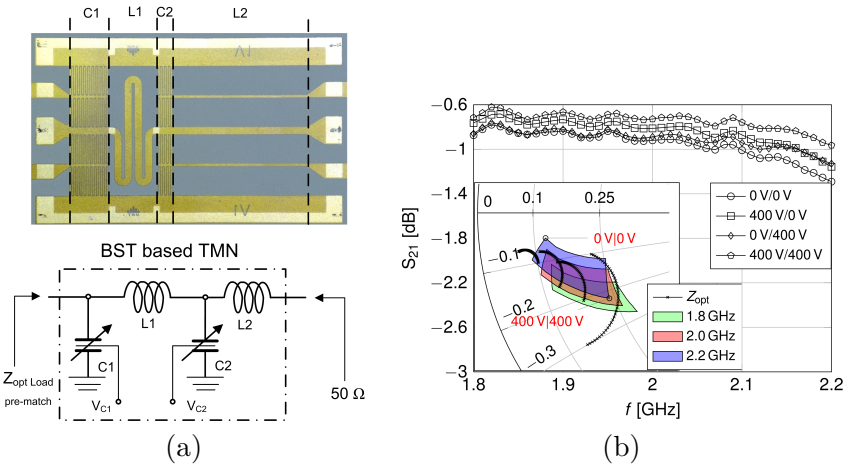


Figure 4.23: (a) Prototype and equivalent circuit of the BST-based varactor; (b) small-signal measurement results of the fabricated BST varactor.

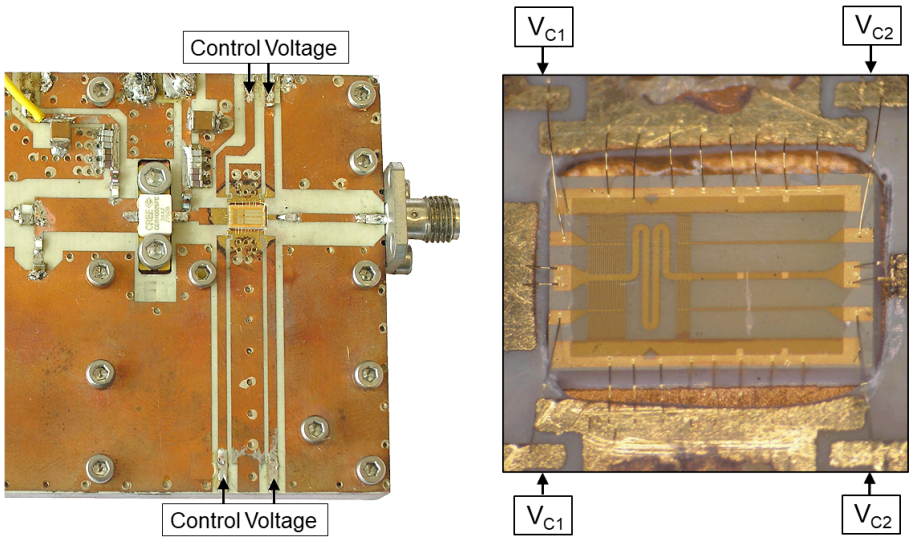


Figure 4.24: (a) Prototype of the fabricated BST-PA; (b) prototype of the fabricated BST based varactors.

4.3.3 Measurement results of CAP-PA versus BST-PA

- **Small-Signal measurements**

Both PAs were biased equally with V_{DD} = 28 V and I_{DQ} = 135 mA to measure the small-signal gain. The CAP-PA design showed a good agreement of small-signal gain with simulated results of 15 dB across the whole bandwidth. Fig. 4.25(a) heeds the small-signal gain of the BST-PA design. The Figure illustrates the comparison between the simulated and measured gain of the BST-PA design (solid line and square symbols respectively). The measured gain of the designed PA was shifted down in frequency from the simulated gain. The measured small-signal gain ranged between 11 and 15 dB across 1.6 - 2.0 GHz as shown in Fig. 4.25(a)

(square symbols). This frequency shift is due to the practical realization of the BST-PA. More precisely, the tolerance of the gap between the BST components and the main substrate as well as the height of the bondwires caused unpredicted extra bondwire inductances on both sides of the BST. These tolerances were simulated and specified to de-embed this frequency shift effect. The gap between the two substrates increased from 350 µm to approximately ~550 µm and the maximum height of the bondwires also increased from 150 µm to ~250 µm. These results in additional inductances on both sides of the BST structure with approximately 0.3 nH are shown in Fig. 4.25(b). This unavoidable inductance caused a 200 MHz frequency shift to lower frequency band compared to the targeted bandwidth. Consequently, all measurement results of the BST-PA design were shifted to compensate this frequency shift and allowed a detailed comparison between both designs.

Fig. 4.25(a) shows the measured de-embedded small-signal gain (circle symbols). The measured results of the BST-PA were presented based on the prescribed de-embedding technique. However, higher insertion loss of the implemented BST as well as additional inductances degraded the small-signal gain at higher frequencies as shown in Fig. 4.25(b).

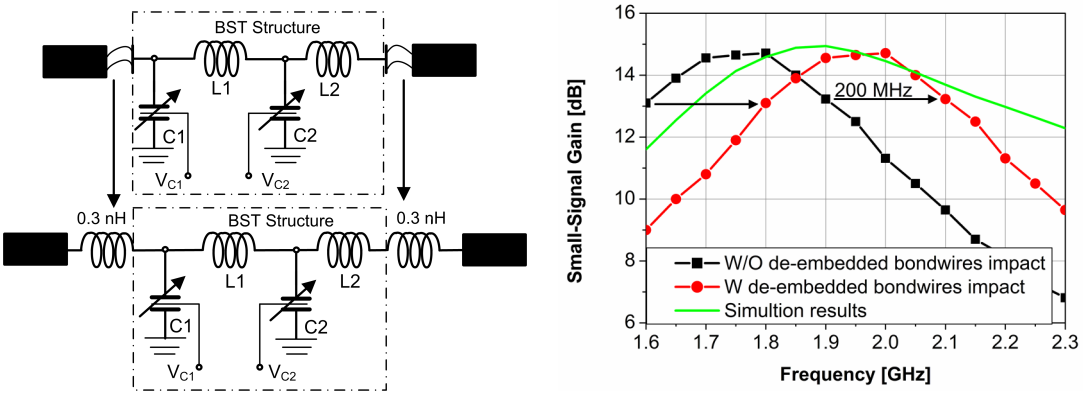


Figure 4.25: (a) De-embedding of the bondwire influences with two inductors; (b) small-signal measurement of the frequency shifted BST-PA design.

- **Large-Signal measurements**

A continuous wave (CW) input signal was used to perform the large-signal measurements. After determining the optimum drain bias of both PAs, the sensitivity of the PA performance against the gate bias voltage V_{GS} was evaluated by applying different gate-bias voltages. The output power and efficiency were measured for each gate voltage. It was observed that the performance could further be optimized by additionally tuning the gate bias voltage. Therefore, the large-signal measurements were performed for both designs in class-C mode with a gate bias voltage of V_{GS} = -4 V and a drain bias voltage of V_{DD} = 28 V. This bias point definitely results in higher PAE at OBO power levels compared to the class-AB operation, due to the less power consumption in class-C mode. However, at the maximum output power level, the efficiency is slightly lower than that of the class-AB mode, due to the lower gain at maximum level compared to class-AB. Experimentally, Fig. 4.26 shows the PAE performance of the CAP-PA design in class-AB and class-C mode at maximum and 6 dB OBO power levels.

At 6 dB OBO power level, the measurements were done twice under two different settings of capacitors. The first one has used the original setting of capacitors, 44 dBm capacitors setting. The second has used the 6 dB OBO power level capacitors setting based on Table 4.3 across the desired band. The results demonstrated a slight difference in PAE performance between the two modes of operation at maximum output power level. However, at 6 dB OBO level, the PAE performance in class-C mode was better than that in class-AB mode in spite of the lower gain. This could be attributed to the higher efficiency performance, due to the less power consumption at back-off level. Moreover, the Figure shows as well that the PAE at 6 dB OBO was enhanced by almost 20 % using appropriate capacitors setting.

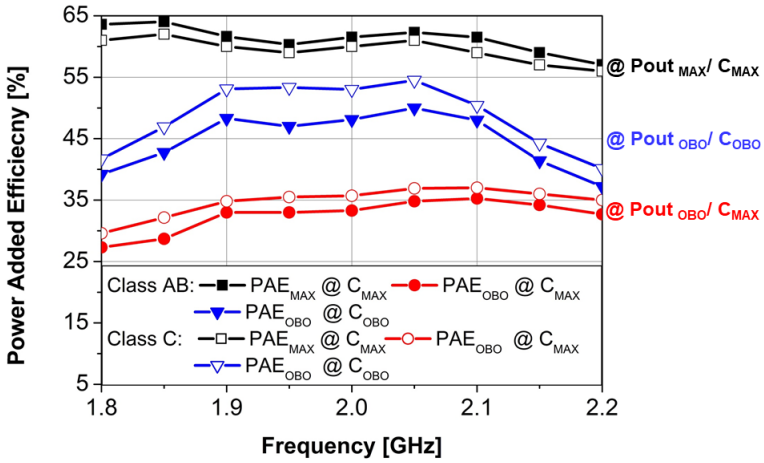


Figure 4.26: Measured PAE at Pout_{MAX} and $\text{Pout}_{6dB-OBO}$ in class-AB (filled symbols) and class-C (empty symbols) mode; at C_{MAX} setting: Pout_{MAX} (black), $\text{Pout}_{6dB-OBO}$ (red); at $\text{C}_{6dB-OBO}$ setting: $\text{Pout}_{6dB-OBO}$ (blue) of CAP-PA.

- **Maximum output power level performance**

Fig. 4.27 shows the performance of both designs at maximum output power level. In the CAP-PA, the capacitors were adjusted to get maximum output power with high efficiency over the desired bandwidth. Fig. 4.27(a) shows the maximum measured output power of 44.5 dBm with drain efficiency of 65 % and a gain of more than 11 dB across the bandwidth. Moreover, the BST-PA design measurement results are presented in Fig. 4.27(b). The maximum drain efficiency at maximum output power was sensitive to the control voltage of the BST (V_{C1} and V_{C2}). It was realized that the performance could further be enhanced by increasing the control voltage to $V_{C1} = V_{C2} = 450\,V$, where the BST based TMN could involve more range of the required $\text{Z}_{opt-Pre}$ at maximum output power across the band. The Figure shows that the design had a maximum output power of 44 dBm with maximum drain efficiency of 70 % and a gain of 9 dB. Fig. 4.27(b) also shows a degradation in performance at higher frequencies. This deviation might be caused due to the increase of losses in BST based TMN structure and the additional bondwire inductances on both sides of the BST as mentioned previously.

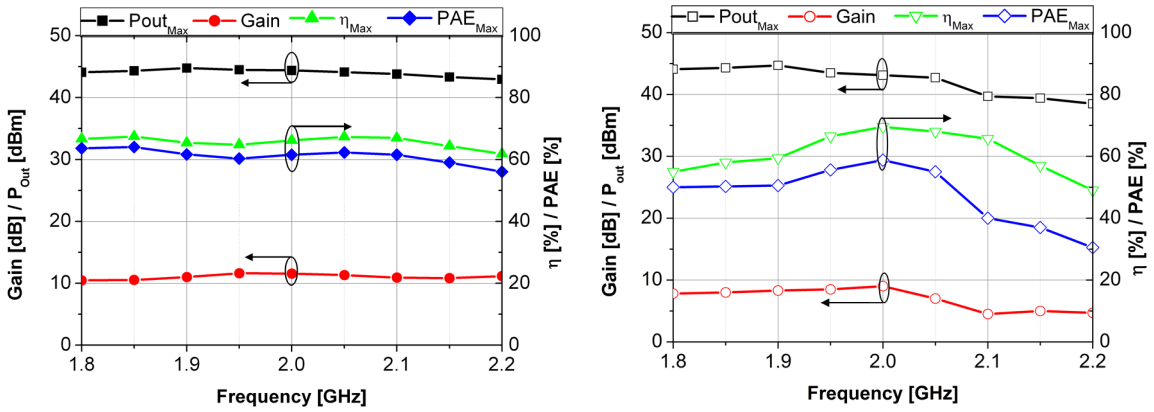


Figure 4.27: Large-Signal measurement results at maximum output power level versus the frequency; (a) CAP-PA at ($C_1 = 0.6$ pF, $C_2 = 0.2$ pF); (b) de-embedded BST-PA at ($V_{C1} = V_{C2} = 450$ V).

- **Drain efficiency evaluations**

The comparison between the two designs in drain efficiency at maximum as well as at 6 dB OBO level with and without tuning the load was evaluated. Fig. 4.28(a) shows the efficiency of the CAP-PA. The capacitance values of the OMN were adjusted according to Table 5.1 in order to ensure maximum available output power with maximum efficiency. The measured efficiency ranged from 61 % to 69 % (filled triangle symbols). However, at 6 dB OBO level and without tuning the load impedances, the efficiency degraded to 32 % - 40 % (filled square symbols). Tuning the load impedances of the OMN by adjusting the capacitance value according to Table 4.3, the efficiency could be enhanced to 45 % - 60 % (filled circle symbols). In other words, 8 % to 20 % of efficiency enhancement in efficiency at 6 dB OBO range was achieved by adjusting the capacitance value of the OMN (filled diamond symbols) across the bandwidth.

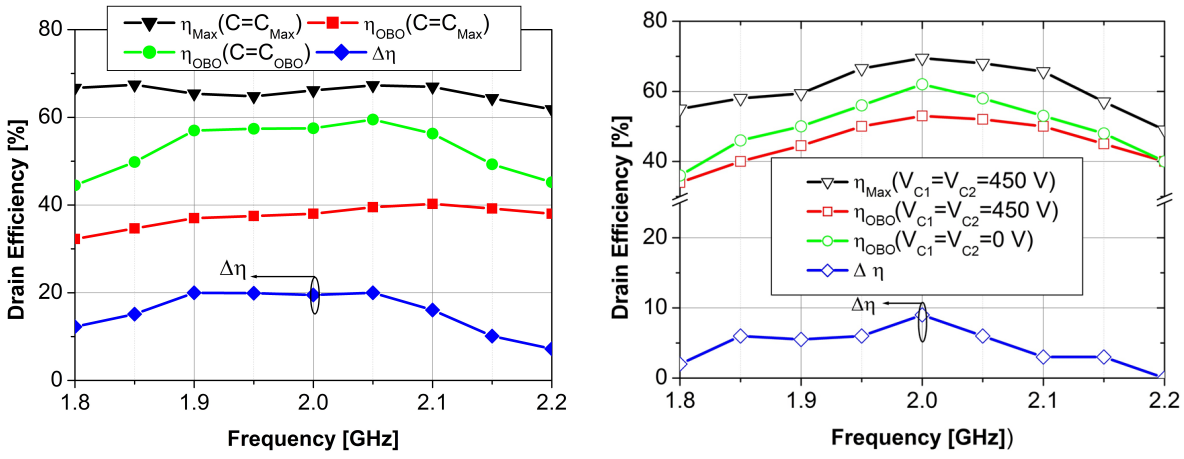


Figure 4.28: Efficiency performance of (a) CAP-PA; (b) de-embedded BST-PA at Pout_{MAX} (triangle symbols); at $\text{Pout}_{6dB-OBO}$ with and without tuning load impedances (circle symbols) (square symbols) respectively; efficiency improvement (diamond symbols).

Fig. 4.28(b) illustrates the drain efficiency performance of the BST-PA at maximum output power and 6 dB OBO power level with two different control voltages of BST-based varactor across the whole band. The measured efficiency at maximum output power level ranged from 50 % to 70 % (hollow triangle symbols) at $V_{C1} = V_{C2} = 450\,V$. However, at the same TMN control setup, the 6 dB OBO level efficiency degraded to 35 % - 52 % (hollow square symbols). To improve the drain efficiency over the whole band, the control voltages V_{C1} and V_{C2} were readjusted to achieve the maximum available efficiency at 6 dB OBO level. Consequently, the bias voltages were tuned to ($V_{C1} = V_{C2} = 0\,V$) to achieve the optimum load impedances at the 6 dB OBO range. As shown in Fig. 4.28(b), the enhancement in efficiency was between 2 % and 9 % over the whole bandwidth (hollow diamond symbols). The improvement in drain efficiency of the BST-PA was lower than the CAP-PA. Moreover, at 6 dB OBO range, the efficiency performance of the BST-PA was significantly better than the efficiency performance of CAP-PA at the maximum setup for both designs. This could be due to the BST thermal sensitivity which will be introduced later.

The final comparison of efficiency performance between the two designs versus the frequency is presented in Fig. 4.29(a). The OMNs in both designs were adjusted for maximum output power setup to ensure a maximum drain efficiency:

- In CAP-PA, the capacitance values were chosen based on Table 4.3.
- In BST-PA, the control voltages were adjusted to $450V$.

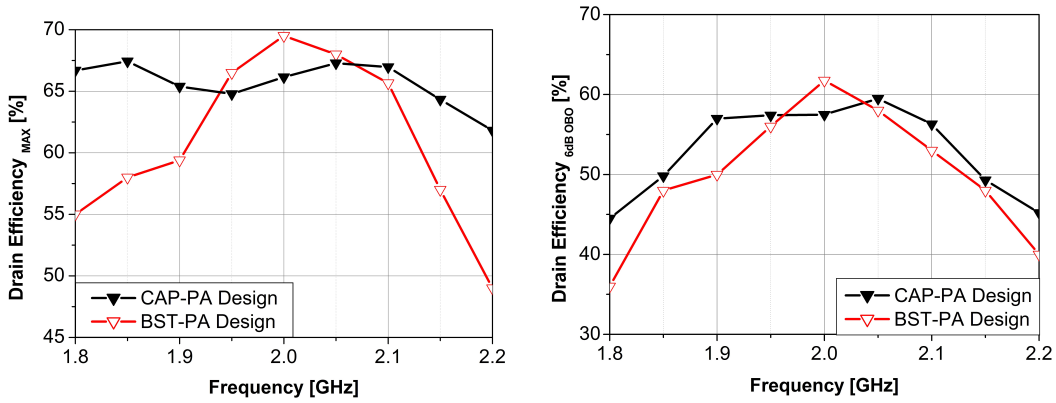


Figure 4.29: Drain efficiency performance comparison of CAP-PA and de-embedded BST-PA: (a) at Pout_{MAX}; (b) at $\text{Pout}_{6dB-OBO}$ with tuning the load impedances.

The maximum efficiency of the CAP-PA was constant and higher than 62 %, whereas the efficiency of the BST-PA ranged between 48 % and 69 % across the bandwidth. The significant degradation of efficiency at 2.1 GHz to 2.2 GHz was caused by the increase of the insertion loss of the BST structure and the additional bondwire inductances, as mentioned previously. The OMNs of both designs were tuned to achieve maximum drain efficiency at 6 dB OBO level. Fig. 4.29(b) shows the efficiency at 6 dB OBO of both designs. It is deployed that there was a good agreement between the two PAs regarding the efficiency enhancement. The fixed

CAP-PA had a back-off efficiency ranging between 45 % and 60 %, and the BST-PA efficiency ranged from 38 % to 62.5 % across the desired band.

Fig. 4.30 shows the drain efficiency performance of both designs versus the output power sweep at the center frequency 2.0 GHz. As previously mentioned, there was an enhancement in drain efficiency performance by accommodating the OMN based on the required output power level. In the BST-PA, an enhancement of 12.5 % was achieved by readjusting the control voltages of the BST structure at 6 dB OBO power level, whereas in the CAP-PA design, the efficiency performance was enhanced by 19 % through adjusting the capacitance values based on Table 4.3. Moreover, at 9 dB OBO, a clear efficiency enhancement was achieved in both designs. The BST-PA had an efficiency of 40 % at maximum setup ($V_{C1} = V_{C2} = 450\,V$) of the control voltage, where it was enhanced to 50 % by changing the control voltage to minimum setup $V_{C1} = V_{C2} = 0\,V$.

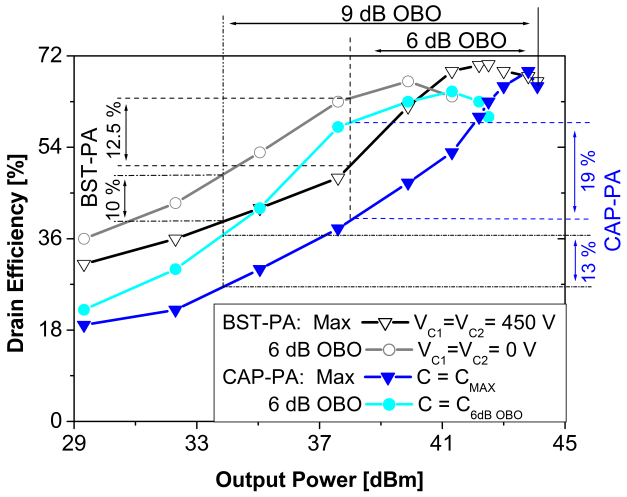


Figure 4.30: Drain efficiency performance at (2.0 GHz) of CAP-PA and de-embedded BST-PA versus the output power sweep at maximum setup and 6 dB OBO setup.

Fig. 4.30 also illustrates that the BST-PA also shows a better efficiency performance at OBO levels without re-tuning the control voltage, compared to the CAP-PA which degrades dramatically. This effect is most likely related to the effect of self-heating described in [89]. At back-off power level, the dissipated power is smaller, as such the equilibrium of heating and cooling is found at a lower temperature. The decrease in RF-induced temperature has the same effect on the dielectric constant as the reduction external electrical field. However, this thermal tuning of the varactor is low compared to the electrical tuning and therefore further investigation is directed towards the reduction of RF against thermal coupling.

5 Summary and Conclusion

This dissertation has mainly considered the most important and challenging components in the radio base station. It has presented various design techniques to improve the bandwidth of operation and efficiency of PAs used in modern wireless communication systems. It has proposed a novel approach for designing a high peak efficiency single-ended power amplifier. The interesting bandwidth of operation of the designs is ultra high frequency (UHF)-band, L-band, and S-band. Monte-Carlo and electromagnetic simulations were performed in order to ensure that the designs were reliable.

For a broadband PA, a design methodology for a single-ended power amplifier with bandwidth ranges between 1.7 to 2.3 GHz was presented and verified. The method is based on a harmonic tuning approach combined with a systematic design of broad matching networks. The amplifier achieved 70 % - 76 % power-added efficiency with an output power range of between 43.5 to 45 dBm.

Extending the bandwidth to more than an octave while maintaining high efficiency was investigated using the adapted approach of harmonically tuned ultra-wideband power amplifier for extracting the optimum load impedances across the desired bandwidth. For this approach, an ultra-wideband PA was proposed and a harmonically tuned power amplifier operating between 1.1 and 2.7 GHz was implemented. This investigation resulted in a highly efficient wideband power amplifier with a power-added efficiency between 60 % - 72 %. This approach has been integrated with a broadside coupled transformer to further expand the bandwidth of operation. As a result, a multi-octave amplifier was presented with a bandwidth of 0.5 - 2.7 GHz. The broadside coupled transformer was used for the first time as the main part of the matching network instead of the commonly used multi-stages low-pass band filter. Using this transformer has reduced the even mode impedances influence of the microstrip lines. The investigation has demonstrated the proposed setup as an important tool for understanding and optimizing the PA and broadside coupled transformer for ultra-wideband harmonically tuned PAs. The design achieved a power-added efficiency range between 50 % - 65 % across the desired bandwidth. Under the same bandwidth of operation, the last design has been demonstrated with four times higher output power for high output power transmitters. Unlike in previous designs, a larger transistor was used here. This presents an additional challenge, due to the low optimum source-/load-impedances of the large transistor. This adds complexity to the matching network design. A detailed analysis of each passive structure integrated into the design was introduced, leading to the state-of-the-art results for ultra-wideband, high power amplifiers, as presented in Table 1.1.

For a transmitter with broadband and high efficiency at various peak-to-average power ratio, the load modulation technique was the used methodology to provide different optimum load impedances based on the output power level. The passive load modulation technique

was used in this dissertation for achieving this target. A detailed analysis of the tunable matching network was considered.

The first design was demonstrated as a reference to prove the usability of using this technique across 1.8 to 2.2 GHz. Where discrete elements were used to improve the efficiency at each output power level. Various varactor technologies were configured and modeled to characterize them. The common challenging issue in all varactor types was the limited tunable and power handling range. Anti-series circuit topology was a beneficial solution in expanding the tuning range of the varactor.

The second design used a barium strontium titanate (BST)-based varactor for the first time as the main part of the matching network. The results of this design show a promising performance, which can be developed to use the BST based varactor mainly in the matching network design. The two designs achieved a comparable performance with state-of-the-art results in this domain using load modulation technique for improving the efficiency, as presented in Table 1.2.

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List of publications

Appended papers

This dissertation is based on the following papers:

[A] **M. T. Arnous**, P. Saad, S. Preis and Zihui Zhang, "Highly efficient and wideband harmonically tuned GaN-HEMT power amplifier," 2014 20th International Conference on Microwaves, Radar and Wireless Communications (MIKON), Gdansk, 2014, pp. 1-4.

[B] **M. T. Arnous**, S. E. Barbin and G. Boeck, "Design of multi-octave highly efficient 20 Watt harmonically tuned power amplifier," 2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON), Krakow, 2016, pp. 1-4.

[C] **M. T. Arnous**, Z. Zhang, S. E. Barbin and G. Boeck, "A Novel Design Approach for Highly Efficient Multioctave Bandwidth GaN Power Amplifiers," in IEEE Microwave and Wireless Components Letters, vol.27, no.4, 2017, pp. 371-373

[D] **M. T. Arnous**, Z. Zhang, F. Rautschke, and G. Boeck, "Multi-Octave bandwidth, 100 Watt GaN power amplifier using planar transmission line transformer," International Journal of Microwave and Wireless Technologies, 2017, vol.9, no.6, pp.1261-1269.

[E] **M. T. Arnous**, Z. Zhang, S. E. Barbin and G. Boeck, "Characterization of high voltage varactors for load modulation of GaN-HEMT power amplifier," 2015 17th International Conference on Transparent Optical Networks (ICTON), Budapest, 2015, pp. 1-4.

[F] **M. T. Arnous,** A.Wiens, P. Saad, S. Preis, Z. Zhang, R. Jakoby, and G. Boeck, "Evaluation of GaN-HEMT power amplifiers using BST-based components for load modulation," International Journal of Microwave and Wireless Technologies, 2014, vol.6, no.3/4, pp. 253–263.

Other papers and publications

The following publications are not appended to the dissertation, either due to contents overlapping that of appended papers, or due contents not related to the dissertation.

- **M. T. Arnous**, Z. Zhang, F. Rautschke and G. Boeck, "Multi-octave GaN high power amplifier using planar transmission line transformer," 46th European Microwave Conference (EuMC), London, 2016, pp. 580-583.

- **M. T. Arnous**, A. Wiens, S. Preis, H. Maune, K. Bathich, M. Nikfalazar, R. Jakoby and G. Boeck, "Load-modulated GaN power amplifier implementing tunable thick-film BST components," 2013 European Microwave Conference, Nuremberg, 2013, pp. 1387-1390.

- **M. T. Arnous**, K. Bathich, S. Preis and G. Boeck, "Harmonically-tuned octave bandwidth 200 W GaN power amplifier," 2012 7th European Microwave Integrated Circuit Conference, Amsterdam, 2012, pp. 429-432.

- Z. Zhang, **M. T. Arnous** and G. Boeck, "Ultra-broadband GaN power amplifier utilizing planar Guanella transformer," 2015 17th International Conference on Transparent Optical Networks (ICTON), Budapest, 2015, pp. 1-4.

- S. Preis, **M. T. Arnous**, Z. Zhang and W. Heinrich, "Linearity analysis of class-B/J continuous mode power amplifiers using modulated wideband signals," 2015 German Microwave Conference, Nuremberg, 2015, pp. 5-8.

- S. Preis, Z. Zhang and **M. T. Arnous**, "Design of a GaN-HEMT power amplifier using resistive loaded harmonic tuning," 2014 9th European Microwave Integrated Circuit Conference, Rome, 2014, pp. 552-555.

- A. Wiens, **M. T. Arnous**, H. Maune, M. Sazegar, M. Nikfalazar, C. Kohler, J. R. Binder, G. Boeck and R. Jakoby, "Load modulation for high power applications based on printed ceramics," 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, WA, 2013, pp. 1-4.

- K. Bathich, **M. T. Arnous** and G. Boeck, "Design of 200 W wideband Doherty amplifier with 34 % bandwidth," 2013 European Microwave Conference, Nuremberg, 2013, pp. 279-282.

- S. Preis, **T. Arnous**, Z. Zhang, P. Saad and G. Boeck, "Bandwidth versus efficiency performance using power combining in GaN-HEMT power amplifiers," 2013 European Microwave Conference, Nuremberg, 2013, pp. 696-699.

- **M. T. Arnous** and G. Boeck, "4 Watt, 45 % bandwidth Si-LDMOS high linearity power amplifier for modern wireless communications systems," 2012 2nd International Conference on Advances in Computational Tools for Engineering Applications (ACTEA), Beirut, 2012, pp. 110-113.
- **M. T. Arnous**, K. Bathich, S. Preis, D. Gruner and G. Boeck, "100 W highly efficient octave bandwidth GaN-HEMT power amplifier," 2012 19th International Conference on Microwaves, Radar & Wireless Communications, Warsaw, 2012, pp. 289-292.

Summary of Appended Papers and Awards

Summary of Appended Papers

Paper A

Highly efficient and wideband harmonically tuned GaN-HEMT power amplifier

In this paper, the design of a highly efficient 25 W GaN-HEMT power amplifier (PA), operating in 1.7 - 2.3 GHz, is presented. The influence of the harmonics and the impact of the parasitic components of the nonlinear device are considered in order to ensure an accurate matching network design to achieve high efficiency. Optimum fundamental and harmonic load impedances were obtained using load-pull simulations across the operation band. From continuous wave large-signal measurements, an average output power of 44 dBm was obtained over the bandwidth. The corresponding drain efficiency ranged between 73 % - 80 % with a gain of 12 dB. Linearized modulated measurement, using 10 MHz LTE signal with 7.3 dB peak-to-average power (PAPR), shows an average power-added efficiency (PAE) of 38.2 % and adjacent channel leakage ratio (ACLR) of almost -45 dBc at 1.8 GHz.

Paper B

Design of multi-octave highly efficient 20 Watt harmonically tuned power amplifier

In this contribution, the design, implementation, and experimental results of a highly efficient, multi-octave bandwidth power amplifier (PA) using a 25 W packaged GaN-HEMT are presented. source-/load-pull setup is used to extract the optimum source-/load-impedances across 1.1 - 2.7 GHz. The harmonics impact is considered to improve the power amplifier efficiency. Utilizing the characteristics of FET transistor leads to modify the optimum fundamental load impedances of the low frequency range, which have higher gain compared to high frequency range, and minimize the influence of the higher harmonics. This method results in a measured minimum output power of 43 dBm with a drain efficiency ranged between 65 % to 75 % and a flat gain of 10.5 $\pm$1 dB over the desired band.

Paper C

A Novel design approach for highly efficient multi-octave bandwidth GaN power amplifiers

This work presents a novel approach to design highly efficient multi-octave bandwidth power amplifiers (PAs). The fundamental load impedances are slightly detuned out of their optimum values to reduce the in-band harmonics influence on output power and power-added efficiency. The design of the output matching network includes a 4:1 planar Guanella transformer for wide bandwidth and low complexity. In the frequency band 0.5 - 2.7 GHz, the PA achieves 10.2 ± 1.6 dB power gain and more than 20 W output power. The drain efficiency varies from 56 % to 70 % over the bandwidth.

Paper D

Multi-octave bandwidth, 100 W GaN power amplifier using planar transmission line transformer

In this paper, design, implementation, and experimental results of efficient, high-power, and multi-octave gallium nitride-high electron mobility transistor power amplifier are presented. To overcome the low optimum source/ load impedances of a large transistor, various topologies of a broadside-coupled impedance transformer are simulated, implemented, and measured. The used transformer has a flat measured insertion loss of 0.5 dB and a return loss higher than 10 dB over a decade bandwidth 0.4 - 4 GHz. The transformer is integrated at the drain and gate sides of the transistor using pre-matching networks to transform the complex optimum source-/load-impedances to the appropriate impedances of the transformer plane. The measurement results illustrate a saturated output power ranged between 80 and 115 W with an average drain efficiency of 57 % and gain of 10.5 dB across 0.6 - 2.6 GHz.

Paper E

Characterization of high voltage varactors for load modulation of GaN-HEMT power amplifier

In this work, a semiconductor varactor and a ferroelectric varactor, used for designing load modulation power amplifiers, are compared. The semiconductor varactor has used silicon hyperabrupt technology. It shows considerable advantages in terms of tuning range, tuning voltage, tuning speed, and losses in comparison to the ferroelectric varactor, which has used a thick-film Barium Strontium Titanate (BST) device. A fixed matching network power amplifier (FMN-PA) was fabricated in order to enable comparisons with a previously designed tunable matching network (TMN) load modulation PA based on BST. Both PAs are driven in class-C, operate at 1.8 GHz and use a GaN-HEMT. The maximum measured drain efficiencies for the FMN-PA and TMN-PA are 79 % and 69 % at the maximum output power of 43 dBm. At 6 dB back-off output power the efficiencies are 45 % and 62 %, respectively, after controlling the bias voltage for the TMN case. Better performance for the TMN-PA is achievable using the semiconductor varactor according to the obtained characterization results of this work.

Paper F

Evaluation of GaN-HEMT power amplifiers using BST-based components for load modulation

In this paper, the concept of load-modulated power amplifiers (PAs) is studied. Two GaN-HEMT PAs, targeted for high efficiency at maximum and output-back-off (OBO) power levels, are designed, implemented, and tested across 1.8 - 2.2 GHz. The load modulation in the first design is realized by tuning the shunt capacitors in the output matching network. A novel method is employed in the second design, where barium–stronrium–titante is used for the realization of load modulation. The large-signal measurement results across the desired band show 59 % - 70 % drain efficiency at 44 - 44.5 dBm output power for both designs. Using the available tunable technique, the drain efficiency of the PAs is enhanced by 4 % - 20 % at 6 dB OBO across the bandwidth.

Contribution awards

- **"IEEE MTT- S Young Scientist Contest Prize"** of the 20th international conference on microwave, radar and wireless communications (MIKON), June 16-18, 2014, Gdansk, Poland.
- **"Student Design Competition Award"** for a Microwave Power Amplifier Design, German Microwave Conference (GeMiC), March 16-18, 2015, Nuremberg, Germany.
- **"Young Scientist Contest Distinction Award"** at the 21st international conference on microwave, radar and wireless communications (MIKON), May 9-11, 2016, Krakow, Poland.