Contact resistance effects in thin film solar cells and thin film transistors

by

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Chapter 1

Introduction

Thin film technology is the keystone in the modern applied science and it has been used for several decades in making electronic devices, optical coatings, decorative parts, etc. A thin film stands for a layer of material deposited on a metal, semiconductor or ceramic base. The base, the substrate, of the thin film device, is mostly used as a mechanical support for thin films. Usual thickness of such layers never exceeds several microns, and they can be with conductive or dielectric properties. Thin film materials and deposition techniques have been summarized at [1]. In early 1960s, the first thin film transistor was proposed [2], and in the 1970s several novel thin film devices were proposed, including the thin film surface acoustic wave (SAW) devices [3], the integrated thin film bulk acoustic wave (BAW) devices [4], and thin film integrated optics [5]. Technological improvements and outstanding material science research has paved the way for today's thin films to be utilized in high precision resistors, SAW devices, optical disks, sensors, active matrices for liquid crystal TVs, to name but a few. As a result of increasingly higher demands for more energy and more cost effective electrical devices, the utilization of thin films has additionally been expanded to other industries, such as a usage in photovoltaics, printable electronics, and organic electronic devices. In recent decades, researches on various thin film solar cells and organic electronic devices have pioneered improvements in performance and miniaturization. As devices further miniaturize, performance of thin film transistors suffers as a result of high electrical Ohmic losses which occur. In thin film devices, such as solar cells, radio frequency identification tags (RFIDs) and thin film transistors, the main contributor to high parasitic losses is the contact resistance between metal electrodes and active semiconductor materials.

Further performance improvements in these devices are only possible by reducing the contact resistance.

Contact resistance occurs every time two or more bodies are in contact, and as a result of contact resistance, the system will perform with losses in electrical, thermal and mechanical properties. Elements that affect electrical contacts properties are: contact surface topography, apparent and real contact areas, and materials that comprise the junction.

The surfaces of materials in devices are not inherently smooth due to manufacturing operations and/or the nature of the material. Surface roughness may incur higher contact resistance, and may be responsible for variable growth of material layers deposited at a later time.

The contact between two rough materials often exhibits higher contact resistance, often because the real contact area between the materials is smaller than the apparent contact area. By improving the surface roughness, or perhaps by reducing the number of surface voids on the contact interface, one may lower contact resistance.

Finally, the contact resistance differs in cases where bulk materials are utilized in devices, as in the case when devices and contacts are formed between thin films. The current transport in these types of devices occurs in different manners that may incur gradients in the contact resistance.

Contact resistance effects in electrical devices are undesirable, but unavoidable. The minimization of these effects on a device's functionality has drawn the attention of many researchers from various fields.

In the classical c-Si photovoltaic industry, contact effects are not a prominent issue due to the high processing temperatures utilized in the fabrication steps. On the other hand, in thin-film photovoltaic industry, the process temperature is one of the limiting parameters for the formation of electrical contacts, especially in the case of devices manufactured on plastic substrates. Due to the high contact resistance, conversion efficiency of the thin film solar cells may be affected.

Furthermore, transistors have been the engine of the electronic revolution. As new areas of thin film devices continue to expand, new and different materials have been under investigation for the manufacturing of thin film transistors. On account of miniaturizing devices, contact effects have become a prominent factor on a device's

performance. Contact effects may reduce the charge carrier mobility of the devices, as well as the switching frequency in thin film transistors [6]. Lastly, in the past two decades, organic materials have been in vogue with respect to thin film research, particularly in organic electronics. Daily improvements in material properties are increasing the mobility of devices, but with further miniaturization the contact effects may be the limiting factor towards practical implementation of organic electronic devices.

1.1 This thesis

This thesis deals with the electrical contact effects in two different types of thin film devices: thin film solar cells and thin film transistors. Although they are operating on different principles, due to the lateral transfer of electrical current in these devices, the contact effect problem is similar for both types of devices. The basic principle of lateral current transport and the general electrical properties of metal-semiconductor contacts are presented in Chapter 2.

The first part of the thesis deals with the contact effect in thin film solar cells, particularly chalcopyrite based solar cells. The basic principles of the solar cells are introduced in Chapter 3, together with the influence of the parasitic effects on their performance, specifically the influence caused by the series and the contact resistance. Chapter 4 deals with measurement techniques to determine the contact resistance of the front electrical contacts on the thin film solar cells. Chapter 5 focuses on the process parameters for fabrication of screen printed electrical contacts for CIS solar cells. Chapter 6 studies the degradation effects of solar cells, as well as the degradation of the electrical contacts caused by aging.

In the second part of this thesis, the contact effects in organic based thin film transistors are examined. Chapter 7 provides the general overview of thin film transistors. Chapter 8 overviews the electronic transport in the organic semiconductors, together with the experimental study of the contact effects in poly-3-hexylthiophene based thin film transistors. Additionally, a new method for determining the contact resistances at the individual electrical contacts of the thin film transistor is presented; a method based on the potential mapping of the transistor

channel. Finally, Chapter 9 focuses on the theoretical model of the contact effects in thin film transistors. This model is applicable for devices designed in both transistor configurations, the coplanar and the staggered configuration.

1.2 References

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Chapter 2

Metal-semiconductor electrical contacts in thin film devices

2.1 Lateral current transport in thin film devices

In thin film devices, metal electrodes are deposited to the structure in order to transport electrical current outside. In thin film devices, two types of electrical contact geometry can be found: the vertical and the planar contact configurations, Fig. 2.1.
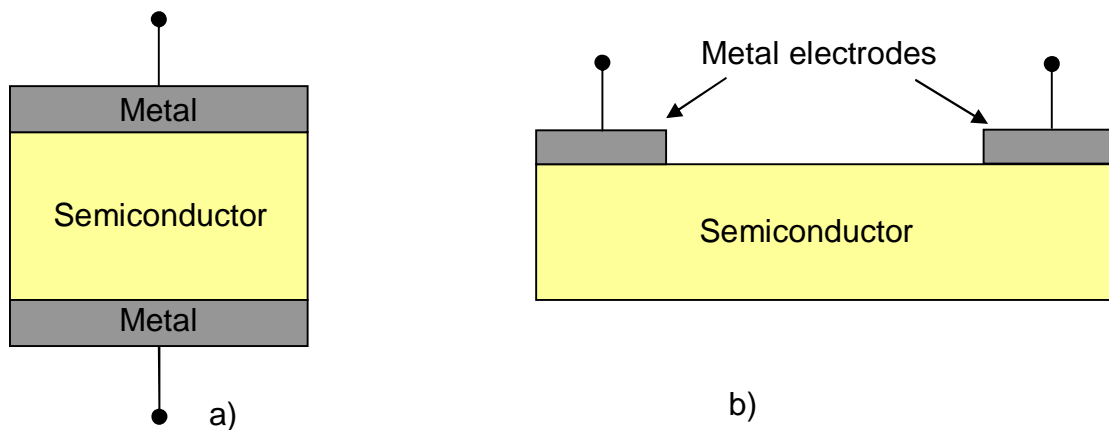
Fig. 2.1 a) Vertical and b) planar contact geometry.

In the vertical contact geometry, Fig. 2.1a, the current is uniformly distributed along the whole contact, making the current lines perpendicularly oriented to the surface of the metal-semiconductor contact. The electrical contact is characterized by a contact

resistance. In the case of the vertical contact geometry, the contact resistance, R_C, is given by:

$$R_C = \frac{\rho_c}{A}$$
(Eq. 2.1)

where ρ_c is defined as the specific contact resistance, and A is the contact area. Most of the thin film devices are working in the way that the electrical current is transferred laterally through the device, Fig. 2.1b. The case of lateral current transfer is typical for the solar cells and also in the case of thin film transistors. In the case of the homogeneous semiconductor layers, the current distribution under the electrical contact is not anymore uniformly distributed along the area below (or above) the electrical contact, because the current is choosing a less resistive path to travel through the semiconductor material. The current density distribution in the case of the lateral contact configuration is shown in Fig. 2.2. One can see that the highest current density occurs on the inner part of electrical contact, and reduces its value along the horizontal contact area.
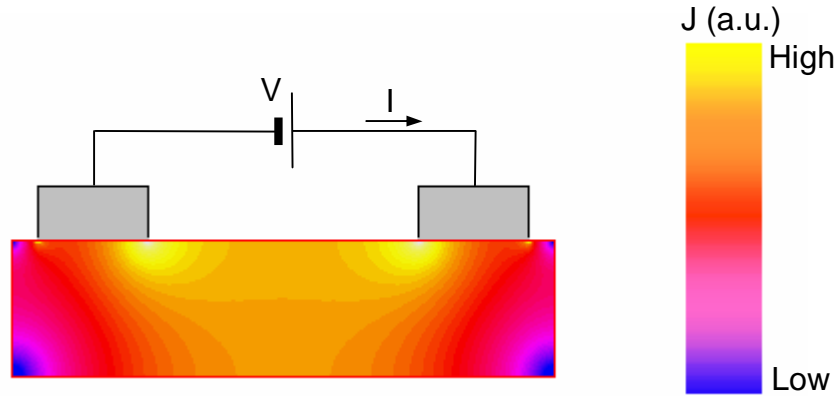
Fig. 2.2 Current density distribution in the lateral contact geometry.

The charge injection from the semiconductor to the metal electrode (and vice versa) can be described with the resistive network shown in Fig. 2.3, which is obtained by slicing the structure into small sections with length Δx. The contact resistance, R_1, and the resistance of a semiconductor, R_2, are given by:

$$R_1 = \frac{\rho_c}{W \cdot \Delta x},$$ (Eq. 2.2)

$$R_2 = R_{Sh} \frac{\Delta x}{W},$$ (Eq. 2.3)

where ρ_c is the specific contact resistance of the metal-semiconductor interface, R_{Sh} is the sheet resistance of the semiconductor layer, and W is the width of the contact. Using the Kirchhoff's laws and switching to the differential domain, one obtains the following set of equation:

$$\frac{dV}{dx} = -\frac{R_{Sh}}{W} I(x),$$ (Eq. 2.4)

$$\frac{dI}{dx} = -\frac{W}{\rho_c} V(x).$$ (Eq. 2.5)
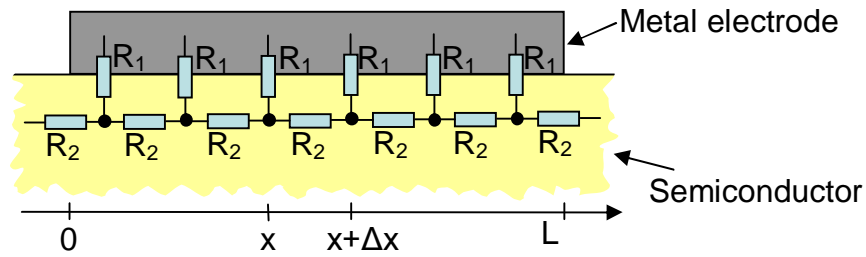
Fig. 2.3 The resistive network circuit of the lateral contact geometry structure. R_1 and R_2 represent the contact resistance of a metal-semiconductor junction and a semiconductor resistance of a slice Δx, respectively.

Equations 2.4 and 2.5 can be combined in the second order differential equation:

$$\frac{d^2 I}{dx^2} = \frac{R_{Sh}}{\rho_c} I(x).$$ (Eq. 2.6)

Using boundary conditions at the contact edges, $I(0)=I_{max}$ and $I(L)=0$, the final solution for the current distribution long the contact is given by:

$$I(x) = I_{max} \frac{\sinh\left(\frac{L-x}{L_T}\right)}{\sinh\left(\frac{L}{L_T}\right)}.$$ (Eq. 2.7)

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L is the length of the electrode and the parameter L_T, known as the current transfer length, is defined as

$$L_T = \sqrt{\frac{\rho_c}{R_{Sh}}} .$$

(Eq. 2.8)

The transfer length represents the length of the contact used for transferring most of the current from the semiconductor to the metal or from the metal to the semiconductor. Distribution of the current that is flowing under a 20 µm contact is illustrated in Fig. 2.4 for different values of the transfer length parameter. In the case when the conductivity of semiconductor film is low, the transfer length becomes small, and most of the current is transferred to the semiconductor close to the edge of the electrical contact. If the conductivity of the semiconductor film is increased, the transfer length takes higher values and the entire electrical contact is used for transferring the electrical current.
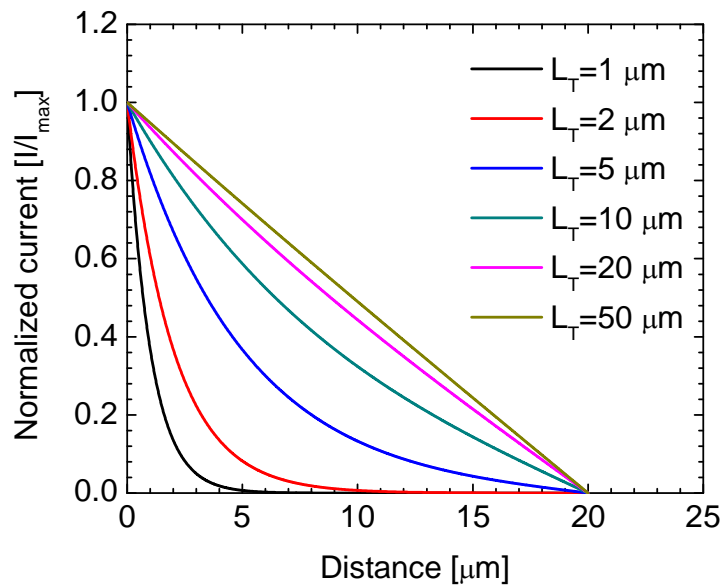
Fig. 2.4 Influence of the transfer length on the lateral current distribution underneath a 20 µm long contact.

The resistance of the metal-semiconductor contact in the lateral configuration is calculated as [1]:

$$R_C = \frac{\sqrt{\rho_c R_{Sh}}}{W} \coth\left(\frac{L}{L_T}\right).$$

(Eq. 2.9)

The influence of the length of electrical contacts on the normalized contact resistance, for different values of the specific contact resistance of the metal-semiconductor interface is shown in Fig. 2.5.
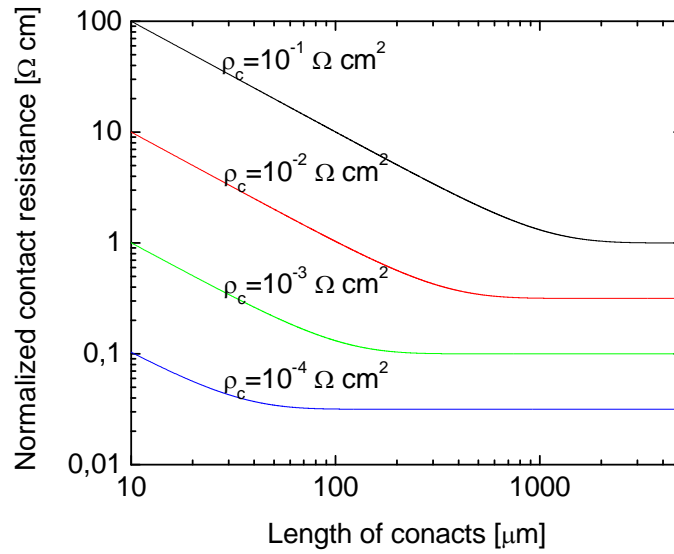
Fig. 2.5 The normalized contact resistance dependence on the length of electrodes for different values of the specific contact resistance of metal-semiconductor interface. The sheet resistance of the semiconductor film is Rs=10 Ω.

For an infinite long electrical contact (or when L>>L_T), the normalized contact resistance becomes independent on the length of the electrical contacts, and reaches its minimal value:

$$R_C W = \sqrt{\rho_c R_{Sh}} = \frac{\rho_c}{L_T}.$$

(Eq. 2.10)

In the limit for a short electrical contact (L<<L_T), the normalized contact resistance is given by:

$$R_C W = \sqrt{\rho_c R_{Sh}} \frac{L_T}{L} = \frac{\rho_c}{L}.$$

(Eq. 2.11)

Electrical contacts of devices with narrower electrodes exhibit higher values of the contact resistance. In order to minimize it, one has to come with a design of electrical contact with longer electrodes, which will make electrical devices bigger. The other way for minimizing electrical losses in the contacts is by minimizing the specific contact resistance parameter of the metal-semiconductor interface. With lower values of the specific contact resistance, the normalized contact resistance is reduced.

2.2 Metal-semiconductor electrical contacts

When a metal is making contact with a semiconductor, electrical charges drift from one side of the contact to another, until the thermal equilibrium is set and the Fermi levels in the two materials is coincident [2]. An ideal contact between a metal and an n-type semiconductor in the absence of surface states for three different types of metal-semiconductor contacts is shown in Fig. 2.6. Similar explanations can be derived for a p-type semiconductor.
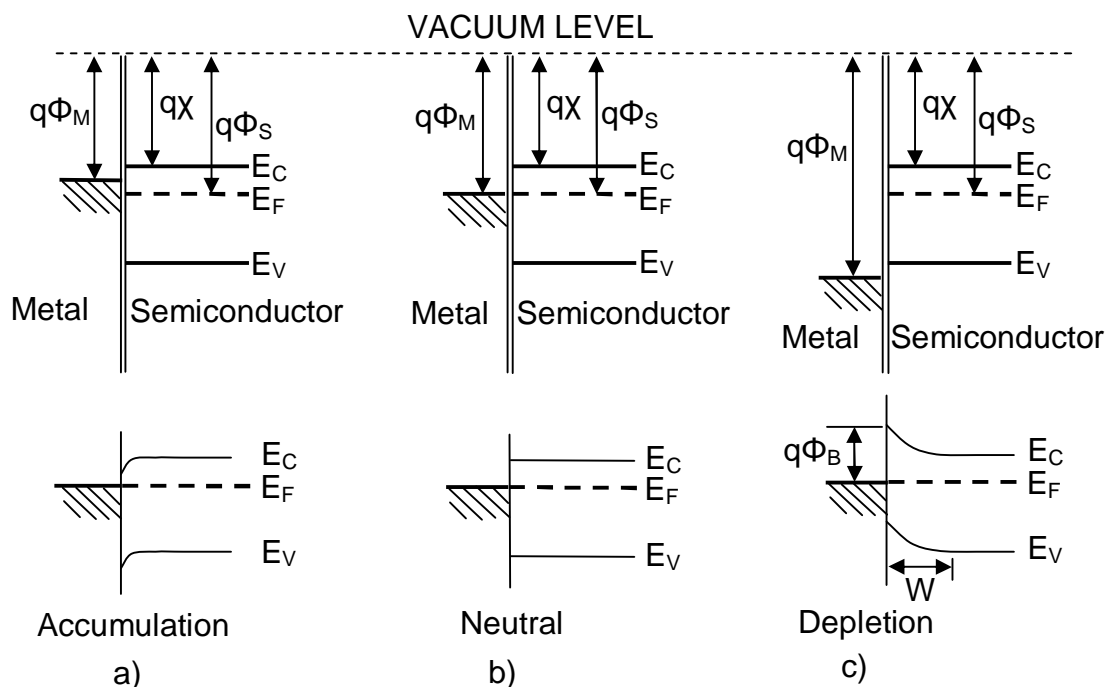
Fig. 2.6 Three different types of the Schottky (metal-semiconductor) contact: a) accumulation, b) neutral and c) depletion contact type. The upper and the lower parts show the energy band diagrams before and after contact, respectively.

The energy band diagrams are shown before contact in the upper part of the figure and after contact in the lower part. The band diagrams are shown for different metal work functions, Φ_M. The work function of a solid is defined as energy needed to elevate an electron from the Fermi level, E_F, to the vacuum level [3].

When the work function of the metal is lower than the semiconductor work function, $\Phi_M<\Phi_S$, electrons flow from the metal side towards semiconductor (Fig. 2.6a). The transfer of electrons will occur until equilibrium is achieved. Higher concentration of electrons on the side of semiconductor effects bending of the conduction and valence band of the semiconductor. This process is also known as an accumulation, since electrons are accumulated on the metal-semiconductor interface.

If both work functions are equal, $\Phi_M=\Phi_S$, there is no flow of charges from the metal to the semiconductor or vice versa. Hence, this is called as a neutral state, Fig. 2.6b.

Finally, when the work function of the metal is higher than the semiconductor work function, $\Phi_M>\Phi_S$, electrons flow from the semiconductor side towards the metal. The concentration of electrons in the semiconductor near the junction is reduced, and bending of the energy bands is observed, Fig. 2.6c. A depletion region and a barrier are formed. The height of the energy barrier is given by:

$$\phi_B = \phi_M - \kappa \, ,$$
<div align="right">(Eq. 2.12)</div>

where χ is the electron affinity of the semiconductor, defined as the difference between the vacuum level, and the bottom of the conduction band, E_C.

According to the Schottky model the work function of the metal has a distinct influence on the barrier height. However, experimental results showed that the work function of the metal sometimes does not have an influence on the barrier height of the metal-semiconductor contact. An improved electrical contact model of the metal-semiconductor junction is established by introducing surface states of the semiconductor [4]. According to this model, all semiconducting materials can be divided in two groups: covalent and ionic semiconductors.

Semiconductor materials from the fourth group of periodic table of the elements (Si, Ge), and most of III-V semiconductor compounds (i.e. GaAs) are highly covalent [5]. The experimental work showed that the barrier height of such covalent materials is almost independent on the metal work function. For the n-type semiconductor, the

barrier height is approximately 2/3 of the semiconductor band gap, $\phi_{B,n} \approx 2E_g/3$, and approximately 1/3 of the band gap for the p-type semiconductor, $\phi_{B,p} \approx E_g/3$.

For highly ionic materials, such as most of the II-VI compounds (i.e. ZnO, ZnS) and the transition-metal oxides (i.e. KTaO$_3$, KNbO$_3$), the barrier height is strongly dependent on the work function of the metal [5]. The formation of electrical contacts with zinc oxide leads to creation of the junction barrier. Different techniques are established to measure the barrier height of the metal-semiconductor junction [6], and here will be just mentioned without going into the details:

- the current-voltage measurement,
- the activation energy measurement,
- the capacitance-voltage measurement,
- and the photoelectric measurement.

In the most of cases the energy barrier between a metal and a semiconductor should be small, so that an ohmic contact is formed between the materials. The best way of forming ohmic contacts is by selecting the appropriate metal that will form neutral or accumulated type of contacts. This is also called barrier height engineering. Finding suitable metal material is usually rather difficult. Hence, a more common technique of forming ohmic contacts is by the deposition of a metal on a highly doped semiconductor.

Low N$_D$
Thermionic
Emission
a)

Intermediate N$_D$
Thermionic/Field
Emission
b)

High N$_D$
Field
Emission
c)
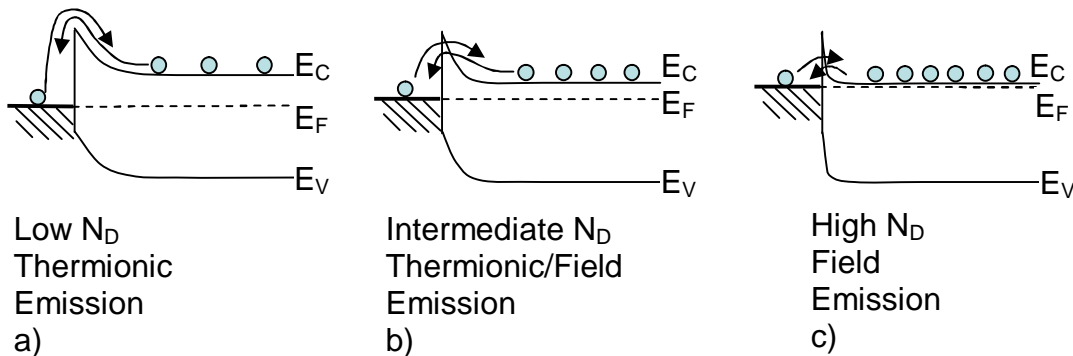
Fig. 2.7 Energy band diagram of a metal semiconductor junction for different doping concentration of the semiconductor.

Nearly all practical metal-semiconductor contacts form a depletion type of contact. The width of the depletion region is inversely proportional to the square root of the doping concentration of the semiconductor, $W \sim N_D^{-1/2}$. For very high doping

concentration the width of the depletion region is very small, so that charges can tunnel through the barrier.

The energy band diagrams of a metal-semiconductor junction for different doping concentrations are shown in Fig. 2.7. For relatively low doped levels, Fig. 2.7a, electrons are thermally excited to energies equal or higher than the barrier height. This process is known as thermionic emission (TE) and the current-voltage relationship is given by:

$$J = A^* T^2 \exp\left[-\frac{q\phi_B}{kT}\right]\exp\left[\frac{qV}{kT}-1\right],$$
(Eq. 2.13)

where A^* is the Richardson constant, T is the absolute temperature in Kelvin, q is the elementary charge, k is the Boltzmann constant. Electrical contacts are characterized by the specific contact resistance, defined as:

$$\rho_c = \left(\frac{\partial J}{\partial V}\right)^{-1}\Bigg|_{V=0}.$$
(Eq. 2.14)

Unit of the specific contact resistance is Ωcm^2. For the thermionic emission, the specific contact resistance is given by:

$$\rho_c(TE) = \rho_1 \exp\left(\frac{q\phi_B}{kT}\right),$$
(Eq. 2.15)

where

$$\rho_1 = \frac{k}{qA^*T}.$$
(Eq. 2.16)

For intermediate doping concentrations of the semiconductor, Fig. 2.7b, the thermionic-field emission (TFE) is the dominant charge transport process. Charges are thermally activated to energy below the barrier height where the barrier is

sufficiently narrow for tunneling to take place. In the case of the thermionic-field emission, the specific contact resistance is given by:

$$\rho_c(TFE) = \rho_1 C_1 \exp\left(\frac{q\phi_B}{E_0}\right).$$

(Eq. 2.17)

For semiconductors with relatively high doping concentrations the Fermi level is close to the bottom of the conduction band, or even inside the conduction band (degenerated semiconductors), Fig. 2.7c. In this case the barrier width is very narrow, and carriers can tunnel through it without additional excitation. This process is known as the field emission (FE). The expression for the specific contact resistance is given by:

$$\rho_c(FE) = \rho_1 C_2 \exp\left(\frac{q\phi_B}{E_{00}}\right).$$

(Eq. 2.18)

In previous equations, 2.17 and 2.18, C_1 and C_2 are functions of the doping concentration N_D, temperature T, and the barrier height Φ_B. The energies E_{00} and E_0 used in equations 2.17 and 2.18 are defined as:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\varepsilon_s\varepsilon_0 m^*}} ,$$

(Eq. 2.19)

$$E_0 = E_{00}\coth\left(\frac{E_{00}}{kT}\right),$$

(Eq. 2.20)

where ε_s is the dielectric constant of the semiconductor, h is the Plank constant, and ε_0 is the electrical permittivity of vacuum.

2.3 References

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Chapter 3

Thin film solar cells

The energy conversion process of a solar cell can be divided into two parts, the photogeneration and charge separation. The solar cell has to be able to absorb a large fraction of the sun spectrum. A schematic cross section of a solar cell is shown in Fig. 3.1. Electron-hole pairs are generated if the photon energy is higher than the energy bandgap of the absorber of the solar cell. In the second step, the electron hole pairs are separated due to the built-in electrical field of the diode, resulting in a photocurrent flow.
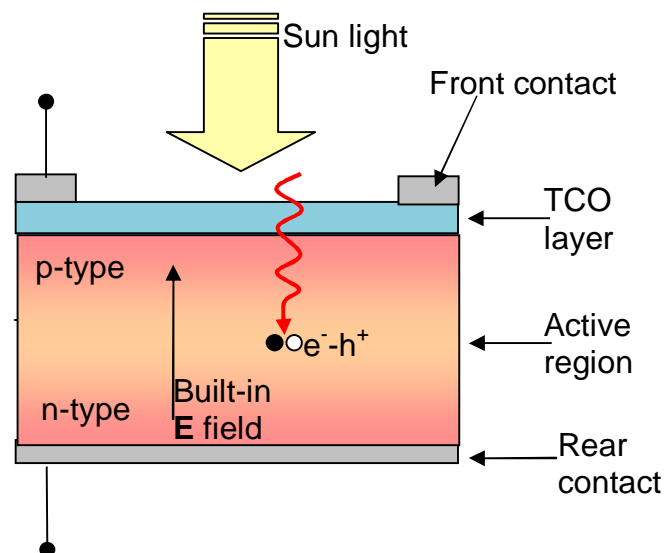
Fig. 3.1. The schematic cross section of a solar cell.

The current-voltage characteristic of an ideal solar cell in dark can be described by [1]:

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right],$$

(Eq. 3.1)

where I_s is the diode saturation current, q is the elementary charge, n is the diode ideality factor, k is the Boltzmann constant, and T is the absolute temperature in Kelvin. If the cell is illuminated, the light generated current I_L is superimposed to the dark (non-illuminated) diode current:

$$I = I_s \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] - I_L.$$

(Eq. 3.2)

The equivalent electrical circuit and the current-voltage characteristic of an ideal solar cell are shown in Fig. 3.2. The maximum power generated from the solar cell is equal to the product of the short circuit current, I_{sc}, the open circuit voltage, V_{oc}, and the fill factor, FF. These three parameters together with the efficiency of the solar cell, η, are the key characterization parameters of the solar cell performance.
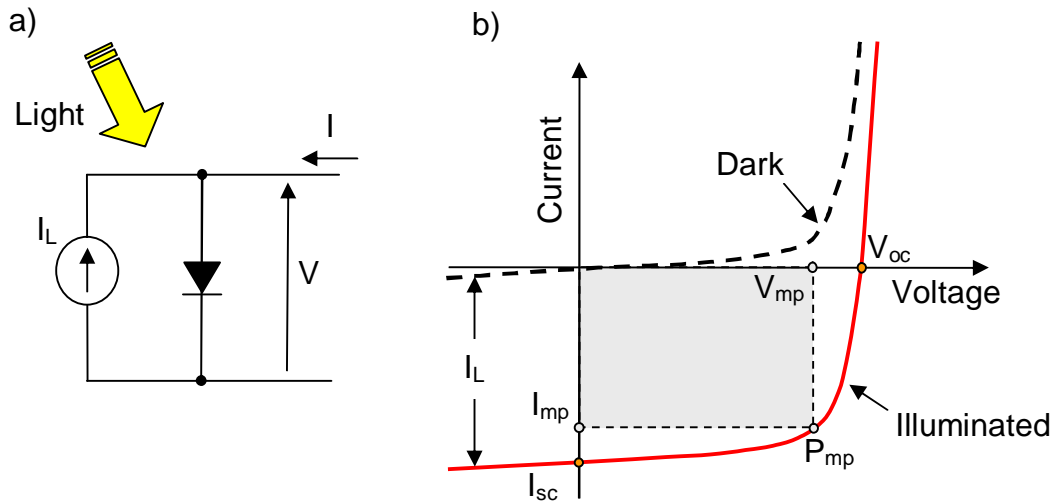
Fig. 3.2. a) The equivalent circuit of an ideal solar cell. b) The current-voltage characteristic of a solar cell with and without illumination.

The short circuit current is given by the photogenerated current at short circuit. The open circuit voltage is obtained when there is no current flow through the cell. According to equation 3.2, the open circuit voltage is defined as:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_s} + 1\right).$$
(Eq. 3.3]

The open circuit voltage depends on the photocurrent and the diode saturation current, I_S. Lowering of the saturation current will increase the open circuit voltage of the solar cell.

The fill factor of a solar cell, FF, is defined by the ratio of the maximal output power of the cell to the product of the short circuit current and the open circuit voltage:

$$FF = \frac{P_{mp}}{I_{sc}V_{oc}} = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}}.$$
(Eq. 3.4)

The conversion efficiency, η, defines the ratio of the photogenerated electrical output to the total power of the incident light:

$$\eta = \frac{V_{mp}I_{mp}}{P_{in}} = \frac{V_{oc}I_{sc}FF}{P_{in}}.$$
(Eq. 3.5)

3.1 Materials for thin film solar cells

Crystalline silicon based solar cells are nowadays well performing and reliable, commercially available and widely used in a variety of photovoltaic systems. However, their cost is still too high to be competitive with classical electricity production. The thickness of 200 μm of a silicon wafer is needed to absorb sun light (if no light trapping techniques are introduced), and this is the main reason for the high cell cost. On the other hand, thin film solar cells have thickness of several hundred nanometers to a few micrometers. Thin film solar cells consist of sequence of thin film layers which form a photodiode. The thin film solar cells are electrically connected by a metal back contact and a front contact which is usually realized by transparent conductive oxide (TCO). Schematic cross sections of various thin film solar cells are shown in Fig. 3.3. Different absorber materials have been used for thin film solar cells. The most promising thin film solar cells are based on chalcopyrite

compounds (CuInGaSeS), cadmium telluride, and amorphous silicon, Fig. 3.3a-c respectively [2], [3].

Al:ZnO / ITO		Substrate		Substrate
ZnO				
n-CdS		ITO		ZnO
		SnO$_2$		
p-Cu(InGa)Se$_2$		n-CdS		p-i-n a-Si:H
		p-CdTe		
Mo				ZnO
Substrate		Ni/Al		Ag/Al
a)		b)		c)
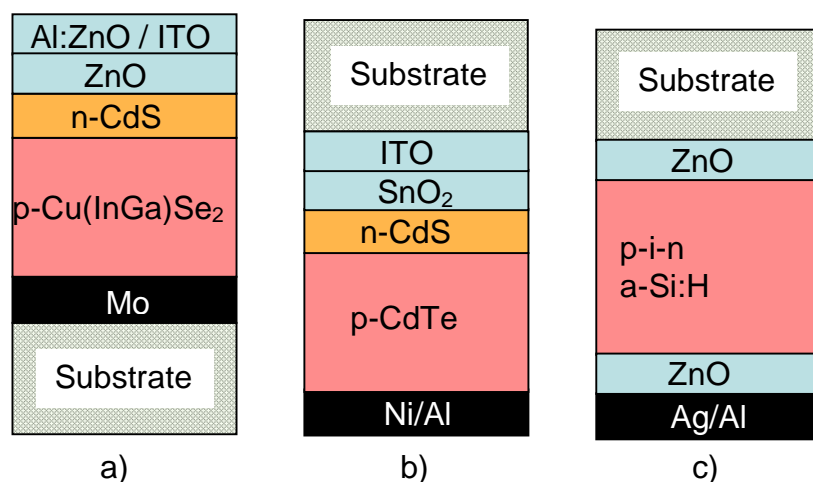
Fig. 3.3. a) Chalcopyrite CIGS solar cell in the substrate configuration. b) CdTe solar cell in the superstrate configuration. c) Amorphous silicon solar cell in the superstrate configuration.

Thin film solar cells can be realized in substrate or superstrate configuration. In the superstrate configuration the substrate acts as a carrier for the solar cell. Since the light enters the light through the substrate, the substrate has to perform with high transparency, and thus glass substrates have been widely used.

In the substrate configuration the substrate just acts as a carrier for the solar cell. Since the transparency is not the key issue for such solar cell, different materials (i.e. the stainless steel foil) may be used to perform as a substrate for a solar cell. The light enters the solar cell through the transparent conductive oxide (TCO) layer, which is deposited on the top of the solar cell. Transparent conductive oxides are mainly deposited by sputtering processes or by low pressure chemical vapor deposition. Typically, transparent conductive oxides are n-type degenerated semiconductor layers with good electrical conductivity and high transparency in the visible part of the spectrum. Although there are huge numbers of materials that suit in these demands, the most often used TCO layers are aluminum doped zinc-oxide (Al:ZnO) and indium tin oxide (ITO).

3.2 From individual solar cells to solar modules

In order to boost electrical output, the solar cells are connected in series and/or in parallel to form a solar cell module. When the solar cells are connected in series, the current that is going through the solar cells is identical through each of them, and the output voltage is equal to the sum of all output voltages of individual solar cells. If the solar cells are connected in parallel, the output voltage over all connected solar cells is identical, and the output current of the device is equal to the sum of the electrical current values generated by individual solar cells. Standard module technology is based on interconnecting the p- type silicon (Si) based solar cells. The interconnections have to connect the rear side of one solar cell with the front side of the neighboring solar cell. The interconnecting process is not simple, and different practical solutions were presented in order to simplify fabrication process and also to achieve some additional esthetical credits [4].

Depending on the thin film solar cell technology and the substrate configuration different concepts are used for serially connection of individual solar cells. In the rigid thin film modules, solar cells and solar modules are manufactured in the same production line. Solar cells are created in the substrate or superstrate configuration, and the electrical connections are created *in situ*, also known as monolithic integration. The serial connection over a solar module on a glass substrate is illustrated in Fig. 3.4. A laser ablation process is used to pattern the individual layers of the solar cell. Three laser scribing steps are needed to interconnect thin film solar cells on a glass substrate. After the deposition of the TCO layer on the substrate, the TCO layer is structured in a way to define solar cells on the substrate. The production continues with deposition of the window and the active layers. The second laser step is used for patterning the active layer of the solar cell in order to make serial connections between the rear electrode of one solar cell and the front electrical contact of neighboring one. Finally, the rear electrode is deposited and the third laser scribing step is used to remove shortcuts. The losses made by interconnecting cells and modules in such way, strongly depends on the accuracy of the laser scribing steps. The fabrication process is finalized with encapsulation process of the module.

The module is laminated with an encapsulant to a front and/or back sheet, typically with a sheet of glass or EVA (ethyl vinyl acetate) encapsulants.
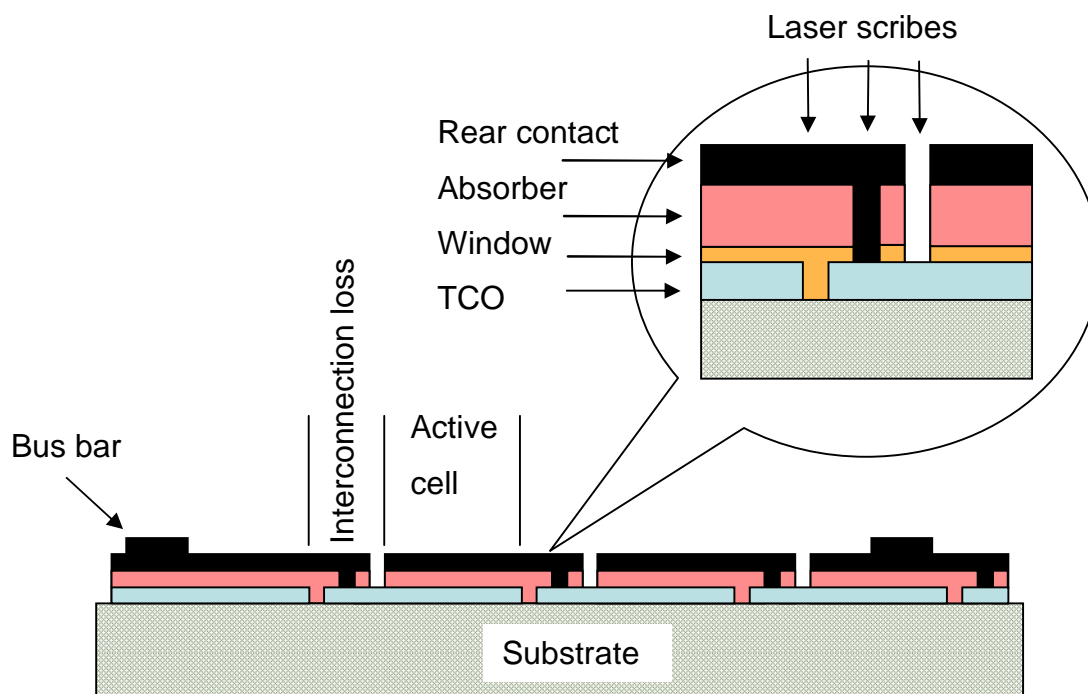
Fig. 3.4. The schematic cross section of a thin film solar module with monolithic integration connections.

Recently, flexible thin film solar cells and modules were demonstrated by depositing the photoactive layer and other necessary layers on a flexible substrate. When the substrate is an insulator, interconnection of solar cells to a module may be done by using the monolithic integration process. In the case when the substrate is a conductor, other techniques for electrical connection must be used. Solar modules may be realized by interconnecting individual solar cells similarly to conventional interconnection process of crystalline silicon solar cells. In this work, the electrical contact formation on CuInSe thin film solar cells was studied. The solar cells were deposited on the flexible stainless steel foil by sputtering processes. The interconnections between individual solar cells were made with copper wire technique. The front electrical contact grid is formed by screen printing metal paste on the top/front surface of a solar cell. The interconnecting process uses copper wire that is glued with the metal paste on the front side of one solar cell. The electrical connection is closed by soldering/gluing the wire to the conductive substrate (in this

case stainless steel foil) of the neighboring cell. The process is repeated over the whole solar cell module.

3.3 Power losses in solar cells

The performance of a solar cell is reduced due to the influence of several power loss mechanisms. To achieve high conversion efficiency the losses in the solar cell have to be minimized. According to the origin, these losses can be divided into two groups, optical and electrical losses.

Optical losses can occur due to:

▪ **surface reflection** – the reflection loss is proportional to the refractive index difference between the solar cell and air.

▪ **front contact shading** – shadowing losses are proportional to the area of solar cell covered with the front contact grid.

▪ **absorption losses** – light is also absorbed in regions that do not contribute to the photocurrent. As an example, the absorption can occur in the window layer of thin film solar cell reducing the amount of light transmitted into the active layer of a solar cell.

The electrical losses can be further classified in **recombination** and **ohmic** losses. Recombination processes play an important role in solar cells. Photogenerated charges can recombine before reaching the electrodes of the solar cell. The recombination of charges mainly reduces the open circuit voltage of a solar cell and increases the diode ideality factor, which have a consequence the reduction of the solar cell fill factor. In solar cells, two different types of recombination are observed:

• the surface recombination,

• and the bulk recombination.

In the case of a crystalline silicon solar cell, which is a diffusion controlled solar cell, bulk recombination can be reduced by using material with high diffusion length. In the case of a thin film silicon solar cell, which is a drift controlled device, bulk recombination can be reduced by using material with high mobility lifetime product. On the other hand, the surface recombination may be minimized with the surface passivation.
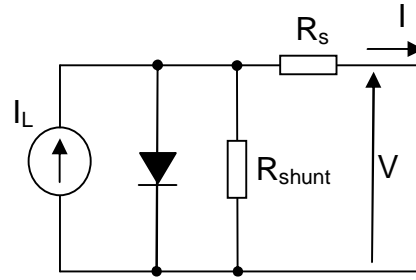
Fig. 3.5. The equivalent electrical circuit of a real solar cell.

The parasitic Ohmic losses in solar cells are undesirable and also unavoidable effects. Parasitic resistances, the series and the shunt resistance, reduce the conversion efficiency of a solar cell. The equivalent circuit of a real solar cell is shown in Fig. 3.5. The shunt resistance, R_{shunt}, represents the resistive losses caused by the current leakage across the diode and along the edge of a solar cell. Impurities and crystal defects in the depletion region are also contributors to a low parallel resistance. Contributors to the series resistance, R_s, will be analyzed separately in the next subchapter.

The current-voltage characteristic of a real solar cell with the parasitic resistances is given by:

$$I = I_L - I_s \left\{ \exp\left[\frac{q}{kT}(V + IR_s) \right] - 1 \right\} - \frac{V + IR_s}{R_{shunt}}.$$
(Eq. 3.6)

The influence of the series and the shunt resistance on the current-voltage characteristics for a thin film solar cell is shown in Fig. 3.6. The illustration has been modeled for the chalcopyrite based CIGS thin film solar cell according to [5]. The solar cell performed with the short circuit current of 34.8 mA/cm^2 and the open circuit voltage of 713 mV over the area of 0.996 cm^2. In the ideal case, the shunt resistance is taking infinite value and the value of the series resistance is zero. As the shunt resistance of the solar cell decreases, the current-voltage characteristic perform with curve bending and the solar cell fill factor reduces its value. For very low values of the shunt resistance (lower than 200 Ωcm^2) the open circuit voltage of the solar cell reduces its value. Values for the shunt resistance higher than 1 kΩcm^2 may be

assumed as a satisfactory value for the shunt resistance of a CIGS solar cell because the current-voltage characteristic is not strongly affected.

a)

b)
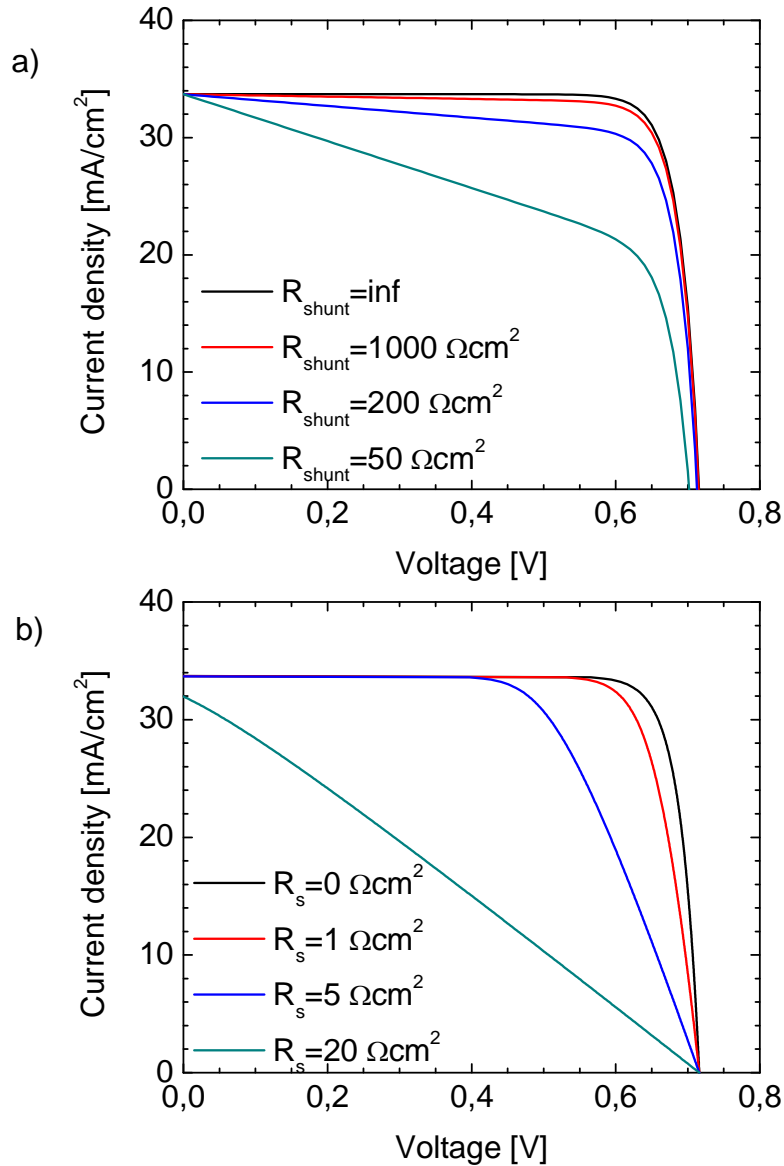
Fig. 3.6. a) Influence of the shunt resistance on the current-voltage characteristics of the CIGS solar cell with neglected influence of the series resistance. b) Influence of the series resistances on the current-voltage characteristic of the CIGS solar cell assuming no effect of shunt resistance. The solar cell parameters in this model were taken from [5] and [6].

On the other hand, the series resistance may cause change of the output characteristic of a solar cell. As the series resistance increases, the bending of

current-voltage characteristic of the solar cell occurs (the characteristic becomes less "squared") and the fill factor reduces, while the open circuit voltage and the short circuit current remain unchanged. As the series resistance is increased to values above 20 Ωcm^2, the short circuit current is reduced, as well as the fill factor of the solar cell. By neglecting the influence of the shunt resistance on the solar cell performance, the generated output power from the solar cell may be calculated as:

$$P = IV = I\left[\frac{kT}{q}\ln\left(\frac{I_L - I}{I_s} + 1\right) + R_s I\right].$$

(Eq. 3.7)
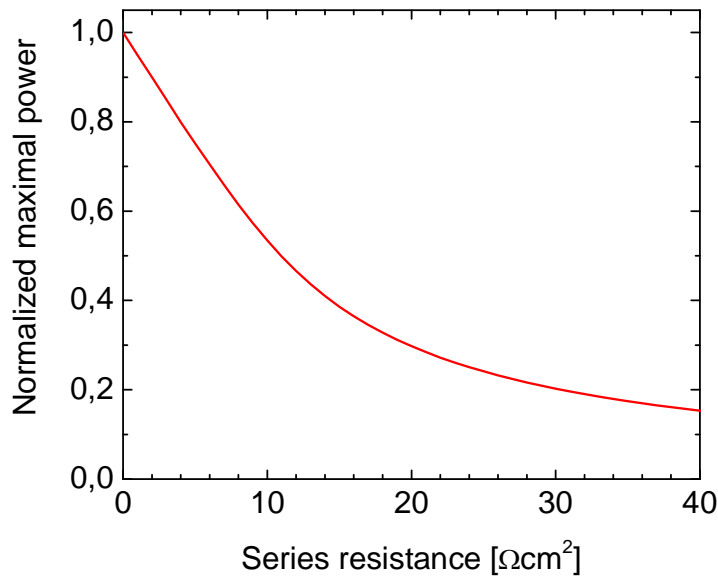
Fig. 3.7. Normalized maximal generated power versus series resistance (according to the Fig. 3.6b).

The Fig. 3.7 illustrates the influence of the series resistance on the generated output power of the CIGS solar cell. The solar cell has been modeled with the same parameters as in Fig. 3.6 and assuming the infinite shunt resistance in the solar cell. As the series resistance increases, the output power of the solar cell reduces, and the drop of the power is very prominent for the small values of the series resistance. The solar cell with the series resistance of 2 Ωcm^2, would perform with 10% lower output power then when there would be no electrical losses generated in the solar cell. As the series resistance of the CIGS solar cell increases to 5 Ωcm^2 the output

power of the CIGS solar cell will be only 75% of its maximal. Thus, minimization of the series resistance is necessary step in order to achieve solar cells with high conversion efficiency.

3.4 Contributors to series resistance of thin film solar cell

The series resistance of a solar cell can be described as the sum of several different resistances, Fig. 3.8:

- Lateral resistance of the rear contact, R_1,
- Contact resistance between the rear electrode and the diode, R_2,
- Bulk/semiconductor resistance, R_3,
- Resistance of the transparent conductive oxide, R_4,
- Contact resistance between the front electrode and the semiconductor, R_5,
- Grid fingers resistive losses, $R_{fingers}$,
- Collection bus ohmic losses, R_{bus}.
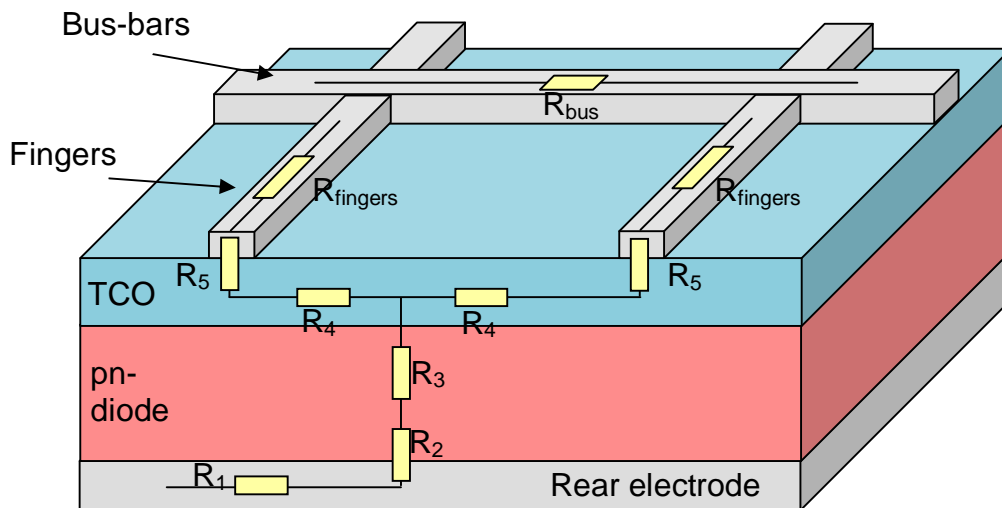
Fig. 3.8. The cross section of a thin film solar cell with an illustration of the resistive losses.

The resistance of the rear metal electrode, R_1, is calculated as:

$$R_1 = \rho_{m,back} \frac{t_m}{A}, \qquad \text{(Eq. 3.8)}$$

where $\rho_{m,back}$ is the resistivity of the rear metal electrode, t_m is the thickness of the rear electrode, and A is the unit area of a cell. Due to very high conductivity of used metal, this resistance is (usually) negligible.

The contact resistance of the back contact electrode to the semiconductor layer, R_2, is given by:

$$R_2 = \frac{\rho_{c,back}}{A}, \qquad \text{(Eq. 3.9)}$$

where $\rho_{c,back}$ is the specific contact resistance of the metal-semiconductor contact on the back side of a solar cell. In the case of the CIGS solar cells studied in this work, the back electrode is in the contact with entire area of the solar cell. Hence, the contact resistance between the rear electrode and the solar cell can be in general neglected.

The bulk resistance, R_3, represents resistive losses in the active region of the solar cell. Since the thickness of thin film solar cells is approximately 1-2 µm, the bulk resistance, $R_3 = \rho_{bulk} \cdot t_{bulk} / A$, is negligible.

The resistance of the transparent conductive oxide layer, R_4, is calculated as [7]:

$$R_4 = \frac{R_{Sh-TCO} d^2}{12A}, \qquad \text{(Eq. 3.10)}$$

where d is the spacing between adjacent fingers, and R_{Sh-TCO} is the sheet resistance of the transparent conductive oxide layer, Fig. 3.9. According to the equation 3.10, as the spacing between contact fingers decreases and the conductivity of the TCO layer increases, the contribution of the window layer to the series resistance may be reduced. However, narrowing the distance between the contact fingers has as a consequence of an increase in the number of fingers over the solar cell. The higher amount of finger structures on the front side of the solar cell would result with an

increase in the shadowing losses, which can be further on reduced only by narrowing the width of the contact fingers.

The resistance between the front contact grid and the transparent conductive oxide layer, R_5, is calculated as:

$$R_5 = \frac{d}{2A} \sqrt{\rho_c R_{Sh-TCO}} \coth\left(W_f \sqrt{\frac{R_{Sh-TCO}}{\rho_c}} \right),$$

(Eq. 3.11)

where ρ_c is the specific contact resistance of the contact finger, and W_f is the width of the finger. The contact resistance has been already introduced in the Chapter 2 of this thesis. It has been shown that the contact resistance can be reduced by increasing the contact geometry (i.e. W_f) and decreasing the specific contact resistance ρ_c.

Fig. 3.9 illustrates the front contact grid pattern on a front side of a solar cell. The pattern consists of a wide metal bus-bar and numerous number of narrow finger structures. The grid fingers are characterized with the length L_f and the width W_f. The resistance of the grid's fingers is proportional to the resistivity of the fingers and to the geometry of the finger structures:

$$R_{fingers} = \frac{\rho_{m,front} d L_f^2}{3 W_f t_{finger} A},$$

(Eq. 3.12)

where $\rho_{m,front}$ is the resistivity of the front contact grid and t_{finger} is the thickness of deposited metal fingers.

The current collected by individual finger structures of the contact grid are further transfer to the bus-bar of a front contact grid. The length of the bus-bar is defined as $L_b = nd$, where n is the number of fingers and d distance between adjacent fingers. If the current enters the bus bar continuously, the resistance over the bus-bar is given as:

$$R_{bus} = \frac{n^2 L_f \rho_{m,front} d^2}{12 W_b t_{bus}},$$

(Eq. 3.13)

where W_b and t_{bus} are the width and the thickness of the bus-bar, respectively.
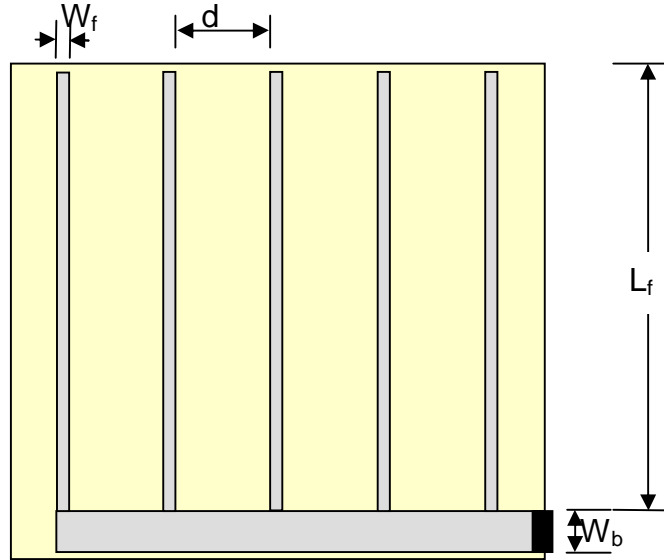
Fig. 3.9. Schematic of the front contact grid pattern on a front side of a solar cell.

The shadowing losses are calculated as a ratio of the total grid area to the total area of a cell. For a rectangular solar cell with the simple grid pattern, as the one in Fig. 3.9, the power lost within the shadowing of the front contact grid is given as:

$$P_{shadow} = P_L \eta \frac{W_b L_b + n W_f L_f}{n d L_f} \ ,$$

(Eq. 3.14)

where P_L is the power density of the incident light and η is the conversion efficiency of the cell.

According to the equations 3.10 – 3.14, dimensions of contact fingers and the bus-bar have a strong influence on the series resistance of a solar cell and also power losses due to the shadowing effect. As an example, the narrower contact fingers may decrease the shadowing losses, but it ought to result in an increase of the series resistance through the contact resistance, R_5, and the finger resistance, $R_{fingers}$. Hence, a detail optimization of the front contact grid parameters is needed.

3.5 References

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Chapter 4

Front electrical contacts of thin film solar cells

In this chapter, the screen printed technique for making front electrical contacts will be described. Details regarding measurement techniques for quantitatively determining properties of electrical contacts will be presented along with industrial requirements that should be reached for electrical contacts of chalcopyrite thin film solar cells.

4.1 Transmission line method

The resistance of a metal-semiconductor contact may be measured with several methods. The standardized technique of measuring the contact resistance is by the 4-probe setup, as depicted in Fig. 4.1. When the current, I, is passing through the sample from the contact 1 to the contact 2, and the voltage V is measured across the two contacts, the total resistance, $R_T = V/I$, is given as:

$$R_T = 2R_C + R_{Semi} = 2R_C + R_{Sh}\frac{d}{W}, \qquad\qquad \text{(Eq. 4.1)}$$

where R_C is the contact resistance given by equation 2.9, d is the electrode spacing, W is the width of the electrodes, and R_{Semi} and R_{Sh} are the resistance and the sheet resistance of the semiconductor layer, respectively. By knowing the sheet resistance

of the semiconductor layer, the width of the electrodes and the spacing between them, the contact resistance can be calculated.
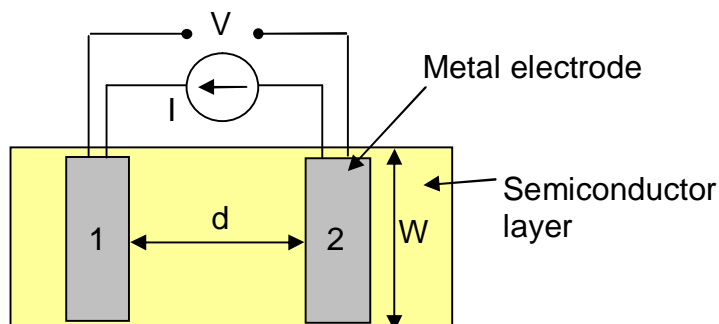
Fig. 4.1 Four probe measurement technique.

The most commonly used technique for measuring the contact resistance is the transmission line method (TLM). The TLM test structure consists of several electrodes as shown in Fig. 4.2a, that exhibit with the same geometry of length L and width W. The measurements of resistances are made between adjacent electrical contacts while the separation between electrodes is varied. The resistance values are plotted for different space distances between electrodes, and linearly fitted to a graph, Fig. 4.2b. From the plot of the total resistance as a function of the electrode spacing, four parameters can be extracted: sheet resistance, contact resistance, specific contact resistance, and the current transfer length. The slope of the linear fit is proportional to the sheet resistance of the sample, Slope=R_{Sh}/W. The intercept with the ordinate is equal to two times the contact resistance. Calculating the sheet resistance of the semiconductor layer and the contact resistance of the metal-semiconductor interface, the specific contact resistance and the current transfer length can be determined according to the equations 2.8 and 2.9.

4.1.1 Three electrodes measurement technique – Enhanced TLM method

The transmission line method is a very powerful method for determining the contact resistance. However, it does not yield correct results if the sheet resistance below the electrical contacts is different from the sheet resistance between the contacts. In this case the model has to be extended resulting in the following expression for the total resistance:

$$R_T = R_{Sh}\frac{d}{W} + 2R_c = R_{Sh}\frac{d}{W} + 2\frac{\rho_c}{L_{Tc}W}\coth\left(\frac{L}{L_{Tc}}\right), \qquad \text{(Eq. 4.2)}$$

where L_{Tc} is the transfer length calculated as $L_{Tc}=(\rho_c/R_{Sh\text{-}c})^{1/2}$, and $R_{Sh\text{-}c}$ represents the sheet resistance under the contacts.
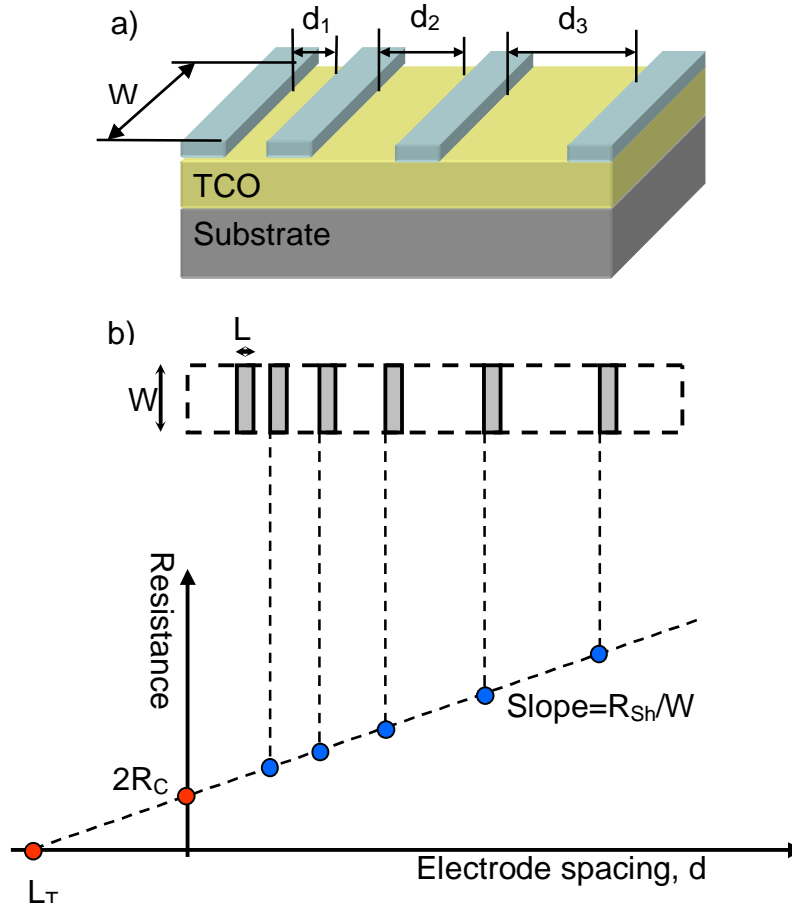
Fig. 4.2 Transmission line method (TLM) a) test structure, and b) measurement technique for determining the contact resistance.

The slope of the linear fit, the plot of the total resistance as a function of the electrode spacing, still leads to the sheet resistance, and more precisely, it is the sheet resistance between the electrodes. The intercept of linear fit with the y-axis is double the value of the contact resistance. However, the specific contact resistance and the sheet resistance under the contacts cannot be determined with the standard TLM method. Thus, additional information can be obtained by using the modified test structure shown in Fig. 4.3. The current probes are applied to the electrodes 1 and 2,

41

while the voltage is measured between the electrodes 2 and 3. This configuration is also known as the contact end resistance configuration.
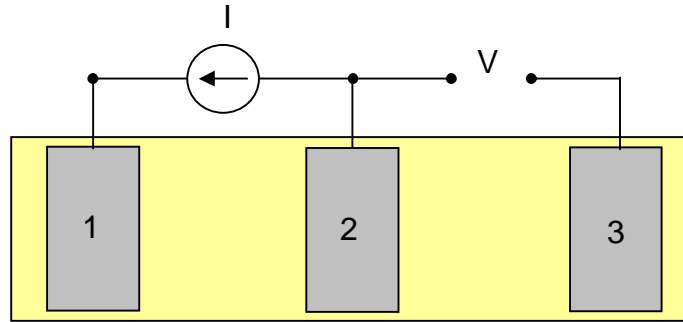
Fig. 4.3 *The contact end resistance test structure.*

By dividing the voltage between electrodes 2 and 3 by current flowing between electrodes 1 and 2, the contact end resistance, R_{CE} is determined. An analytical expression for the contact end resistance is given as:

$$R_{CE} = \frac{V}{I} = \frac{\rho_c}{L_{Tc}W} \frac{1}{\sinh\left(\dfrac{L}{L_{Tc}}\right)}, \qquad \text{(Eq. 4.3)}$$

where L_{Tc} represent the transfer length in the case when the sheet resistance under the electrodes differs from the sheet resistance between the electrodes. The ratio of the contact end resistance and the contact resistance is:

$$\frac{R_{CE}}{R_C} = \frac{1}{\cosh\left(\dfrac{L}{L_{Tc}}\right)}. \qquad \text{(Eq. 4.4)}$$

By measuring the contact resistance with the transmission line method and determining the contact end resistance with the three electrodes setup, the specific contact resistance and the transfer length parameter can be calculated. In addition, it is possible to determine the sheet resistances between and under the electrical contacts. The enhanced TLM method demands the accurate measurement of small resistances on the milliohm scale, otherwise the specific contact resistance may be incorrectly calculated.

4.2 Screen printing technique for making electrical contacts

In industrial applications, the formation of the electrical contacts is one key steps towards the fabrication of final solar cell, yet often, industries are turning towards less expensive deposition techniques and less expensive materials. Printing techniques have a special place in various industry branches because of their simplicity, financial costs, promptness, and flexibility to be used within different technologies. Commonly used printing techniques are: screen printing, syringe printing [1], [2], stencil printing [3], [4], pad printing [5], [6], and roller printing [1], [2]. In the photovoltaic industry, screen printing is the most commonly used method for deposition of thick paste films onto a substrate. In this thesis, electrical contacts for applications in thin film solar cells were fabricated by the screen printed technique.
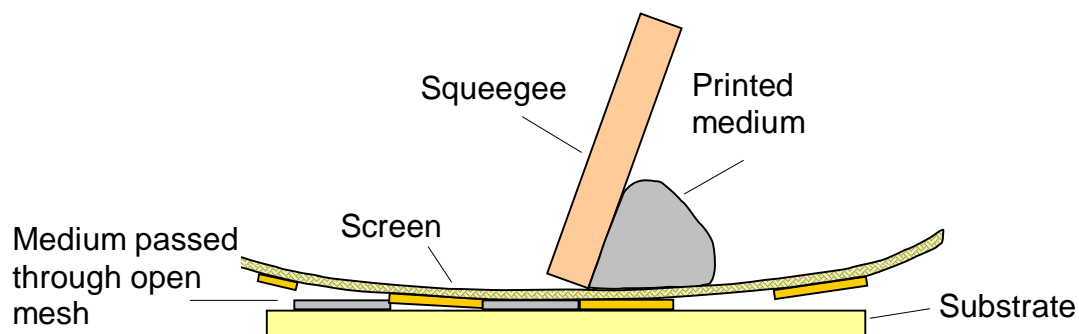
Fig. 4.4 The screen printing process.

The key advantages of the screen printing are the simplicity, the effectiveness, and the speed of the process [7], [8]. The screen printing is also known as the off-contact printing, since the screen is fixed just above the substrate before printing actually takes place. The process uses a squeegee to press the fluid (i.e. metal paste, ink) through predefined openings in the screen. The screen is a wire netting, typically made from stainless steel, which is then coated with an emulsion layer. As the squeegee starts moving across the screen, it pushes the mesh down into contact with the substrate, and the surplus medium is rolled in advance of the passing squeegee, Fig. 4.4. As the squeegee moves forward, the section of the screen initially pressed then peels away from the substrate behind the advancing squeegee, depositing the paste on the surface as the screen peels off. After leveling, the printed

films are dried, and compound films of very small grain sizes, some reaching up to a few micrometers, are formed.

The printing quality depends on the mesh openings, the wire diameter, and the mesh thickness. Furthermore, the printing process can be controlled with the speed of the squeegee, as well as with the pressure and the angle that squeegee makes on the screen. In order to achieve printing lines with a high quality, the perfect combination of mentioned parameters must be met.
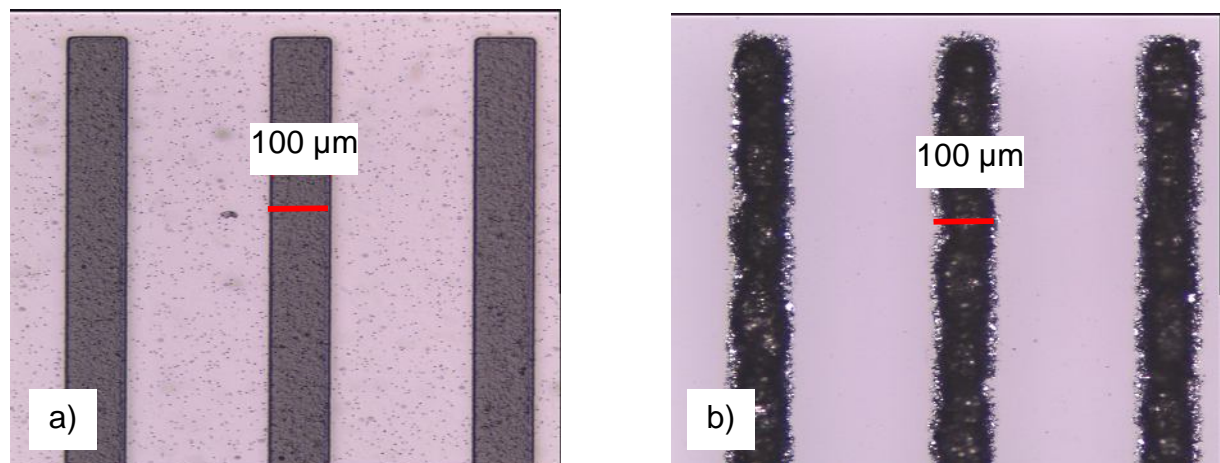
Fig. 4.5 a) Micrograph of a predefined pattern on the screen used for the formation of electrical contacts. b) Micrograph of screen printed structures of CE3104WXL silver paste on the sputtered ZnO substrates, after a thermal treatment.

In this work, all electrical contacts for solar cell applications were produced by a semiautomated screen printing machine. At first, the screen printing process was optimized by varying screen printing parameters, until the resulting printed structures exhibited performances within a desired tolerance. Fig. 4.5a demonstrates a typical designed pattern micrograph for screen printing electrical contacts. Through the openings in the screen, which appear as dark stripes, various metal pastes may be printed on semiconductor substrates, followed by a thermal process to form the electrical contacts. Fig. 4.5b exhibits a micrograph of the screen printed structures of silver paste CE3104 on a sputtered zinc oxide layer. The printed film was then thermally treated for 5 minutes at 125 °C in an air flow oven. The shape and the dimensions of the screen printed structures correspond to the pattern of the screen, however, the silver paste may spread during the screen printing process, which sets the limitation of fine line printing to approximately 100 μm.

4.3 Requirements for front side metallization

Metal pastes used to form screen printed electrical contacts contain two main components. The first component consists of an organic binder and a low vapor pressure solvent. The binder and solvent determine the viscosity of the metal paste, which is the key parameter in fine line printing. The component consists of fine metal particles which ensures a high lateral conductivity and governs the electrical properties of the final contact.

Certain requirements must be met in order to use metal pastes for the fabrication of front electrical contacts on CIGS solar cells. A metallic paste should establish sufficient mechanical contact with the substrate, or as in the case of front electrical contacts of CIGS thin film solar cells, a paste ought to provide good adhesion with to a layer of transparent conductive oxide (TCO). The commonly used technique for testing the adhesion quality of a manufactured electrical contact is the scotch tape test. Scotch tape is applied on a sample with screen printed electrical contacts for certain duration of time, and then swiftly removed. The amount of residuals on the tape indicates the adhesion quality. Moreover, printed pastes must be chemically inert for solar cells and module components.

The specific resistance, or resistivity, of deposited metal films must be kept a minimum as to reduce losses in the front contact grid which contributes to the series resistance of a solar cell. The optimal value for the sheet resistance of metallic films should not exceed $2 \cdot 10^{-4}$ Ω. The resistivity a metal paste may be further improved by using higher drying temperatures to remove any residual organic binders, but to avoid degradation with CIGS solar cells, the thermal treatment of the screen printed electrical contacts should not exceed temperatures of 170 °C. Low annealing temperatures may also permit the use of metal pastes within devices processed on plastic substrates. In addition to annealing temperature limitations, the annealing time should be kept as short as possible in order to minimize fabrication costs.

In the Chapter 3, it was demonstrated that one of the main contributors to the series resistance of solar cells is the contact resistance of the interface between a metal and a semiconductor layer. In the case of thin film solar cells, the screen printed metal pastes must provide low resistivity electrical contacts with transparent

conductive oxide layers. Fig. 4.6 demonstrates the influence of the specific contact resistance of the metal-TCO interface on the conversion efficiency of a CuInS (CIS) thin film solar cell. The given model assumes the width of printed fingers of 100 µm and a sheet resistance of 10 Ω for the TCO layer, while neglecting other contributing influences to the solar cell series resistance [9]. The influence of the specific contact resistance on the efficiency can be divided in two regions. For the values below 10 $m\Omega cm^2$, the conversion efficiency is independent on the performance of the front electrical contacts. As the specific contact resistance of metal-TCO electrical contacts increases above 10 $m\Omega cm^2$, the conversion efficiency of CIS solar cells drop, and this drop becomes more prominent as the specific contact resistance increases further. Hence, metal pastes used in the fabrication of the front contact grid on CIS solar cells must result in an electrical contact with a specific contact resistance below 10 $m\Omega cm^2$.
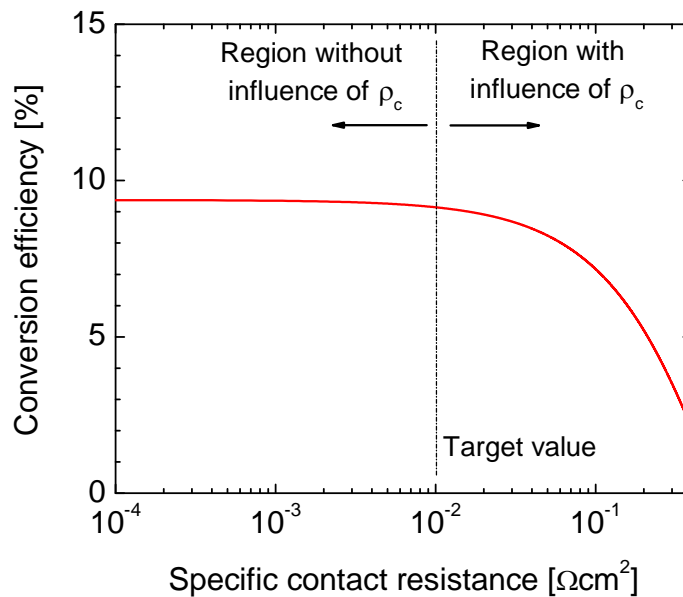
Fig. 4.6 Influence of the specific contact resistance on the efficiency of CIS solar cell.

Furthermore, metal pastes must fulfill the fine printed line requirement in order to be used for screen printing of grid fingers and bus-bars of a solar cell. As explained in the Chapter 3, the geometry of the front contact grid influences the series resistance of the solar cell, and therefore the conversion efficiency is as well affected. Fig. 4.7 demonstrates the dependence of the conversion efficiency of a CIS solar cell on the geometry of printed fingers. A 10 cm x 10 cm solar cell has been used as a model,

with a 10 Ω sheet resistance of the TCO layer and a specific contact resistance between the front contact grid and the TCO layer of 1 mΩcm^2. A low value of ρ_c has been selected in order to minimize the influence of the front contact grid resistance in the total series resistance of the solar cell. When the spacing between fingers is small, the solar cell is largely shadowed resulting in a reduced conversion efficiency. As the finger spacing increases, the conversion efficiency increases until a maximum value is reached. At maximal conversion efficiency, the more light that enters the cell outweighs the liability of the increased series resistance on account of the increase in finger spacing. For the optimal spacing between fingers when the optical benefits are canceled with resistive losses in the solar cell, the conversion efficiency reaches its maximal value. After this point when the conversion efficiency of the solar cell is maximized, further increasing the finger spacing results in increasing the series resistance, and hence the conversion efficiency drops.
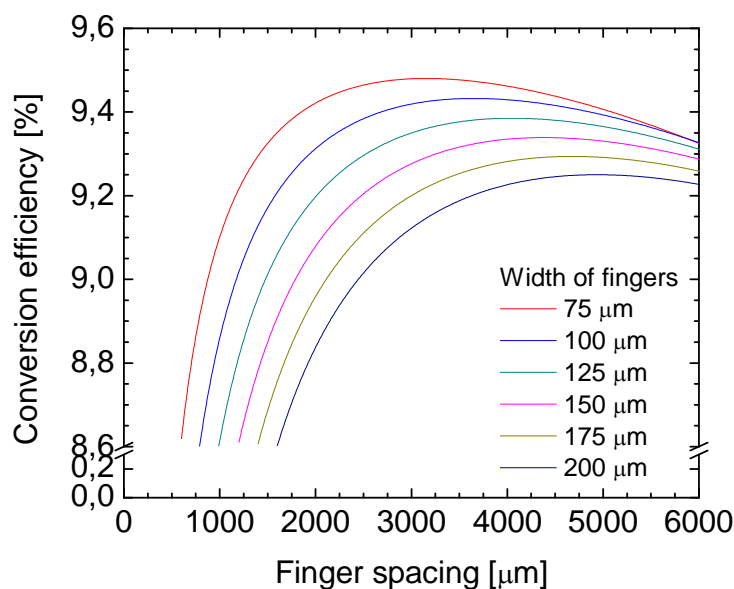
Fig. 4.7 Influence of the geometry of printed contacts on the efficiency of a CIS solar cell.

A higher conversion efficiency may be reached by further narrowing the fingers. As the width of the fingers reduces, the conversion efficiency increases as a result of more light shining on the solar cell. Furthermore, as the width of the fingers reduces, the optimal finger spacing when the conversion efficiency is maximized reduces as well as a result of the increase in the series resistance of the solar cell.

Finally, the screen printed metal pastes must fulfill a reliability performance. The properties of the electrical contacts must perform without deviation in their functionality and in the appearance of the solar cell under an accelerated aging test. The long term reliability test, also known as the damp heat test or simply as the aging test, is carried out at elevated temperatures of 85 °C and 85% relative air humidity. Electrical devices and their components are typically exposed for 1000 hours to such harsh conditions.

Silver paste	Manufacturer	Average size of silver flakes	Binder/Solvent	Curing temperature
CE 3104	Emerson & Cuming	~ 1000 nm	Not available	Above 120 °C
PV410	DuPont Ltd.	~ 100 nm	Dipropylenglykol-monomethylether	Above 120 °C
TEN	Advanced Nano Products	~ 5 nm	α-Terpineol	Above 120 °C
TESN5050	Advanced Nano Products	~ 80 nm	α-Terpineol	Above 120 °C
TES	Advanced Nano Products	~ 600 nm	α-Terpineol	Above 120 °C
TESM8020	Advanced Nano Products	~ 1000 nm	α-Terpineol	Above 120 °C

Table 1 List of silver pastes used in this study.

In this study, screen printed electrical contacts are formed by using various silver metal pastes, which are summarized in Table 1. These pastes contain more than 80% silver and are classified according to the average silver particle size. The solvents utilized in the pastes determine the minimal curing temperatures of the printed films. Silver pastes are then screen printed on various transparent conductive oxide films and CIS thin film solar cells. Within the subsequent two chapters, the properties of screen printed electrical contacts will be studied by evaluating the influence of various process parameters on the resulting electrical performance.

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Chapter 5

Front electrical contact on CIS solar cells in substrate configuration

5.1 Fabrication process of chalcopyrite CIS solar cell

In this section electrical contact effects on chalcopyrite $CuInSe_2$ (CIS) thin film solar cells are studied. The cross section of a typical chalcopyrite CIS solar cell is shown in Fig. 5.1 [1]. Thin film solar cells were deposited in the substrate configuration on a stainless steel foil. The active layer of the solar cell is then formed with a $CuInSe_2$ compound that performs with the thickness of a few micrometers. A majority of irradiative energy absorbs within this $CuInSe_2$ layer, and the electromagnetic energy then gets converted into the energy of electron-hole pairs. To form a good electrical contact, one must bridge the absorber layer and the rear electrode, so molybdenum was selected and a thin layer was deposited between the two. The deposition of the absorber layer was followed with a buffer layer of the solar cell, which provides the solar cell with optimal transparent and electrical junction with the front electrical contact. The most common materials used as buffer layers for the CIS solar cells are CdS and CuI. On the top of the buffer layer, a window layer has then been sputtered few hundreds of nanometer thick. The window layer of the solar cell plays a double role. First, it must perform with high optical transparency in order to avoid unnecessary losses due to reflection, and secondly, it must transfer the generated electrical charges towards the electrical contacts. Thus, the conductivity of this layer

must be high while minimizing the electrical losses in the layer itself. Due to high recombination rate of the charges in highly doped (highly conductive) materials, the engineering process of a satisfactory window layer that meets both requirements of high conductivity and minimized electrical losses is a formidable challenge, and has been in the focus of many research groups. The most commonly used materials as the window layer in thin film solar cell are the transparent conductive oxide (TCO) films: highly aluminum doped zinc oxide layers, Fig. 5.1a, and stacked aluminum doped zinc oxide layer with an indium tin oxide film, Fig. 5.1b.
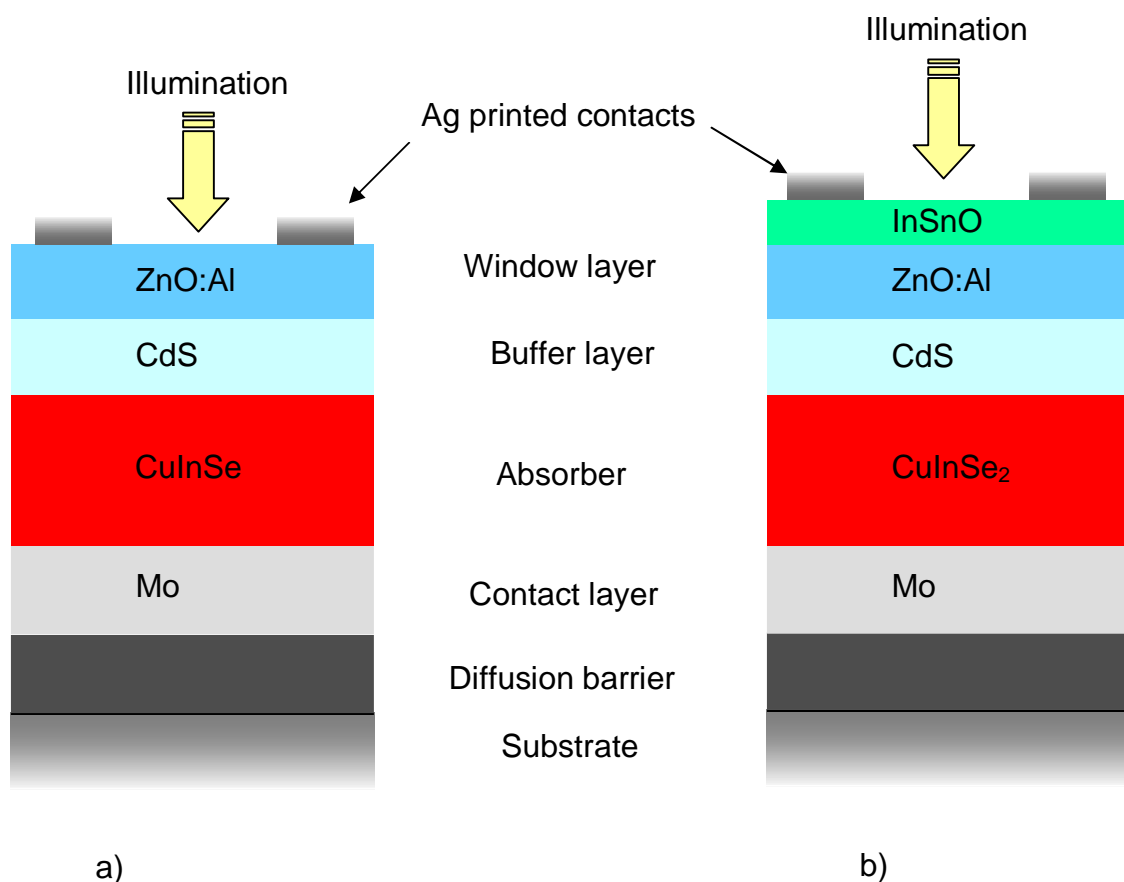
Fig. 5.1 The cross section of the CIS thin film solar cell with different window layers: a) aluminum doped zinc oxide and b) stacked of aluminum doped zinc oxide layer with an indium tin oxide film.

When the generated charges reach the conductive window layer, they transfer laterally towards metal contact electrodes. The metal electrodes are deposited on the front side of the solar cell by using different deposition techniques and various materials. Common materials used for front electrical contacts are nickel, aluminum,

and silver. This thesis will focus on silver paste screen printed electrical contacts as a possible solution for low cost and high reliable CIS solar cells. As previously explained, the front electrical contacts must perform with low resistive ohmic contacts with the window layer. As the front electrical contacts are deposited on prefabricated solar cells, the formation process of the front electrical grid has been limited with process parameters. During the thermal annealing process of the screen printed electrical contacts, the high temperatures may cause a destruction of the solar cell, and thus, the upper boundary for the process temperature of electrical contacts is set at 175 °C.

5.2 Electrical contacts on indium tin oxide and zinc oxide smooth films

Indium tin oxide (ITO) films are commonly used as conductive electrodes in electronic industries. In the photovoltaic industry, ITO layers are used as a front transparent conductive electrode. In this study, silver pastes were screen printed on the ITO films in order to study behavior of the electrical contacts. ITO was sputtered at room temperatures on a glass substrates with a thickness of approximately 200 nm. These ITO sputtered films performed with a sheet resistance of 20 Ω and a root mean square (RMS) roughness of approximately 3-5 nm. Silver pastes with various silver particle sizes were screen printed on the sputtered ITO films, followed by a thermal process, and the contact resistance of the rendered contacts was determined with the TLM method. The silver pastes consist of 70-80% silver particles, with the remaining content belonging to various organic additives for better paste adhesion on the substrate. The average diameter of the silver particles in the pastes was 1 µm in the PV410 paste and 100 nm in the CE3104 paste. After screen printing of the silver pastes, the samples were annealed in an air flow oven, with the annealing temperature varied from 125 °C to 250 °C and an annealing time of 30 minutes. The resistivity of the screen printed silver films was measured in the range of 10^{-5} Ωcm, which allows one to neglect the voltage drop over the printed structures. The specific contact resistance of silver screen printed electrical contacts on ITO substrates is given in Fig. 5.2a. The silver paste containing large silver particles of 1 µm exhibits

the highest specific contact resistance, and exceeds 10^{-2} Ωcm^2 at low annealing temperatures. As the annealing temperature exceeds 200 °C, the specific contact resistance drops below 10^{-4} Ωcm^2. For the silver paste containing 100 nm large particles, the specific contact resistance decreases when the process temperature increases, and the specific contact resistance was determined to be below 10^{-4} Ωcm^2, irrespective of the annealing temperature.
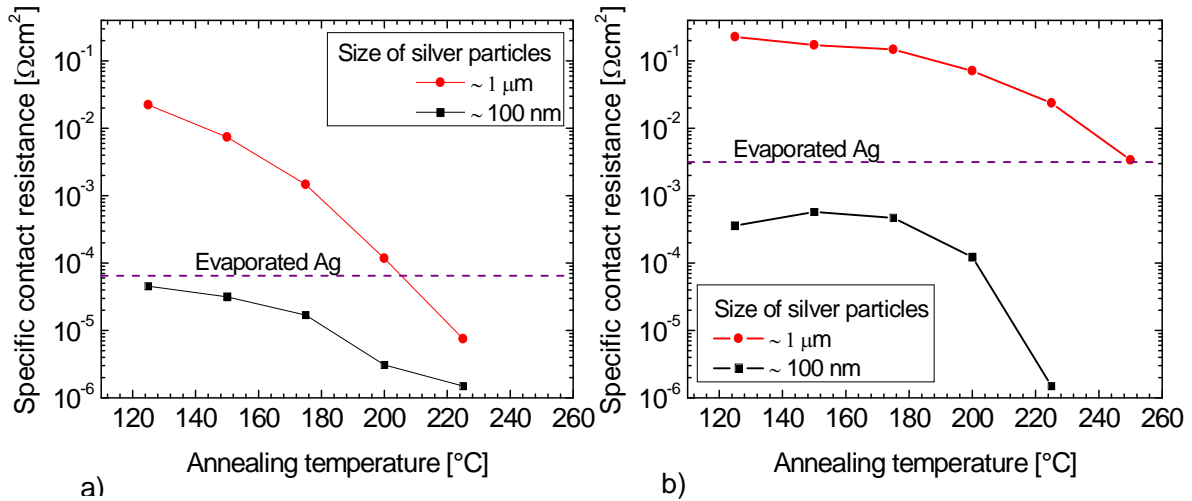
Fig. 5.2 The influence of the annealing temperature on the specific contact resistance of silver screen printed electrical contacts on a) indium tin oxide and b) aluminum doped zinc oxide films for a variety of annealing temperatures. The size of the silver particles in the paste was varied, and the dashed line represents the specific contact resistance of the evaporated silver electrodes on the ITO films.

In addition to screen printed electrodes, silver contacts were thermally evaporated on the ITO films while not thermally treating the samples themselves. Evaporated silver electrodes exhibited the specific contact resistance of $0.6*10^{-4}$ Ωcm^2, which is in a good agreement with values observed in literature [2] and may be taken as the lower limit for the untreated silver-ITO electrical contacts.

The screen printed silver electrical contacts in silicon based solar cells are typically treated at temperatures exceeding 700 °C. When annealed at elevated temperatures, silver particles begin to diffuse in the layer that the paste is in the contact with, and hence the contact resistance is reduced. In the case of CIS solar cells, annealing temperatures are much lower than the typical annealing temperature where diffusion may occur, and thus the diffusion effect of the silver into ITO films may be excluded.

Therefore, the drop in the specific contact resistance may most likely be attributed to the evaporation of the solvents in the paste. As the annealing temperature increases, the amount of residual solvent in the paste reduces, and thus the specific contact resistance decreases.

Due to economic demands, the entire electronics industry, and specifically photovoltaics, strives toward competitive innovations with exceedingly more fiscally viable materials. As of recently, zinc oxide (ZnO) films have been studied in the hope to replace ITO as the window layer in the solar cells 68[3]. Acceptable electrical and optical properties of the ZnO films are obtained when these films are doped with aluminum. Therefore, as a possible solution for the low cost CIS solar cells, the screen printed silver electrodes were deposited on aluminum doped ZnO (ZnO:Al) layers and their electrical contact properties studied..

The specific contact resistance of screen printed silver electrical contacts on ZnO:Al films is depicted in Fig. 5.2b. The film thickness of sputtered ZnO:Al films comprised of approximately 200 nm and a root mean square roughness of approximately 5 nm. The silver paste which contained larger silver particles of 1 μm rendered electrical contacts with a specific contact resistance of 10^{-1} Ωcm^2 at low annealing temperatures of 125 °C, dropping significantly with an increase in annealing temperature to the point where in excess of 220 °C the specific contact resistance reduced to merely 10^{-3} Ωcm^2. Similarly, by reducing the average size of the silver particles to 100 nm leads to a distinct drop of the specific contact resistance by a factor of 200. Again, as the annealing temperature increases, the printed electrical contacts demonstrated a drop of the specific contact resistance in the same manner as printed contacts on ITO layers.

In addition to the screen printed contacts, silver electrical contacts were formed with ZnO:Al by thermal evaporation without further treatment of the electrodes, producing contacts with a specific contact resistance of $3\bullet10^{-3}$ Ωcm^2. This lower contact resistance value of screen printed electrodes with 100 nm large silver particles then by evaporated silver can best be described as a result of better adhesion of printed films on the ZnO:Al films.

By comparing the electrical properties of the screen printed silver contacts between ITO and ZnO:Al films, one can observe that silver pastes, regardless in their particle size, yield a higher contact resistance on ZnO:Al substrates by approximately tenfold.

This difference in the electrical properties can most likely be attributed to the difference of the work function for the two TCO layers [4], [5].

5.3 Screen printed electrical contacts on CIS solar cells

The electrical contacts of PV410 silver paste with a silver grain size of approximately100 nm on smooth ZnO:Al films exhibited a contact resistance below 1 $m\Omega cm^2$. On account of its low contact resistance, PV410 silver paste was screen printed on CIS solar cells with ZnO:Al as the window layer.
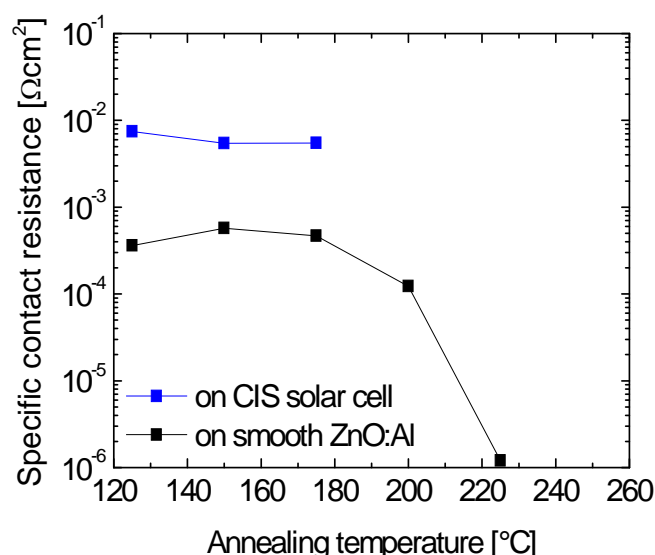
Fig. 5.3 Comparison of electrical contacts printed with silver paste containing 100 nm large silver particles on smooth and textured ZnO:Al films, and comparison with contacts printed on CIS solar cells.

Fig. 5.3 depicts the influence of the annealing temperature on the specific contact resistance of silver-aluminum doped ZnO contacts on two different types of ZnO films with approximately the same film thickness, the smooth sputtered ZnO and the CIS thin film solar cell with a ZnO:Al window layer. The electrical contacts on the solar cells were thermally treated to temperatures as high as 175 °C in order to avoid overheating and the destruction of the solar cells. The electrical contacts on the CIS solar cells performed with higher contact resistance, and the specific contact resistance was determined to be 10-50 times higher than smooth ZnO films. One

possible explanation for this increase of the specific contact resistance may be the increased interface roughness between the screen printed silver electrodes and the ZnO layer. Additionally, as the annealing temperature increased, the specific contact resistance of the silver electrodes on CIS solar cell demonstrated a slight decrease in value. Both, electrical contacts performed with a specific contact resistance below 10 mΩcm^2.

5.4 Electrical contacts on textured ZnO films

Due to the sputtering process of the various CIS solar cells layers, the final layer of the solar cell, an aluminum doped ZnO, comprised of a rough surface. Though this rough surface was unintentional, it may lead to better light trapping and higher conversion efficiency of thin film solar cells [6], but on the other hand this roughness may incur a higher contact resistance of the front electrical contact grid. In order to examine the influence in CIS solar cells of surface roughness on the electrical contact behavior, films with various degrees of surface roughness require investigation. In this study, electrical contacts were screen printed on textured surfaces of sputtered ZnO:Al films. The most common technique for texturing the surface of ZnO layers is by wet chemical etching. This controlled etching process was accomplished by etching the ZnO films with hydrochloric acid (HCl) solutions [7]-[9]. Sputtered ZnO films were exposed to 0,5% solution of HCl, and the roughness of the ZnO films was controlled by the duration of etching in the acidic solution. Fig. 5.4a depicts the dependence of the RMS roughness on sputtered ZnO films with respect to the duration of etching. When merely treated for 5 seconds in 0.5% HCl, the roughness in ZnO films increased to approximately 25 nm. As the etching time further increases, the RMS roughness increases linearly, reaching upwards to approximately 50 nm when treated for 30 seconds. Once ZnO films are textured for longer durations than 20 seconds they begin to exhibit an RMS roughness comparable with roughness values of CIS solar cells [10]. Atomic force microscope (AFM) images of textured, 20 seconds of etching in 0.5% HCl, and a non-textured ZnO layer are depicted in Fig. 5.4b and c, respectively. After the etching process, films were then rinsed in deionized water.
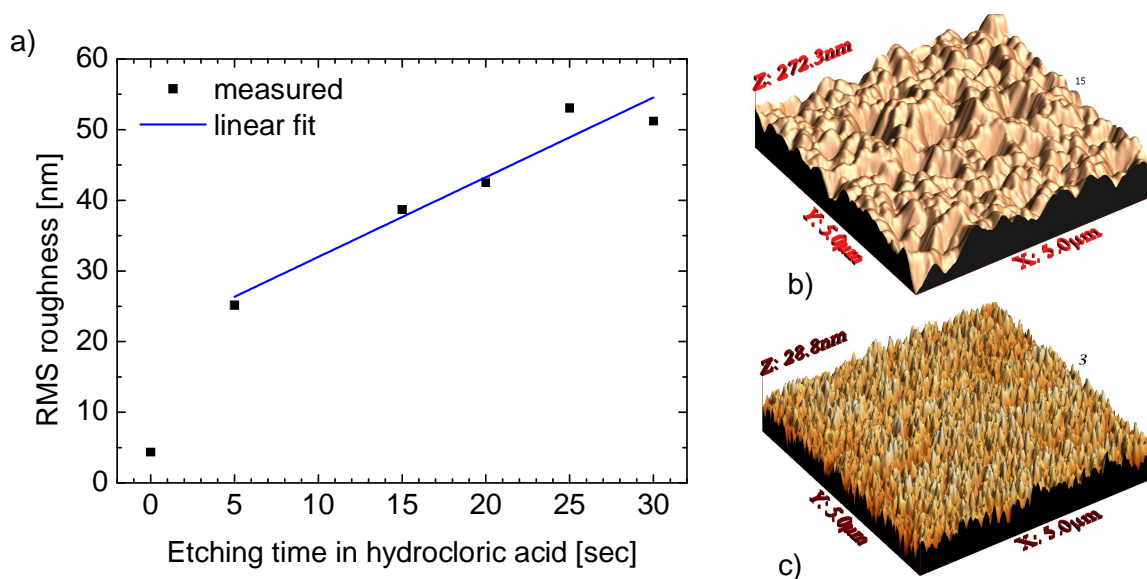
Fig. 5.4 a) Increase of the surface roughness of ZnO films during the etching process in 0,5% HCl. b) The surface morphology of sputtered ZnO films after 20 seconds of treatment in 0,5% HCl solution. c) The AFM graph of the smooth aluminum doped ZnO layer.

After the etching process comprising of 20 seconds in 0.5% HCl, PV410 silver paste containing 100 nm silver particles was screen printed on the textured ZnO layers. The electrical contacts were then annealed in the oven at various temperatures and the properties of the electrical contacts were determined by the TLM method. Fig. 5.5 depicts the comparison between the contact properties of screen printed electrical contacts on smooth and textured ZnO films, alongside with those deposited on a CIS solar cell. As the process temperature increased, the specific contact resistance on textured ZnO layers exhibited a specific contact resistance of approximately 10 $m\Omega cm^2$ with only slight variations for all annealing temperatures. Furthermore, one can observe that the values of the specific contact resistance on textured ZnO films and solar cell exhibited similar values at different process temperatures. While keeping this similarity in specific contract resistance values in mind, and recognizing that the surface roughness of textured ZnO films is comparable with the roughness of CIS solar cells, one may utilize the model of textured ZnO films for further studies of contact properties for CIS solar cells with a ZnO:Al window layer.

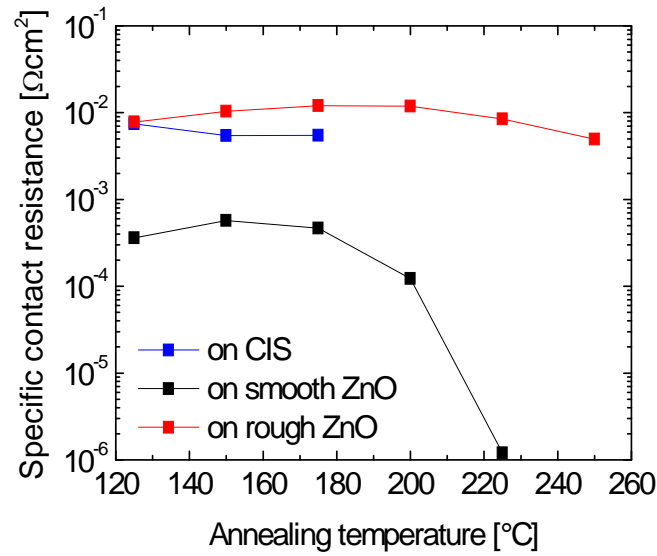Fig. 5.5 Comparison of electrical contacts printed with silver paste containing 100 nm silver particles on smooth and textured ZnO films, and in comparison with contacts printed on CIS solar cells.

Silver paste with 100 nm and 1µm silver particles were printed on the textured ZnO:Al films that were textured for various durations in hydrochloric acid, and subsequently annealed for 30 minutes in an air flow oven. In the case of silver paste with a particle size of 1 µm, the specific contact resistance could not be determined by the TML method on account that the contacts formed between the silver paste and the textured ZnO films were not reproducible. In the case of the paste containing 100 nm silver particles, the influence of the annealing temperature on the specific contact resistance is depicted in Fig. 5.6a. As the roughness of the textured films increases by increasing the etching duration, the specific contact resistance of the Ag-ZnO contacts increases as well. For low annealing temperatures between 125 °C and 175 °C, the specific contact resistance increases by 10-30 folds in comparison to the smooth non-textured sputtered films, and further increasing the annealing temperature results in even larger difference in the specific contact resistance. When ZnO substrates were etched for longer durations, the annealing temperature demonstrated a negligible influence on the specific contact resistance.

Assuming no change in the barrier height of Ag-ZnO contacts, the observed increase of the contact resistance on the rougher films implies that the effective contact area

of Ag-ZnO interface may be reduced due to the rougher surface of textured ZnO films.
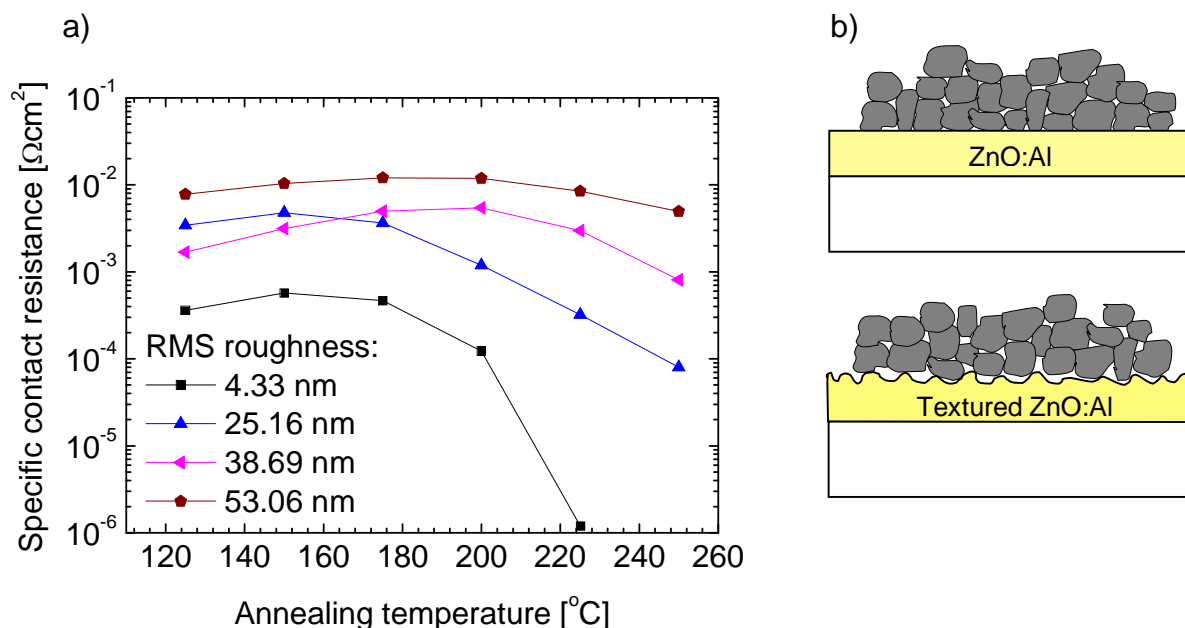
Fig. 5.6 a) Annealing temperature influence on the specific contact resistance of screen printed contacts on textured aluminum doped ZnO films. b) An illustration of the contact interface between silver particles deposited on smooth and textured ZnO films.

The higher values of the specific contact resistance of electrical contacts on textured ZnO films then on smooth films may be related to a reduction in surface coverage of silver particles on the ZnO substrate. On rougher surfaces, silver particles do not cover the surface in the same manner as in the case of smooth substrates, Fig. 5.6b. Silver particles on the textured surfaces render cavities and voids, diminishing the effective contact area, thereby increasing the specific contact resistance.

Fig. 5.7 depicts the influence of etching duration of ZnO films on the specific contact resistance of screen printed electrical contacts when PV410 silver paste containing 100 nm silver particles is utilized. Printed electrical contacts were annealed at 125 °C, 150 °C, and 175 °C for 30 minutes. This 50 °C processing temperature range was specifically selected since 125°C is the lowest temperature permissible to form electrical contacts from PV410 silver paste, while 175°C is the highest processing temperature used for the formation of front electrical contact grids in CIS solar cells. For the shortest etching duration of 2 seconds for ZnO films in 0.5% HCl, the specific

contact resistance increased one order of magnitude in comparison with smooth films. Any further increase in surface roughness is followed with a slight increase of the specific contact resistance, reaching up to 10 mΩcm^2 for ZnO films textured for 30 seconds. The process temperatures did not impart a pronounced influence on the specific contact resistance, despite that the electrical contacts fabricated at the lowest annealing temperature performed with the lowest contact resistance.
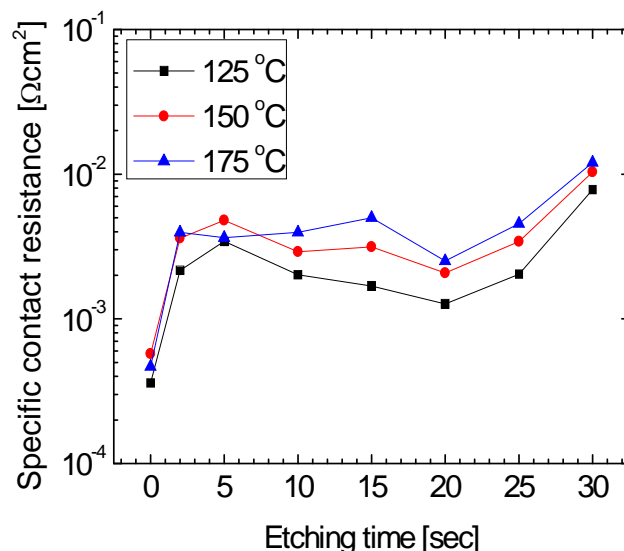
Fig. 5.7 Influence of the surface roughness of ZnO films and annealing temperature on the specific contact resistance of screen printed contacts using the silver paste with 100 nm large silver particles.

5.5 Influence of the annealing time on the contact properties

Until now electrical contacts were annealed in an air flow oven for 30 minutes at various temperatures. While the process time is one of the key parameters that influence the final price of the finished product, the annealing time of the screen printed electrical contacts should also be shortened, and this shortening should not affect the contact properties of Ag-ZnO contacts. The PV410 silver paste containing 100 nm silver particles was screen printed on smooth and textured ZnO films, utilizing a 50 seconds etching duration in 0.5% HCl solution, as well as on smooth ITO films. Fig. 5.8 depicts the behavior of electrical contacts that were annealed at

150 °C at various process durations. The annealing time was varied from 5 minutes to 2 hours of processing and one may observe that after five minutes of annealing process, electrical contacts on the various semiconductor layers demonstrated stable values of specific contact resistance. In agreement with previous results, the lowest specific contact resistance occurs for contacts printed on ITO films while the largest occurs for the textured ZnO films.
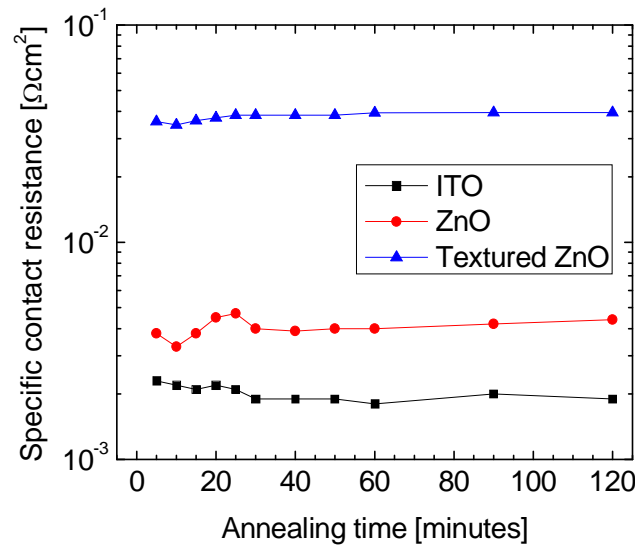
Fig. 5.8 Influence of annealing time on the performance of screen printed electrical contacts with 100 nm silver particles on various substrates. All contacts were annealed at 150°C.

5.6 Nanoparticle silver pastes

Very rough ZnO films resulted in electrical contacts with values of the specific contact resistance greater than 10 mΩcm^2. As a result of the screen printed electrical contacts performing poorly due to poor surface coverage when deposited on textured zinc oxide films, a possible remedy to improve the specific contact resistance may be to utilize silver pastes with contain smaller silver particles. Silver particles were tailored an average diameter of 5 nm, 80 nm, 600 nm, and 1000 nm, and were uniformly dispersed in α-Terpineol with a volume ratio of 3:1 [11]. The prepared silver pastes were screen printed on sputtered ZnO:Al films, and thermally treated in an air

flow oven. The contact resistance of screen printed silver contacts on sputtered ZnO films was measured for the silver pastes containing particles of different sizes, and the specific contact resistance of such electrical contacts was determined by the TLM method.

Fig. 5.9 Influence of the annealing temperature on the screen printed silver electrical contacts on smooth ZnO sputtered films with varying size of silver particles contained in the silver pastes utilized.

Fig. 5.9 shows the influence of the process temperature on the specific contact resistance of silver printed contacts on smooth sputtered zinc oxide films. The silver paste containing largest particles exhibits a specific contact resistance above 10^{-2} Ωcm^2 at the lowest annealing temperature, while with increasing the annealing temperature up to 200°C the specific contact resistance drops logarithmically to approximately 10^{-3} Ωcm^2. With the exception of the 5 nm particle silver paste, the 80 nm and 600 nm particle silver pastes also follow this trend, with their specific contact resistance dropping to values of 10^{-3} Ωcm^2 with increasing temperature. As the average size of silver particles in the paste reduces, the specific contact resistance on smooth ZnO substrates reduces as well. The paste with silver particles of 80 nm exhibited a 4 fold lower specific contact resistance for all process temperatures in comparison with silver paste containing particles of several microns. Further reduction in the silver particle size approximately 5 nm reduces the specific contact resistance to below 10^{-4} Ωcm^2 for annealing temperatures above 150°C. The drop of

the specific contact resistance for 5 nm silver contacts between the annealing temperatures of 125 °C and 150 °C can be attributed to the complete evaporation during annealing of the solvent from the paste deposited during printing.

In order to investigate the influence the roughness on the contact resistance of a thin film solar cell, zinc oxide substrates were textured by wet chemical etching by immersing sputtered ZnO substrates for 20 seconds in 0.5% hydrochloric acid solution. The films exhibited a RMS roughness of approximately 40 nm, which is approximately 8 fold greater than the RMS roughness of non-textured sputtered ZnO films. The resulting influence of the particle size in silver pastes and the process temperature on the specific contact resistance of printed electrical contacts on textured ZnO films is depicted in Fig. 5.10a.
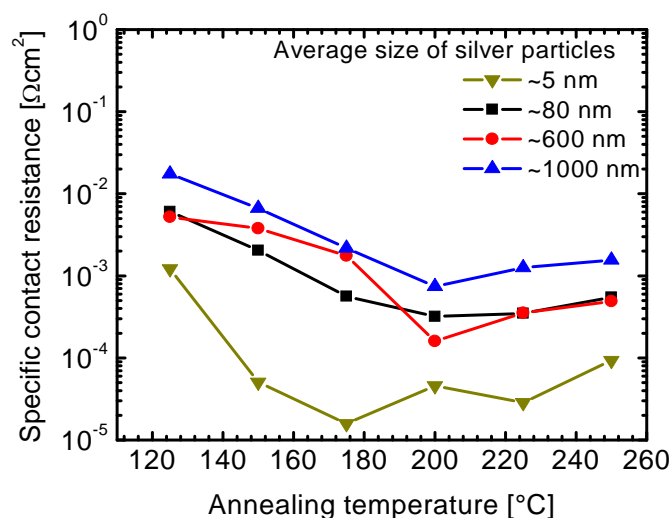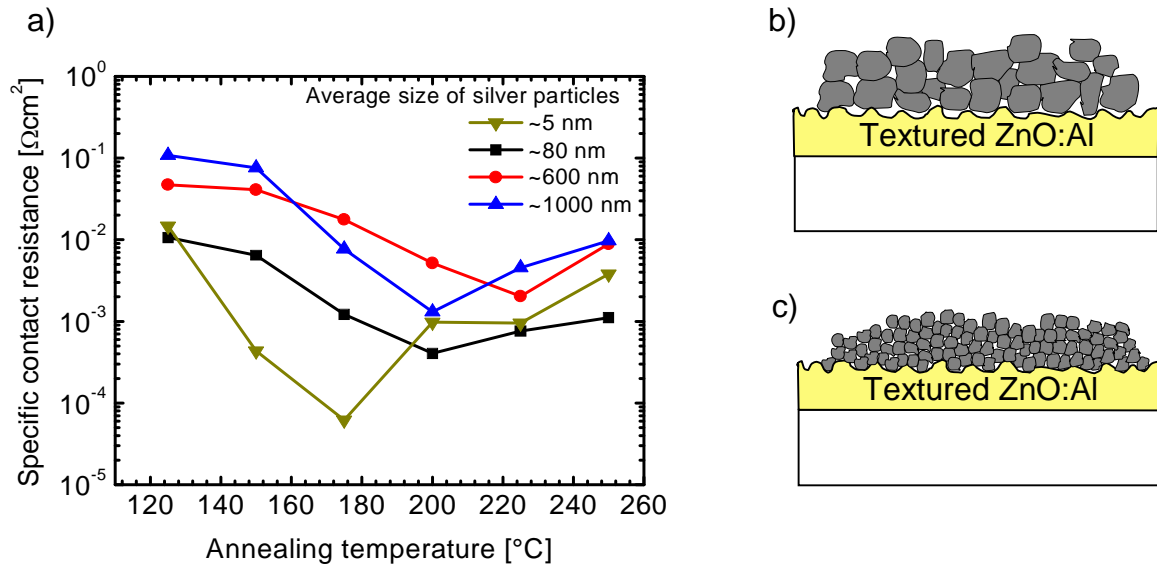

Fig. 5.10 a) Influence of the annealing temperature on the screen printed silver electrical contacts on the textured ZnO films with varying particle size in the silver pastes. b) Illustration of the surface coverage with silver paste containing larger grain sizes. c) Illustration of the surface coverage with silver paste containing nanoparticles.

The highest specific contact resistance occurs for the TESM8020 silver paste containing 1 µm silver particles exceeds 100 $m\Omega cm^2$ after annealing at lower temperatures. As the annealing temperature increases, the specific contact resistance of Ag-ZnO contacts decreases, so much so that the TESM8020 paste ultimately renders yields a specific contact resistance of 2 $m\Omega cm^2$ when processed at

200°C. As the silver particle size decreases, a drop in the specific contact resistance of the Ag-textured ZnO contacts occurs. When using the nanoparticle silver paste, printed contacts perform with a specific contact resistance of 10 mΩcm^2 at low annealing temperatures of 125°C, but drops three orders of magnitude to below 0.1 mΩcm^2 and as the temperature increases to 175 °C. The general trends of pastes with smaller particle sizes exhibiting a lower contact resistance in Ag-textured ZnO contacts can be seen, and the reason for such behavior may be a result of better surface coverage on the textured ZnO surface when smaller silver particles pack upon annealing, as illustrated in Fig. 5.10b and c. When printed, the large silver particles on the textured surface of ZnO may lead to uncovered areas of the contact interface, creating cavities and not filling voids on the textured surface, which effectively reduce the contact area, and incur a higher contact resistance. In the case of the nanoparticle paste, the small silver particles are more effectively able to cover the larger area of the contact interface, thereby leading to a lower contact resistance. By comparing results from the smooth ZnO films, one concludes that all four silver pastes of varying particle size increased the specific contact resistance of printed silver contacts on textured ZnO films. When printed on rougher films, the two silver pastes with 600 nm and 1000 nm silver particles exhibited specific contact resistance 5-10 fold greater then values obtained from non-textured films. By comparing smooth to textured films, the specific contact resistance of the contacts with silver paste containing 80 nm silver particles doubled. In the case of the 5 nm silver particle paste, the fabricated electrical contacts performed with the lowest specific contact resistance, below 10^{-4} Ωcm^2, when annealed at 175°C. Increasing the process temperature, electrical contacts printed with silver pastes based on α-Terpineol (TEN, TESN5050, TES, and TESM8020) demonstrated a reduction in the specific contact resistance, but as the annealing temperature increases to 200°C, the solvent from the printed films vaporizes, thereby increasing the effective contact area on Ag-ZnO interface and reducing the specific contact resistance. Beyond 175°C, any further increase in the process temperature does not reduce the contact resistance in printed contacts, moreover, a slight increase in the specific contact resistance occurs when contacts are annealed at elevated temperatures above 200°C. This slight increase in the specific contact resistance may be related to the evaporation of chemical binder used in the silver paste enabling contact with the surface, and thus

the contacts exhibit poor adhesion with textured ZnO films and higher contact resistance.

Despite that the electrical contacts printed with the 5 nm particle containing silver paste performed with low contact resistance values, the high price of silver nanoparticles would result in high priced CIS solar cells. The more complicated manufacturing process involved to produce nanoparticulate silver, the price of the silver nanoparticle paste would be 3-4 times the cost of silver paste with 80 nm silver particles, and more than 10 times more expensive then pastes with even larger silver particles. Thus, a compromise between price and performance of the electrical contacts has to be resolved. As the silver pastes with 600 nm and 1 µm silver particles do not satisfy the necessary specific contact resistance requirement, and since the silver nanoparticle paste is economically unfeasible for commercial production, the remaining silver paste containing 80 nm silver particles, TESN5050, appears to be the sole option of the pastes investigated which fit the ideal characteristics desired.

The sputtered ZnO substrates were textured in HCl for various etching durations, and ZnO films exhibited the RMS roughness from approximately 5 nm for non-textured films to approximately 50 nm for the films etched for 30 seconds. The silver paste containing 80 nm particles was screen printed on textured ZnO films, and the specific contact resistance of such electrical contacts was determined and presented in Fig. 5.11, which depicts the influence of the annealing temperature and the surface roughness on the performance of printed electrical contacts. As the surface roughness of textured ZnO films increases, the specific contact resistance of fabricated contacts increases as well. For low annealing temperatures between 125 °C and 175 °C, the specific contact resistance increases by factor of 4-5 when the RMS roughness of the films increases from 5 nm, such as smooth films, to 50 nm, as in the case of rough zinc oxide surfaces. As the annealing temperature increases, the specific contact resistance reduces. By utilizing silver paste with an average silver particle diameter of 80 nm affords the opportunity to achieve the specific contact resistance of a printed electrical contacts below 1 mΩcm^2, despite the fact that contacts were made on ZnO films with high degree of roughness.
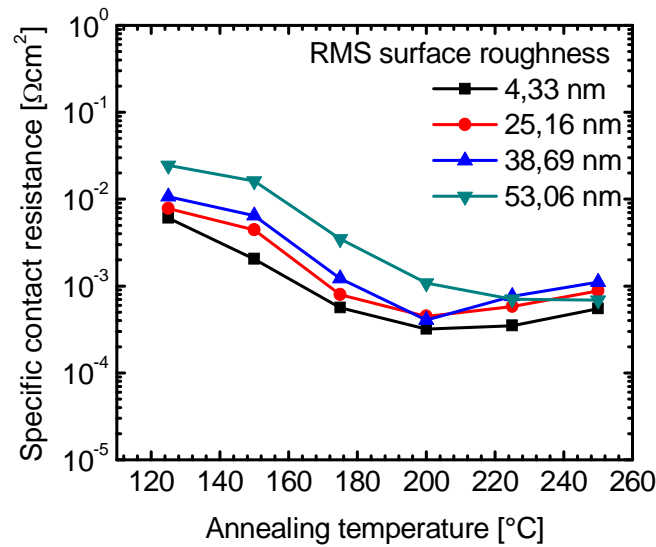
Fig. 5.11 The influence of annealing temperature and roughness of the sputtered ZnO films on the performance of screen printed silver electrical contacts. The silver particles in the paste were 80 nm in diameter.

Finally, the pastes with various sized silver particles were screen printed on CIS solar cells. The electrical contacts were formed by thermal treatment in an air flow oven, and the influence of the annealing temperature on the specific contact resistance of silver contacts on CIS solar cells is depicted in Fig. 5.12. After annealing at 125 °C, only TEN and TESN5050 silver pastes (with average sized of particles of 5 nm and 80 nm, respectively) performed electrical contacts with a specific contact resistance below the targeted value of 10 mΩcm^2. As the process temperature increases, electrical contacts printed with each silver paste performed with a lower specific contact resistance parameter. Furthermore, as the silver particle size decreases the contact performance improves. After annealing at 175 °C, the electrical contacts with the silver nanoparticle paste exhibited a specific contact resistance of 0.08 mΩcm^2, while contacts fabricated from TESN5050 silver paste performed with the specific contact resistance of 0.7 mΩcm^2.

The remaining two silver pastes, with particle sizes of 600 nm and 1 μm, when printed on CIS solar cells achieved a specific contact resistance slightly below 10 mΩcm^2 after annealing at higher temperatures.
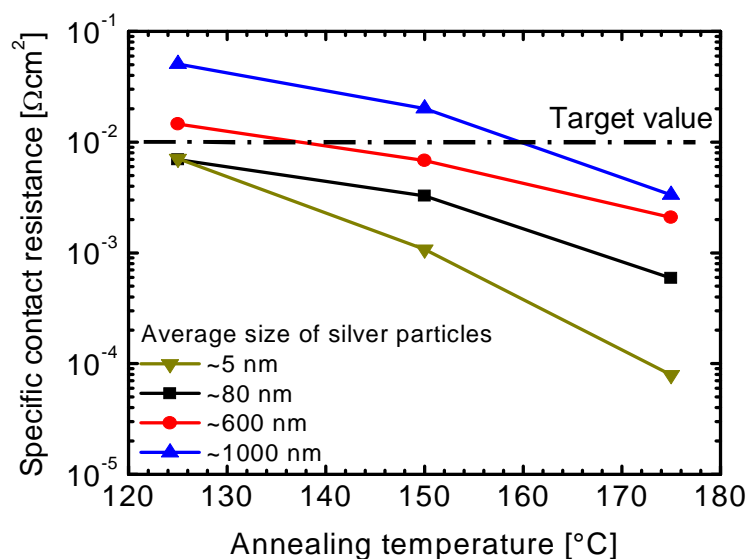
Fig. 5.12 The performance of electrical contacts utilizing a variety of silver particle containing silver pastes used to screen printed on the CIS solar cells

The values of the contact resistance obtained from the screen printed electrical contacts on the CIS solar cells are in a good agreement with results obtained from the textured ZnO substrates. Therefore, the texturing model of ZnO surfaces may be used for further studies of contact effects on CIS solar cell.

5.7 Summary

In this chapter, the formation of screen printed silver electrical contacts on aluminum doped zinc oxide and indium tin oxide as windows layers for CIS solar cells were investigated. Specifically, the influence of the annealing temperature on the formation of the printed silver contacts was investigated for silver pastes containing silver particles for a variety of sizes. Additionally, the formation of electrical contacts on transparent conductive oxides strongly depends on the surface roughness. For rough substrates, the specific contact resistance increased by a factor of 10 for lower annealing temperatures (125 - 175 °C), and several orders of magnitude at higher annealing temperatures (>200 °C). For rough substrates, the specific contact resistance is mainly determined by the surface roughness, while the annealing

temperature only plays a minor role. The increase in the specific contact resistance on the textured zinc oxide films is most likely caused by the reduced coverage of the surface with the silver particles. Surface coverage may be reduced by using silver nanoparticle pastes, and thus, the front contact resistance on textured ZnO films may as well be reduced. Silver nanoparticle paste reduces the specific contact resistance of screen printed electrical contacts on smooth and textured zinc oxide films, as well as on the CIS solar cells. Electrical contacts on textured zinc oxide films exhibited similar values of the specific contact resistance as to ones printed on CIS solar cells. Lastly, the RMS roughness of textured ZnO films perform with similar roughness as the surface of CIS solar cells, and furthermore, textured zinc oxide may be used as a model for studying the actual front surface of CIS solar cells.

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Chapter 6

Degradation effects of electrical contacts in thin film solar cells

In this chapter, the lifetime degradation effects of electrical contacts on CIS thin film solar cells are examined. In order to supply devices which last longer without compromising performance, the photovoltaic industry is turning towards novel materials. Solar cell components and the materials of which they are made are not environmentally resistant, and hence vital solar cell parameters degrade over time due to environmental aging effects. As with many aspects of the solar cell in which environmental aging effects, the front electrical contacts are amongst them. In order to understand degradation behavior with respect to front electrical contacts, the morphology of screen printed silver films was investigated. In the previous chapter, the surface roughness of ZnO films was shown to have a strong influence on the properties of Ag-ZnO electrical contacts, yet within this study, the degradation of various transparent conductive oxide layers will be investigated, in addition to the influence of process parameters on the long term stability of fabricated front electrical contacts. Afterwards, the influence of aging in front electrical contacts with respect to the long term stability of solar cell parameters will be presented.

6.1 Experimental

After the fabrication process of front electrical contacts, samples were stressed under elevated temperature and humidity. Such treatment is a commonly used procedure

for estimating the outdoor reliability and stability of solar cells and modules. The accelerated aging test, also known as the damp heat test (DHT, standard IEC 1215 of the International Electro technical Commission), is one of the commonly run analysis in order to test performance longevity of electronic and electrical devices [1]-[3]. The damp heat test has been shown to be highly reliable for predicting a devices' behavior within a set operating duration. Manufactured devices are placed in an environmental chamber and exposed to elevated temperatures of 85°C and a relative humidity of 85% for finite durations of time, known as the damp heat time. Screen printed electrical contacts were characterized with the transmission line method prior to and after the environmental stress. The degradation of transparent conductive oxide films and front electrical contacts were then examined.

6.2 Degradation effects of semiconductor thin films

The previous chapter demonstrated that the specific contact resistance of printed silver electrodes strongly depends on the work function of the TCO layer, as well as the surface roughness of the window layer. Front electrical grids were screen printed and the sheet resistance parameter characterized by TLM with various transparent conductive oxides (TCO) films: sputtered indium tin oxide (smooth ITO), sputtered aluminum doped zinc oxide (smooth ZnO), textured zinc oxide films and CIS solar cells. It was found that the performance of TCO films was not affected during the fabrication process of the front electrical contacts. . During the damp heat test, the TCO films were monitored for changes in the sheet resistance.

Fig. 6.1 demonstrates the change of the sheet resistance during the damp heat experiment for various TCO layers. All examined TCO thin films exhibited an increase in the sheet resistance during the damp heat time. Smooth ITO films exhibited a linear sheet resistance increase over the course of 1000 hours from 5 Ω to 7 Ω, while smooth non-treated ZnO films exhibit a similar behavior as ITO films yet reached a final value of 12 Ω over the same duration. Concurrently, resistivity of the films increased due to the decrease of the carrier concentration and mobility with increasing damp heat time [4].
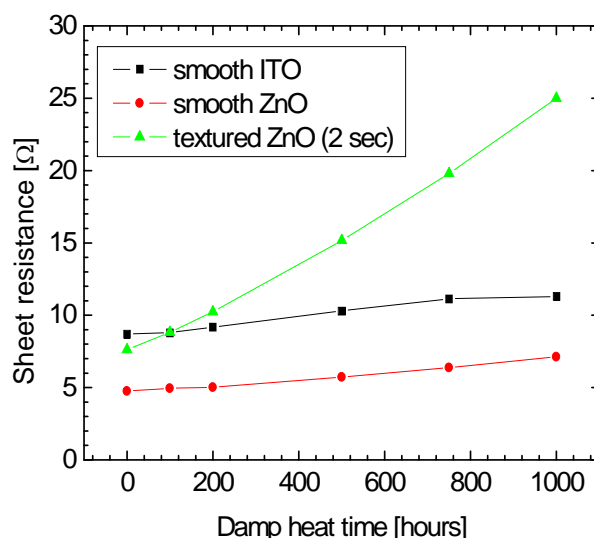
Fig. 6.1 Aging effects on the different transparent conductive oxide layers. Indium tin oxide (ITO), zinc oxide (ZnO), and an etched ZnO film, 2 seconds in dilute HCl, were analyzed.

In the case of textured ZnO films, the increase of the sheet resistance with damp heat time is more prominent. The ZnO films that were textured for 2 seconds in 0.5% hydrochloric acid (HCl) solution exhibited a stronger linear increase of the sheet resistance as compared to both smooth ITO and non-textured ZnO films. The sheet resistance shifted from 7.5 Ω to 25 Ω within 1000 hours of accelerated aging. During the etching process, the film thickness of textured ZnO films reduced and the RMS roughness increased in comparison with smooth ZnO films. The new morphology of the textured films allows for easier penetration of water and oxygen molecules in ZnO films [5], thereby rendering a stronger increase of the sheet resistance as compared to non-textured smooth ZnO layers.

Furthermore, sputtered ZnO films that were textured for a longer duration in diluted HCl exhibited an increase in their RMS roughness. Rougher ZnO films exhibited a stronger increase in sheet resistance during the damp heat test. Fig. 6.2 demonstrates the sheet resistance change on account of 15 seconds of dilute HCl etching on a ZnO film when damp heat time is applied, resulting in the sheet resistance increasing more than 30 fold when exposed to 1000 DH hours. A similar change of the sheet resistance during the aging experiment is apparent for CIS thin film solar cell, and both films exhibit the change of sheet resistance from ~10 Ω to

~300 Ω after 1000 hours of treatment in the climate chamber. On account of the similar aging effect between these two films affords the use of textured zinc oxide films as a model for further analysis of contact properties on CIS solar cells.
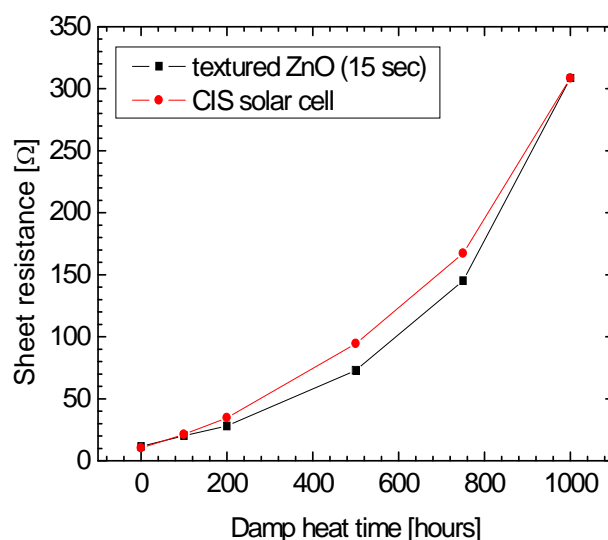
Fig. 6.2 Comparison of the sheet resistance change during the damp heat time for a CIS solar cell and textured ZnO films. ZnO films were textured for 15 seconds in the diluted hydrochloric acid.

Screen printed electrical contacts on CIS solar cells are formed by thermal annealing. The printed contacts were processed at various temperatures and over various durations in an air flow oven, and finally tested via accelerated aging. On account of an encapsulation layer which is placed over the solar cell module, the actual aging of CIS solar cells may be reduced. The encapsulation layer protects the solar cell from water and oxygen molecules, and therefore the aging study of solar cells does not require 1000 hours to test, and the damp heat time may be reduced. A set of CIS solar cells were prepared under identical conditions, and the silver electrical contacts were screen printed on top of the CIS solar cells. The screen printing process of silver pastes was followed by an annealing step, and the annealing process parameters for formation of front electrical contacts were varied. The electrical contacts were formed under following annealing conditions:

Sample A: 125 °C   5 minutes

Sample B: 125 °C   30 minutes

Sample C: 150 °C   5 minutes

Sample D: 150 °C   30 minutes

Sample E: 175 °C   5 minutes

Sample F: 175 °C   30 minutes

Fig. 6.3 summarizes the change of the sheet resistance of CIS solar cells in the first 200 damp heat hours due to the influence of the process parameters used for the formation of front electrical contacts.
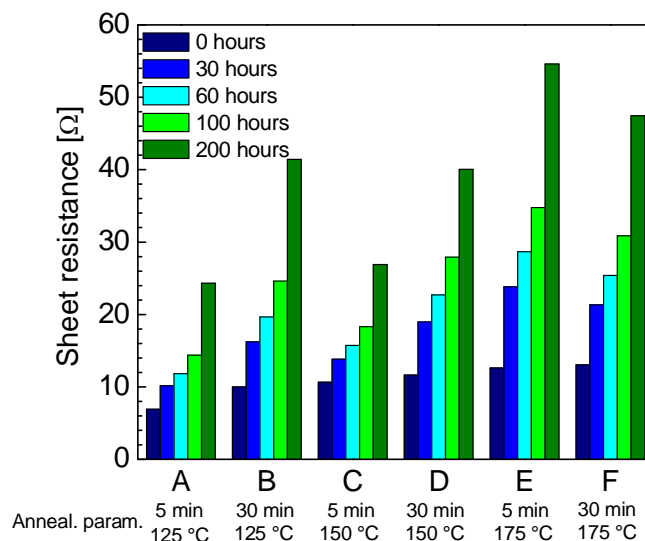
Fig. 6.3 The change of the sheet resistance of the CIS solar cells with damp heat time. The annealing parameters in forming the printed silver electrodes were varied.

The annealing parameters used in the formation of printed electrical contacts influenced the initial value of the sheet resistance. Sample A which was annealed for 5 minutes at the lowest temperature, 125°C, exhibits a sheet resistance of 7 Ω, while sample F which was annealed for 30 minutes at the highest temperature, 175°C, exhibited a sheet resistance of 13 Ω. One may therefore extrapolate that longer annealing durations and higher process temperatures for solidifying silver pastes increase the sheet resistance of CIS solar cells.

During the degradation experiment, the sheet resistance of CIS solar cells increased. By comparing samples that were annealed at identical temperature (samples A and

B, or samples C and D), one can see that the longer annealing duration during the formation of the electrical contacts for samples B and D increases the degradation rate of the sheet resistance. Samples annealed for 30 minutes, such as in samples B and D, exhibited higher values of the sheet resistance, exceeding 40 Ω after 200 DH hours, than samples annealed for 5 minutes, such as in samples A and C, with the values of the sheet resistance of 25 Ω. Furthermore, the annealing temperature imparts an influence on the degradation rate of the sheet resistance of analyzed CIS solar cells. CIS solar cell samples with screen printed silver electrodes annealed at different temperatures and all processed for the same duration in an air flow oven exhibit different sheet resistance values after 200 damp heat hours. Samples A, C, and E were all annealed for 5 minutes, yet at temperatures of 125°C, 150 °C, and 175°C, respectively. Sample E, annealed at the highest temperature, exhibited a faster degradation rate of the sheet resistance then samples annealed at lower temperatures Moreover, the sheet resistance of CIS solar cell sample E shifted from 12 Ω to 55 Ω during 200 DH hours, while the sheet resistance of sample A increases 3 fold within the same damp heat time.

Finally, the thermal process used in the formation of front electrical contacts imparts a substantial influence on the performance of CIS solar cell. As the annealing time and/or annealing temperature increase, the sheet resistance of CIS solar cells will be increased. During the aging of solar cells, the process parameters may be the reason for the sharper increase of the sheet resistance in CIS solar cells.

6.3 Degradation of electrical contacts on sputtered zinc oxide films

Adding to the degradation study of transparent conductive oxide layers and CIS solar cells, this subchapter shall focus on the aging effect on the performance of silver-TCO electrical contacts. The silver pastes with various sized silver particles were screen printed on sputtered ITO and ZnO films. Printed contacts were then annealed for 30 minutes in an air flow oven at 150°C. The specific contact resistance of aforementioned prepared samples was measured via the TLM method. Following the thermal treatment, samples were then exposed to accelerated aging in an environmental chamber. The contact properties measurements were performed

before and after the accelerated aging treatment. The TLM measurements were obtained after 100, 200, 500, 750 and 1000 DH hours. Fig. 6.4 shows the influence of the accelerated aging on the contact performance of printed silver electrical contacts on smooth TCO films. The electrical contacts of CE3104 silver paste, with micrometer large silver particles, on ITO substrates demonstrates an increase in the specific contact resistance of 3 fold after 1000 hours of accelerated aging. The specific contact resistance exceeded the value of 10mΩcm^2 after 1000 hours. In the case of electrical contacts on ZnO films, the CE3104 silver paste exhibits electrical contacts with very high initial specific contact resistance. After the initial measurement, the specific contact resistance could not be determined on account of the poor adhesion properties of the printed electrical contact. PV410 silver paste with average size of silver particles of 100 nm also exhibits an increase of the specific contact resistance when annealed as the contact on an ITO surface. The specific contact resistance increased from $4 \bullet 10^{-5}$ Ωcm^2 to $6 \bullet 10^{-4}$ Ωcm^2 after 1000 DH hours. A similar behavior occurs when the paste is printed on sputtered ZnO films. Values of the specific contact resistance on the ZnO surface are 10-20 times higher than on ITO substrates, reaching up to 7 mΩcm^2 after 1000 damp heat hours.
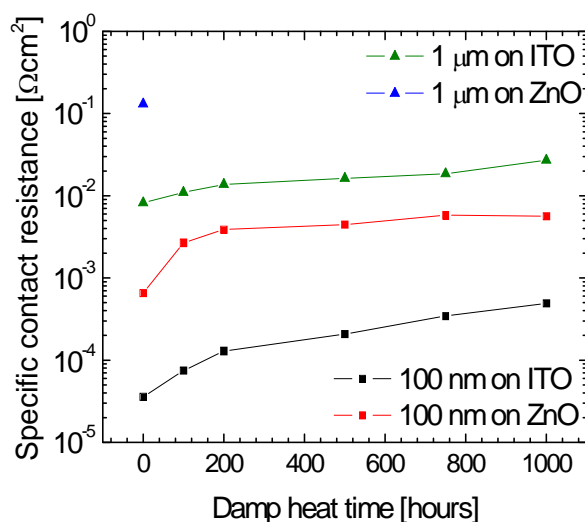

Fig. 6.4 The specific contact resistance of screen printed silver electrical contacts on smooth ITO and ZnO sputtered films. The size of silver particles in the pastes was 100 nm and 1µm.

Since the surface of the actual solar cell is rougher than the surface of sputtered ZnO, a similar experiment was repeated for textured ZnO surfaces. Texturing of the ZnO was done in diluted hydrochloric acid, in the same manner as explained in Chapter 5. Textured ZnO films were etched for different durations in a 0.5% HCl solution in order to render films with various RMS roughnesses. Silver paste with 100 nm large silver particles was screen printed, and samples were annealed at 150°C for 30 minutes. The influence of the surface roughness on the electrical properties of printed contacts during the damp heat experiment is depicted in Fig. 6.5.
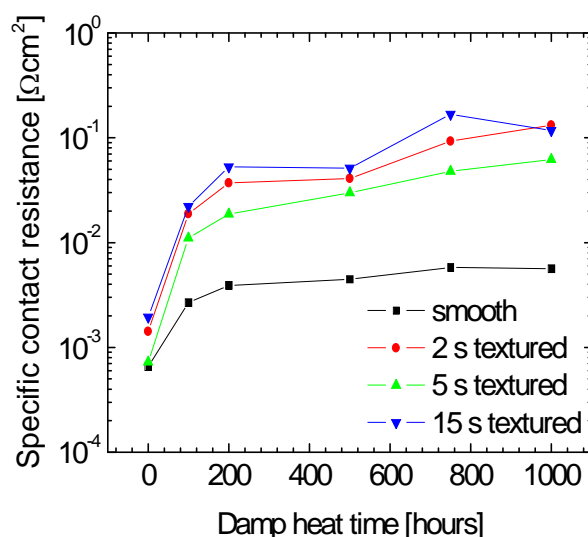
Fig. 6.5 The influence of the surface roughness of ZnO sputtered films on the specific contact resistance during aging experiments. Silver paste with 100 nm large silver particle was used for producing electrical contacts.

By increasing the roughness of the ZnO surface, the specific contact resistance increases. Samples that were textured for a longer duration in diluted hydrochloric acid exhibited higher values of specific contact resistance during the entire damp heat experiment. As the damp heat time increases, the difference in the specific contact resistances between textured and non-textured samples also increases. The most prominent increase of the specific contact resistance occurred in the first 200 hours of the accelerated aging experiment. The specific contact resistance increased merely 5 fold for non-textured ZnO films, whereas it increased 10-20 fold for textured

films. After 1000 damp heat hours, the specific contact resistances of textured samples are 10-20 folds higher than non-textured samples. The electrical contacts on textured ZnO surfaces exhibited a specific contact resistance of 70-100 $m\Omega cm^2$ at the conclusion of the damp heat experiment. The specific contact resistance of screen printed silver electrical contacts on textured ZnO samples exceeds the critical value of 10 $m\Omega cm^2$, and therefore the contact resistance may impart a severe negative influence on the conversion efficiency of a solar cell.

As it has been shown in Chapter 5, lower contact resistance on textured ZnO films may be achieved by reducing the silver particle size in the silver pastes. The silver pastes contained silver particles with an average diameter of 5 nm, 80 nm, 600 nm, and 1000 nm. The particles were uniformly dispersed in α-Terpineol with a volume ratio of 3:1 [6]. Prepared silver pastes were screen printed on smooth sputtered ZnO films. The samples with screen printed electrodes were exposed to a thermal treatment in an air flow oven for 30 minutes at a temperature of 160°C. While degradation has the most profound influence on the specific contact resistance in the first 200 damp heat hours, a closer examination of the contact behavior in this time interval is necessary.
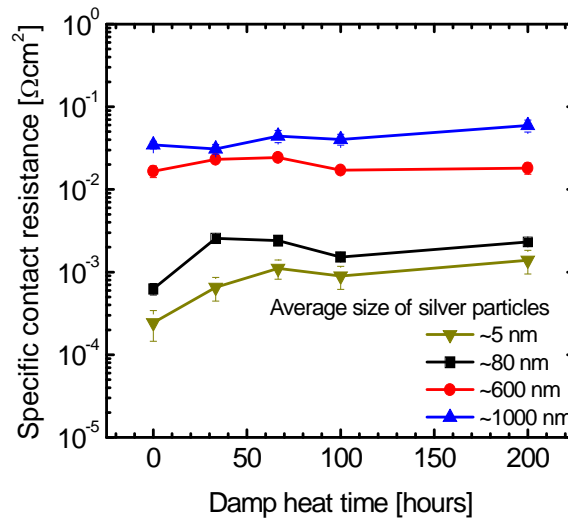

Fig. 6.6 The contact properties of silver electrical contacts on non-textured sputtered ZnO films. The size of the silver particles was varied from few nanometers to several microns.

Fig. 6.6 shows the influence of tailored silver particle size in pastes on the degradation of electrical contacts. Silver pastes with the largest silver particles TESM8020 and TES, with average silver grain sizes of s of 600 nm and 1000 nm, respectively, exhibited a specific contact resistance above 10 mΩcm^2 during 200 DH hours. By reducing the silver particle size, the specific contact resistance of the silver on ZnO contact is also reduced. Silver pastes with 5 nm and 80 nm large silver particles exhibited specific contact resistances of 0.2 mΩcm^2 and 0.7 mΩcm^2, respectively, prior to the damp heat stress. During the degradation experiment, the specific contact resistance of samples prepared with nanometer sized silver particle pastes remained below 2 mΩcm^2, and therefore, pastes with nanometer large silver particles, such as TEN and TENS5050, are promising materials for fabricating screen printed electrical contacts on CIS solar cells.

6.4 Degradation of electrical contacts on CIS solar cells

Previous results demonstrated that the specific contact resistance of screen printed electrical contacts may be controlled by the thermal process which is necessary for the contact formation on the front surface. The specific contact resistance of silver electrodes on sputtered ZnO films reduces as the annealing temperature increases. Furthermore, it was shown that contact properties are independent of the annealing duration. When exposed to accelerated aging, the annealing parameters demonstrated an influence on the sheet resistance of ZnO layers. Higher annealing temperatures and longer annealing durations resulted in faster degradation of the CIS solar cells' window layer. Next, the influence of the annealing process parameters on the degradation of electrical contacts on CIS solar cells will be examined.

PV410 silver paste with 100 nm silver particles was screen printed on the CIS solar cells. After the printing of electrical contacts, samples were annealed at the various temperatures in an air flow oven for 5 minutes. The influence of the annealing temperature on the behavior of the electrical contacts during the first 200 hours of the accelerated aging experiment is shown depicted in Fig. 6.7. Samples annealed at higher temperatures initially exhibited lower values of the specific contact resistance.

The contacts fabricated at 160°C exhibited approximately a 10 fold lower initial specific contact resistance than when annealed at 125°C. With damp heat time, the specific contact resistance of all samples increases. After 200 hours in the environmental chamber, electrical contacts that were prepared at higher temperatures performed with a lower specific contact resistance. However, the specific contact resistance of the contact annealed at the temperature of 160°C performed with the highest relative increase during the damp heat treatment. The specific contact resistance of screen printed contacts of 100 nm silver particles on CIS solar cells increased from 4 mΩcm^2 to 80 mΩcm^2 during the first 200 damp heat hours.

Fig. 6.7 Annealing temperature influence on the specific contact resistance of electrical contacts printed with silver paste containing silver particles of 100 nm. Printed contacts were thermally treated for 5 minutes.

The screen printed electrical contacts with PV410 silver paste, containing silver particles of 100 nm, and an annealing duration of 5 minutes perform demonstrated a specific contact resistance greater then 70 mΩcm^2 after 200 DH hours. The reason for the high specific contact resistance may be on account of a large amount of chemical binder residuals that remained in the printed films after merely a 5 minute annealing duration. Residual binder compounds in the printed films may be removed with a longer thermal treatment.

In order to confirm this hypothesis, the silver paste with 100 nm silver particles was again screen printed on a CIS solar cell. The annealing duration to form the electrical contacts was increased to 30 minutes, and the results of the degradation experiment are summarized in Fig. 6.8.
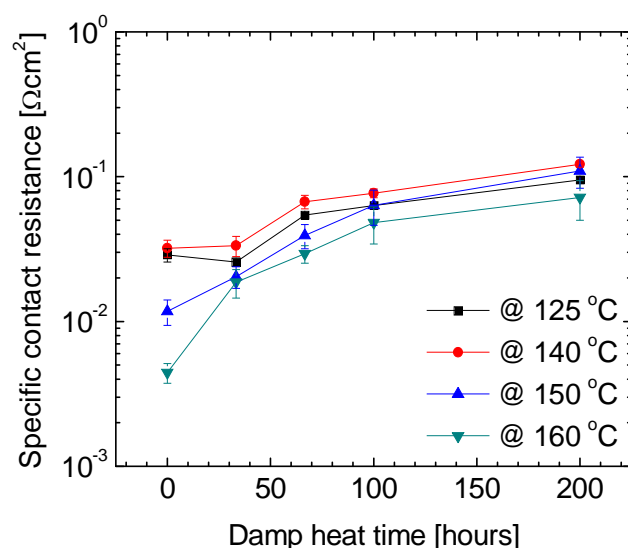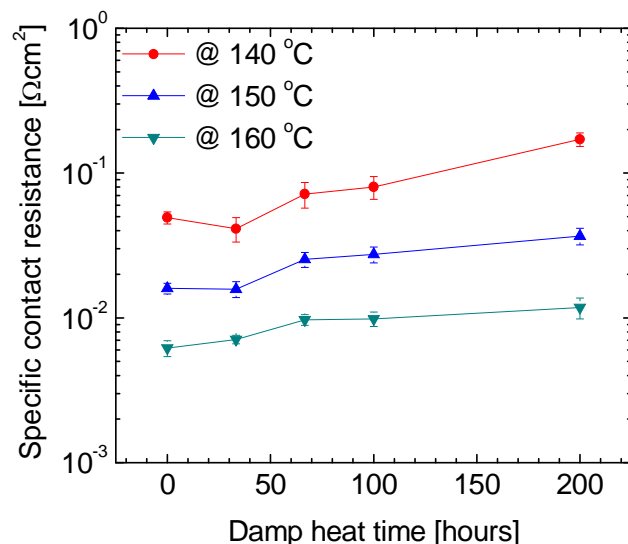

Fig. 6.8 Annealing temperature influence on the specific contact resistance of electrical contacts printed with silver paste containing silver particles of 100 nm. Printed contacts were thermally treated for 30 minutes.

Initial values of the specific contact resistance for samples that were exposed for 30 minutes in an air flow oven are in good agreement with results of samples that were annealed for 5 minutes. This confirms a previous statement that the annealing duration does not impart a significant influence the initial value of the specific contact resistance of printed contacts. During the accelerated aging test, screen printed contacts annealed for 30 minutes exhibited an increase in the specific contact resistance. The higher annealing temperature renders electrical contacts with a lower specific contact resistance. The sample annealed at 160°C for 30 minutes performed with a specific contact resistance of 12 mΩcm^2 after 200 damp heat hours.

The comparison between screen printed electrodes with 100 nm silver particles that were annealed at 160°C for various annealing durations is depicted in Fig. 6.9. The initial value of the specific contact resistance for both samples was 5-6 mΩcm^2 and after 200 damp heat hours, the sample treated for merely 5 minutes exhibited a specific contact resistance that is 8-9 times greater than one annealed for 30

minutes. The relative increase of the specific contact resistance in the case of electrodes annealed for a longer duration is lower than for the contacts treated for 5 minutes. Contacts annealed for a longer duration performed with a lower degradation rate due to reduced amount of organic residuals in the printed silver films.
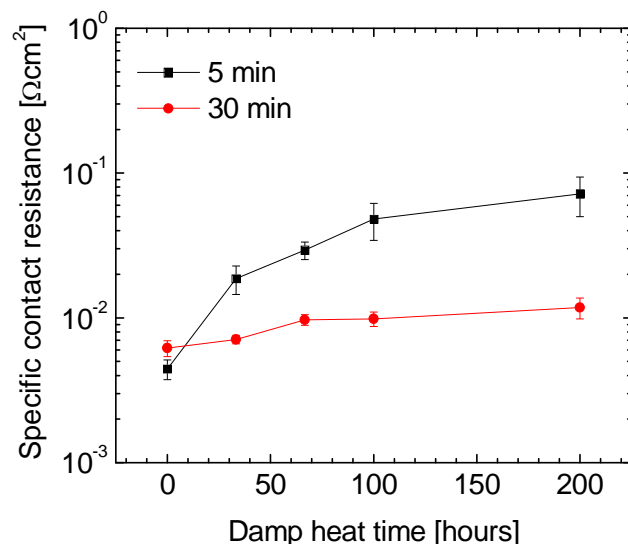

Fig. 6.9 Annealing duration influence on specific contact resistance. Screen printed silver electrodes with paste that contain 100 nm silver particles were annealed at 160°C.

As previously mentioned, further reduction of the specific contact resistance of silver printed electrodes on CIS solar cells may be possible by reducing the silver particles size in the pastes. Pastes with various sized silver particles were screen printed on a CIS solar cell and annealed for 30 minutes at 160°C. The influence of the various sizes of silver particles on the contact behavior during the damp heat test is demonstrated in Fig. 6.10. The initial value of the specific contact resistance reduces when the size of silver particles in the pastes is reduced. All analyzed samples perform with a low degradation rate during the damp heat test. After 200 damp heat hours, the smaller sized silver particle pastes exhibited a lower specific contact resistance of screen printed contacts on the CIS solar cells. The paste with the smallest size of silver particles, approximately 5 nm, reached a specific contact resistance of merely 3 mΩcm^2 after 200 damp heat hours.
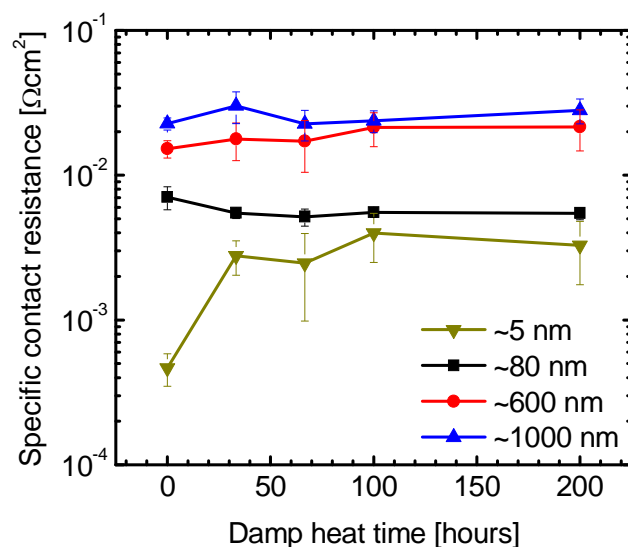
Fig. 6.10 Degradation of screen printed electrical contacts that were screen printed on CIS solar cells. Silver paste utilized contained silver particles of various sizes. Electrical contacts were annealed for 30 minutes at 160°C.

Chapter 5 demonstrated that silver nanoparticles render better surface coverage on rough and textured surfaces then silver pastes with larger particle sizes. As a consequence, a lower contact resistance occurs for electrical contacts with nanoparticle silver paste. Furthermore, better performance of electrical contacts printed with silver nanoparticle paste after the damp heat test may be attributed to a more densely printed contact film.
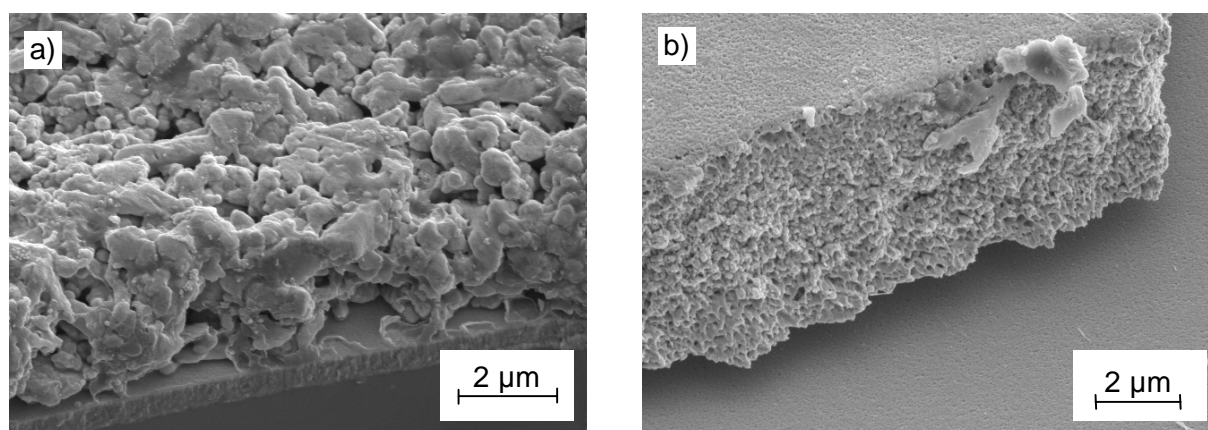
Fig. 6.11 SEM micrographs of screen printed electrical contacts on ZnO films with a) PV410 silver paste and b) nanoparticle silver paste.

Fig. 6.11 shows scanning electron microscope images of screen printed silver films on smooth ZnO layers with a) PV410 silver paste, and b) nanoparticle silver paste. As one can see, printed films with silver paste containing 5 nm nanoparticles exhibit a denser film then a film printed with a paste containing 100 nm silver particles. The less porous films will better protect contacts from moisture, water, and oxygen molecules that are responsible for more quickly degrading electrical contacts.

6.5 Degradation effects of solar cells parameters

CIS solar cells with screen printed silver front electrical contacts were exposed for accelerated aging. Current-voltage characteristics over an area of 1 cm^2 of solar cells were measured prior to placement in an environmental chamber and after 30, 60, 100, 200, 500, and 1000 damp heat hours. The parameters of the solar cells such as the short circuit current, the open circuit voltage, the fill factor, and the conversion efficiency, were extracted from the measured current-voltage curves. In addition, the series resistivity, R_{OC}, was calculated at the point of the slope of the current voltage where the total solar cell current is equal to zero. Furthermore, the shunt resistance, R_{SC}, defined as the resistance when the entire cell voltage equals 0 V, is measured. In a case of an ideal solar cell, the series resistance of a solar cell is zero, and the shunt resistance of a solar cell approaches infinity.

Front electrical contacts were formed on the front side of CIS solar cells. PV410 silver paste with 100 nm silver particles was screen printed, and the electrical contacts formed by thermal treatment at various temperatures in an air flow oven for 30 minutes. As previously shown, the annealing parameters influence the aging of the specific contact resistance of silver-ZnO contacts and the sheet resistance of the ZnO layer. Both of these parasitic resistances contribute to the series resistance of the cell. Fig. 6.12 depicts the influence of the damp heat test on series resistance. As the solar cells age, the series resistance increases.
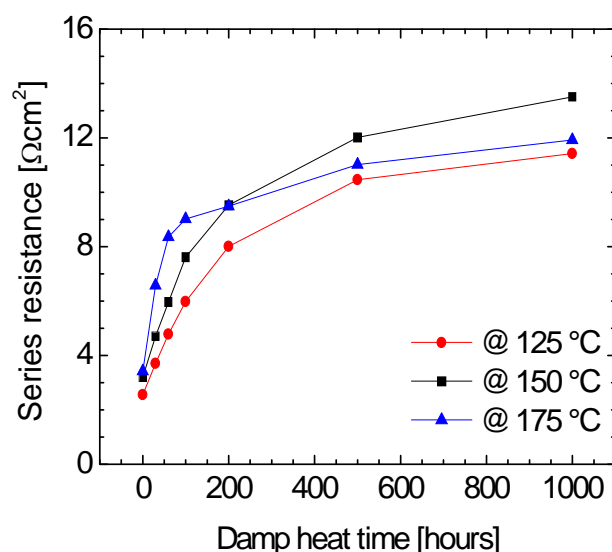
Fig. 6.12 Influence of degradation on the series resistance of silver electrical contacts on a CIS solar cell. Printed contacts were annealed for 30 minutes at various temperatures.

Solar cells with electrical contacts annealed at 125°C demonstrated the lowest series resistance during the damp heat experiment and increases from 2.5 Ωcm^2 to 10 Ωcm^2 after 1000 DH hours. Solar cells with contacts annealed at 175°C exhibited a more rapid increase in series resistance in the first 100 DH hours then cells annealed at lower temperatures. The more rapid initial degradation rate for cells annealed at 175°C can be attributed to the more rapid increase in the sheet resistance of the ZnO layer due to aging effects. Curiously enough, further exposure beyond 100 DH hours then reduced the degradation rate of the sample annealed at 175°C compared to other samples annealed at lower temperatures. After 1000 DH hours, the series resistance of the sample annealed at 175°C is comparable to a sample annealed at 125°C. A possible explanation for this behavior may be the more rapid increase of the specific contact resistance for samples annealed at lower temperatures.

The influence of aging on the shunt resistance parameter is summarized in Fig. 6.13. On account that the determined values for the series and shunt resistances during the damp heat experiment are far from the idealized solar cell, the values obtained for the shunt resistance should not be considered representative for all solar cells.
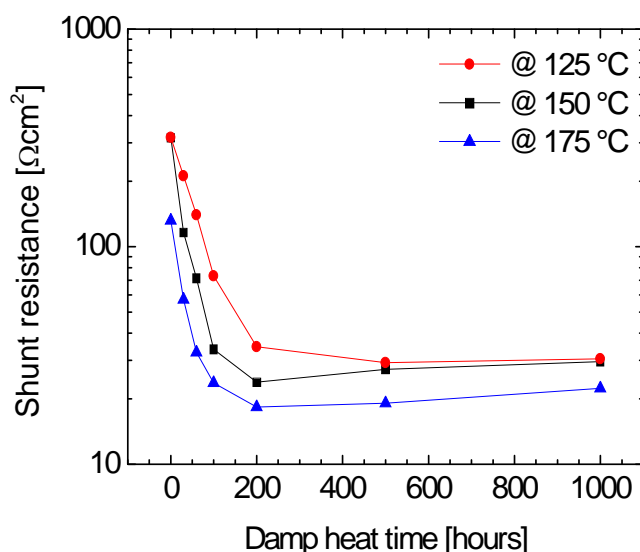
Fig. 6.13 Influence of degradation on the shunt resistance of silver electrical contacts on the CIS solar cell during the degradation experiment. Printed contacts were annealed for 30 minutes at various temperatures.

Due to degradation, the shunt resistance of CIS solar cells will decrease, though the process temperatures used for the formation of the electrical contacts on the front side of the CIS solar cells influence the aging of the shunt resistance. For low annealing temperatures, such as 125°C, used in the formation of electrical contacts, the shunt resistance reduces from 350 Ωcm^2 down to 30 Ωcm^2 after 1000 DH hours. Solar cells with contacts annealed at lower temperatures demonstrate a slower degradation rate of the shunt resistance with respect to DH time. The reason for very low shunt resistance values may be attributed imperfectly optimized process steps in the manufacturing CIS solar cells.

The fill factor of a solar cell is affected by the series and shunt resistance. Annealing temperature of front contact formation influences the fill factor of CIS solar cells, as depicted in Fig. 6.14. The fill factor's initial value will depend upon the annealing temperature of the electrical contacts. A lower process temperature will render a cell with a higher fill factor, and this behavior resembles the behavior of the shunt resistance. Furthermore, one may say that the fill factor is largely determined by the shunt resistance. This relationship is also realized via results obtained during aging. The fill factor drops with damp heat time and the degradation rate of the fill factor is at its most minimum when contacts are prepared at the lowest temperature. This

same behavior is apparent in the degradation of the shunt resistance in solar cells. Therefore, the aging of the fill factor in CIS solar cells was completely dominated by the degradation of the shunt resistance in the cells. In the case of the solar cell with silver electrical contacts annealed at 125 °C, the fill factor exhibit an initial value of 60%, and later during the damp heat experiment reduced to 32%. After 1000 DH hours, the fill factor of CIS solar cells all plummeted to 25-30 %.
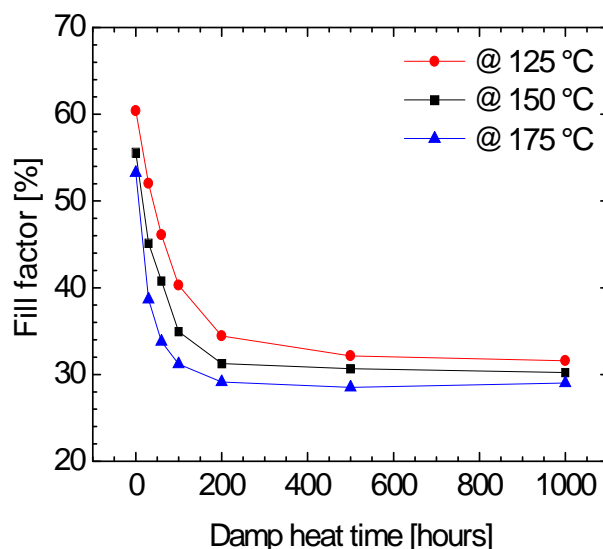
Fig. 6.14 Influence of annealing temperature during contact formation on the degradation of the solar cell fill factor.

As previously stated in Chapter 3, the short circuit current of a solar cell may be affected by the series resistance of a cell, though unchanged by small values of the series resistance. After the series resistance exceeds a critical value, the short circuit current of a solar cell reduces in value. The change in degradation of the short circuit current in CIS solar cells with screen printed electrical contacts is depicted in Fig. 6.15. With the damp heat time, the short circuit current reduces in value, and may be related to the increase of series resistance. In analyzed cells, solar cells with electrical contacts fabricated at lower temperatures exhibited higher values of short circuit current. The solar cells performed with an initial short circuit current of 34 mA/cm^2 after formation of the electrical contacts, and in the first 100 DH hours, the series resistance remains under 7 Ωcm^2 while the short circuit current remains unchanged. As solar cells with electrical contacts prepared at the higher temperatures of 150°C and 175°C exceed the critical 7 Ωcm^2 value of the series

resistance during the accelerated aging test, the short circuit current of these cells declined.
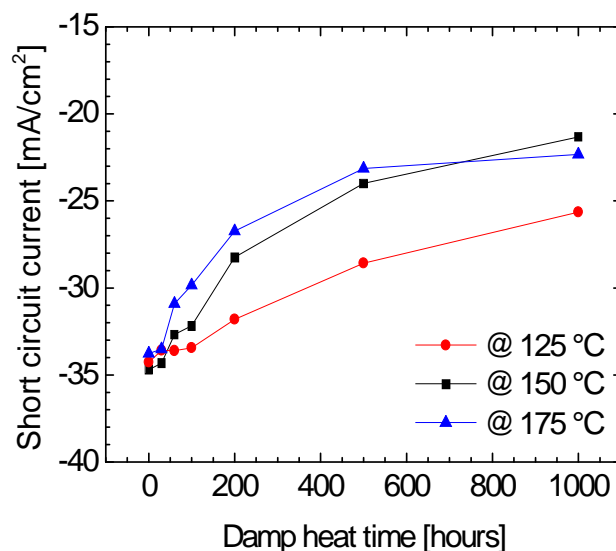

Fig. 6.15 Influence of degradation on the short circuit current of CIS solar cells with printed front electrical contacts. Contacts were formed after thermal treatment for 30 minutes at various temperatures.

As previously discussed in Chapter 3, the open circuit voltage of a solar cell can be affected by its shunt resistance. Ideally, the shunt resistance has an infinite value, yet as the shunt resistance reduces, the open circuit voltage of a solar cell also reduces. Fig. 6.16 demonstrates the affect of aging on the open circuit voltage of CIS solar cells with screen printed silver electrodes. Here one may observe how with damp heat time, the open circuit voltage is reduced. For the solar cell treated at 125°C, the open circuit voltage reduces from 430 mV to 370 mV in the first 200 DH hours, yet as damp heat time increases beyond 200 DH hours, the open circuit voltage remains unchanged. Furthermore, solar cells thermally treated at higher temperatures exhibited more distinct drop in open circuit voltage in the first 200 DH hours. Solar cells with silver printed contacts treated at 175 °C exhibit an open circuit voltage of 320 mV after 1000 DH hours. Despite the temperature difference during thermal treatment of the printed electrical contacts, all tested solar cells exhibited similar values of shunt resistance, between 20-30 Ωcm^2, after 1000 damp heat hours. As the difference between the values of the open circuit voltage for samples prepared at various temperatures is much larger than it would be if the shunt resistance was the

only factor influencing the change in open circuit voltage, the influence of the annealing temperature utilized during fabrication of the electrical contacts must also be affecting the properties of the $CuInS_2$ solar cells, which was already known in the literature [7]. As the annealing temperature during formation of the front electrical contacts increases, so does the degradation rate of the open circuit voltage during the DHT.

Fig. 6.16 Influence of degradation on the open circuit voltage of a CIS solar cell with printed front electrical contacts. Contacts were formed after thermal treatment for 30 minutes at various temperatures.

The performance of a solar cell is usually observed through the conversion efficiency. Degradation of the conversion efficiency of analyzed CIS solar cells is depicted in Fig. 6.17, and resembles the same decline occurred in the short circuit current, the open circuit voltage, and the fill factor as a result of damp heat time. Solar cells with front electrical contacts fabricated at the lower annealing temperature of 125°C performed with a higher efficiency after 1000 DH hours, and exhibited a drop in conversion efficiency from 8.6 % to 3.0 %.
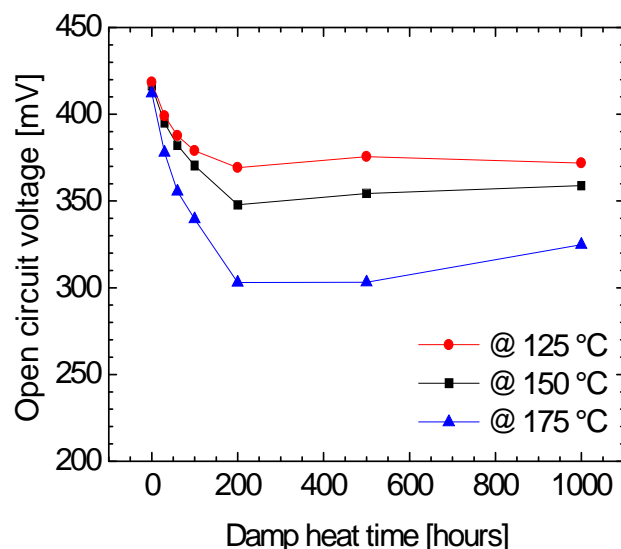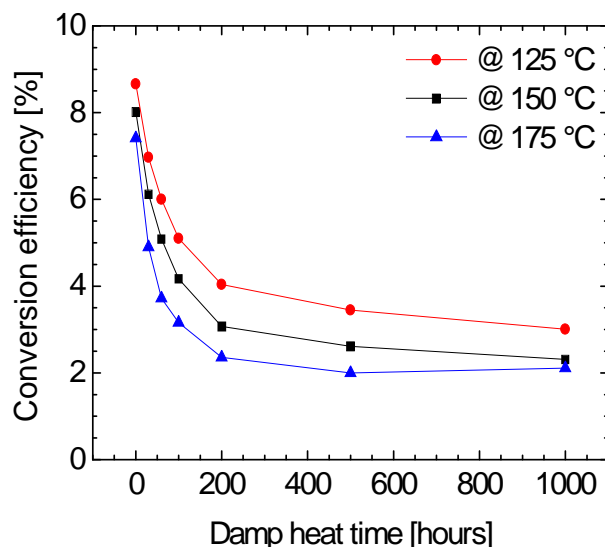
Fig. 6.17 Influence of degradation on the conversion efficiency of CIS solar cells with printed front electrical contacts. Contacts were formed after thermal treatment for 30 minutes at various temperatures.

6.6 Summary

In this chapter, it was shown that the degradation process affects not only the electrical properties of the silver-TCO contacts, but also the properties of TCO layers. The change of the sheet resistance between textured ZnO films and the CIS solar cells occurs in a similar fashion, therefore, the textured ZnO film model may be adopted to further investigate electrical contacts on CIS solar cells. It has been shown that the annealing process parameters, such as the annealing temperature and the annealing time, influence the change of the sheet resistance of CIS solar cells. Higher annealing temperatures and longer annealing times incur large sheet resistance values, thereby increasing the series resistance in solar cells. This increase in the series resistance then reduces the conversion efficiency of a solar cell.

As previously mentioned in chapter 5, by reducing of size of the silver particles in the printing pastes, one may reduce the ohmic losses in the silver-ZnO electrical contacts. After accelerated aging tests, contacts with screen printed silver

nanoparticles with an average size of 5 nm exhibited a specific contact resistance of 0.7 mΩcm^2 when printed on sputtered ZnO films, and 3 mΩcm^2 when printed on CIS solar cells. Additionally, longer annealing durations and higher annealing temperatures are necessary in order to remove residual organic binder from the printed silver films which most likely results in more rapid electrical contact degradation.

The degradation of the electrical contacts and the sheet resistance of the ZnO layer were utilized to study the degradation of CIS solar cell parameters. The annealing process used in the fabrication of front electrical contacts influences the performance of CIS solar cells and their parameters, and it was found that higher annealing temperatures result in more rapid degradation of all solar cell parameters. Lastly, analyzed CIS solar cells demonstrated very low shunt resistance values, which masks the influence of the contact properties on the performance of the solar cells.

6.7 References

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Chapter 7

Introduction to thin film transistors

The silicon industry dominated different spheres of electronic industries in the last 60 years. In the last decades the thin film transistor (TFT) industry evolved from the standard silicon industry and became the dominant factor on the display market. Most of the TFTs in the display industry are based on amorphous silicon (a-Si) and a smaller fraction is based on polycrystalline silicone (poly-Si). Beside the display market, thin film transistors are also used in digital X-ray imagers, in radio frequency identification (RFID) tags, in sensing devices, in various medical applications and in low cost disposable electronics. Nowadays, researchers are looking for new materials and new fabrication techniques that can improve performance of TFTs. Upcoming generations of TFTs will perform with new functionalities that will result with new applications: such as organic light emitting diodes (OLED) displays, flexible, printable and low-cost electronics.

7.1 Basic principle of operation of thin film transistor

The field effect transistor (FET) is the most important device for very large scale integrated circuits. The field effect transistor is a three terminal device. A semiconductive material is deposited between source and drain electrodes. The conductivity of active material of a transistor can be modulated from a conducting state (On state) to a non-conducting state (Off state) by the gate terminal potential. The schematic cross section of a FET and its equivalent electrical model is shown in Fig. 7.1. A gate electrode is deposited on an inert substrate, usually on glass or

polymer foil or steel foil. In the laboratory applications, silicon/silicon-dioxide substrates are very often used as a gate electrode and gate insulator for fabrication of thin film transistors. Over the gate electrode, an insulator layer is deposited. The active semiconducting material is then applied on the top of the insulator layer. The active material can be either organic or inorganic semiconducting material. Finally, two conductive contacts are deposited on the top. The distance between the contacts is called the channel length, L, and the width of the source/drain contacts defines the width of the channel, W.
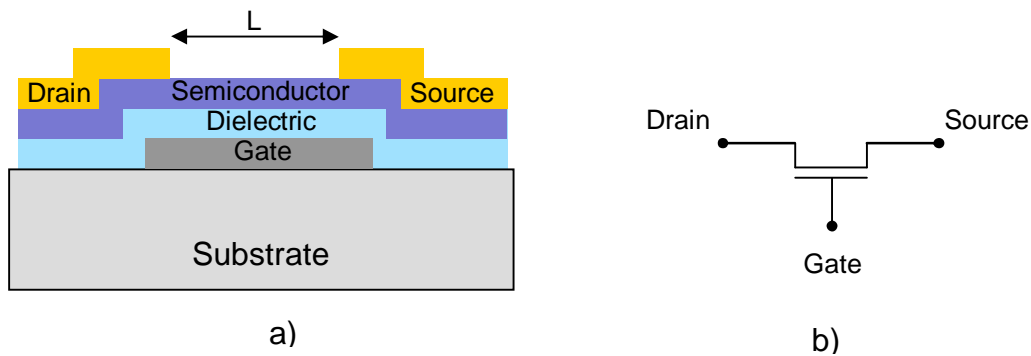

a)   b)

Fig. 7.1 a) The cross section of a thin film transistor. b) The equivalent electrical scheme of a thin film transistor.

The thin film transistor, as a field effect transistor, is commonly used for studying the transport properties of materials used as the active channel. By applying a voltage over the gate electrode, the charge carrier density in the channel is modulated. In the case of a transistor with a p type semiconductor as the active layer, when a negative voltage is applied on the gate electrode positive charges are induced in the channel. Due to the high concentration of the accumulated charges, a conductive channel is formed between source and drain electrode, and the transistor is operating in the on mode. Increasing the voltage on the gate electrode towards positive values, the charge carrier density in the channel is reduced, until there are no more free charges and the transistor is switched off. A further increase of the gate voltage would result in the accumulation of negative charges in the channel. The boundary between the 'on' and 'off' state of a transistor is called the threshold voltage of the semiconductor, V_T.

For a n type semiconductor, the conductive channel is formed by applying positive gate voltage, V_{GS}. The current through the device is controlled by applied voltage

over the source/drain electrodes. When the source electrode is grounded, and positive V_{DS} voltage applied to the drain electrode, the current I_{DS} will flow through the channel of the transistor. The thin film transistor can operate in two different modes regarding the ratio between applied drain-to-source, V_{DS}, and gate-to-source, V_{GS}, voltages. If the applied positive drain voltage, V_{DS}, is smaller than the applied gate voltage subtracted with the threshold voltage, V_{GS}-V_T, the transistor operates in the linear regime (also known as the ohmic mode). In this regime the charges are uniformly distributed along the conducting channel. The current going through the transistor when it operates in linear mode is given by [1]:

$$I_{DS} = \frac{W}{L} C_i \mu \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS} \qquad \text{(Eq. 7.1)}$$

where μ is the charge carrier mobility, and C_i is the capacitance per surface area of the insulator layer. For a small drain voltage, the current of the device depends linearly on the applied V_{DS} voltage. Increasing the drain voltage to the point when it becomes equal to the effective gate voltage, V_{GS}-V_T, will result in no free charges in the region between the drain and the gate electrodes. This is also known as the pinch-off effect. A further increase of drain-to-source voltages, will not affect the channel current that saturates to:

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2. \qquad \text{(Eq. 7.2)}$$

This regime of transistor operation is called saturation regime.

The performance of the transistor is observed through several parameters: a charge carrier mobility, a threshold voltage, a subthreshold slope and an on/off ratio.

The charge carrier mobility describes how fast the charge drifts due to the applied electric field. The charge carrier mobility can be extracted from the transfer characteristic (I_{DS} vs. V_{GS}) of a transistor in the linear and the saturation regime. The charge carrier mobility in the linear regime can be calculated as:

$$\mu_{lin} = \frac{L}{WC_iV_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} . \tag{Eq. 7.3}$$

Similarly, the charge carrier mobility in the saturation regime can be determined by:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 . \tag{Eq. 7.4}$$

The threshold voltage, V_T, can be determined from the transfer characteristics in the linear and the saturation regime as well. It is defined as an intercept of the V_{GS} axis with the tangent to the transfer curve in the point where the curve is steepest, Fig. 7.2. Ideally, the threshold voltage equals to 0 V, but due to the presence of dopants it can vary. Similarly, the threshold voltage in the saturation regime can be extracted by the linear fit of the square root of the drain current. The intersection with the voltage axis gives the threshold voltage.
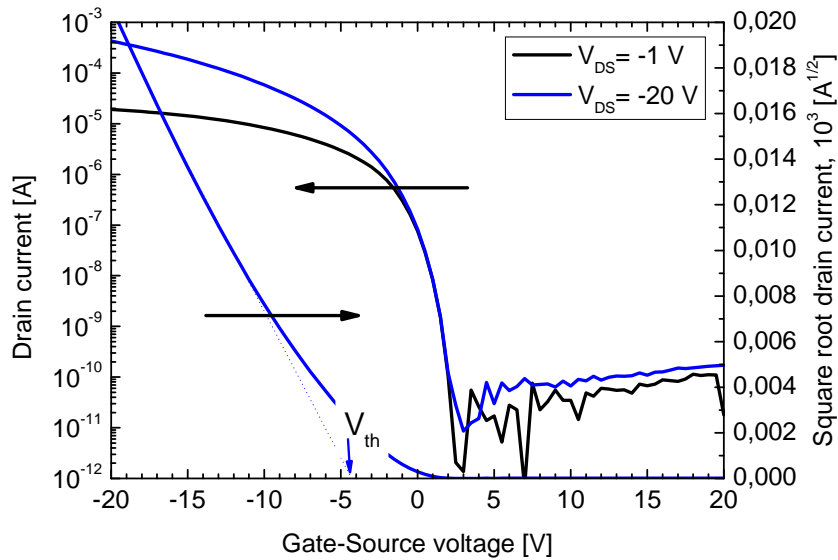

Fig. 7.2 Transfer curves of a pentacene thin film transistor.

For a gate voltage higher than the threshold voltage where a transistor is still not turned on, a transistor operates in the subthreshold regime. The drain current in this region is increased exponentially with the gate voltage. The slope of the logarithmic

transfer curve at the steepest point determines the subthreshold slope. The subthreshold slope of a TFT indicates how fast a transistor turns on, and is defined as:

$$S = \frac{\partial V_{GS}}{\partial (\log I_{DS})}.$$ (Eq. 7.5)

The subthreshold slope is expressed in V/dec units. For practical applications it is necessary that transistors turned on quickly, which will correspond with small values of subthreshold slopes.

Finally, a thin film transistor is characterized with the current on/off ratio. The on/off ratio of the drain current is defined as the ratio of the drain current when the transistor is on, to the drain current of the off state of the transistor. For most of the applications (like for memories and display applications) the current on/off ratio has to be as high as possible (usually greater than 10^6). The conductivity of the semiconductor material and the film thickness has an influence on the on/off ratio.

7.2 Parasitic effects in thin film transistors

In the ideal case transistor behavior is described with the equations 7.1 and 7.2. In reality parasitic effects can have a strong influence on the transistor characteristics. Parasitic capacitances and resistances can affect the performance of transistors by reducing the switching frequency of the devices and reducing the effective charge carrier mobility of devices.

The parasitic capacitances in a thin film transistor occur between the transistor terminals: the capacitance between the source and the gate, C_{GS}, the capacitance between the drain and the gate, C_{GD}, the channel capacitance, C_{CH}, and the capacitance between the source and the drain electrodes, C_{DS}. The capacitances between the source/drain and the gate electrodes are influenced by the physical overlap between these electrodes. The negative effect of these parasitic capacitances can be observed through the reduced transfer frequency of a transistor [2].
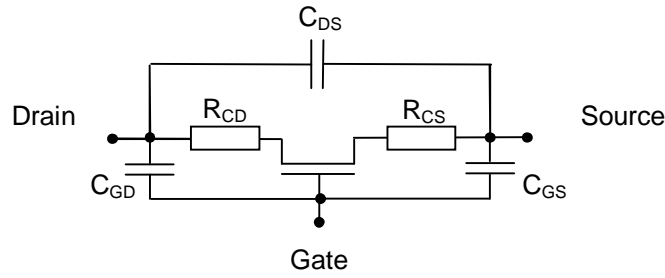
Fig. 7.3 The equivalent electrical scheme of a thin film transistor with parasitic capacitances and resistances.

Furthermore, the transistor performance can also be affected by parasitic ohmic losses that occur on the junction between the source/drain electrodes and the semiconducting material. The equivalent electrical scheme for a transistor with parasitic contact resistances is shown in Fig. 7.3. The contact resistance between the source electrode and the semiconducting material is modeled with R_{CS}, and consecutively the contact resistance between the drain electrode and the semiconducting material is represented with R_{CD}.

In order to include the parasitic contact resistances in the model of a thin film transistor, the drain current of a transistor that operates in the linear regime given with the equation 7.1 has to be modified. The effective gate to source voltage is modified by subtracting the voltage drop over the source contact resistance from the applied gate voltage, V_{GS}-$R_{CS}I_{DS}$. Similarly, the effective drain to source voltage is given as V_{DS}-(R_{CS}+ R_{CD})·I_{DS}. The expression for the drain current in the linear regime then becomes:

$$I_{DS} = \frac{W}{L} C_i \mu \left(\left(V_{GS} - R_{CS} I_{DS} \right) - V_T - \frac{V_{DS} - \left(R_{CS} + R_{CD} \right) I_{DS}}{2} \right) \cdot \left(V_{DS} - \left(R_{CS} + R_{CD} \right) I_{DS} \right).$$

(Eq. 7.6)

The previous equation for the drain current may be solved by considering an approximation that the source and the drain contact resistances are equal, (R_{CS} = R_{CD}). Now, Eq. 7.6 becomes:

$$I_{DS} = \frac{L}{L + W \mu C_i R_C \left(V_{GS} - V_T - V_{DS}/2 \right)} \frac{W}{L} C_i \mu \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) \cdot V_{DS}, \qquad \text{(Eq. 7.7)}$$

where the total contact resistance is given as $R_C=R_{CS}+R_{CD}$. The equation 7.7 may be rewritten in similar form as the equation 7.1:

$$I_{DS} = \frac{W}{L}C_i\mu_{eff}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)\cdot V_{DS},$$
(Eq. 7.8)

where the effective charge carrier mobility, μ_{eff}, is defined as:

$$\mu_{eff} = \mu\frac{L}{L+W\mu C_i R_C\left(V_{GS}-V_T-V_{DS}/2\right)}.$$
(Eq. 7.9)

The channel resistance of a thin film transistor is defined as:

$$R_{CH} = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{L}{WC_i\mu\left(V_{GS}-V_T-V_{DS}\right)}.$$
(Eq. 7.10)

and the previous expression for the effective charge carrier mobility can be rewritten as:

$$\mu_{eff} = \mu\frac{1}{1+R_C/R_{CH}}.$$
(Eq. 7.11)

For the short channel devices, the channel resistance becomes lower, while the contact resistance remains unchanged. When the contact resistance becomes larger than the channel resistance ($R_C>R_{CH}$), the reduction of the effective charge carrier mobility occurs. The influence of the contact resistance on the effective charge carrier mobility becomes more prominent for the short channel transistors. The influence of the contact resistance on the transistor performance through the transfer characteristic is shown in Fig. 7.4. As one can see, the extraction of the values for the charge carrier mobility and the threshold voltage from the transfer characteristic of a transistor with prominent contact effects can be influenced by the parasitic contact resistances at the source/drain electrodes.
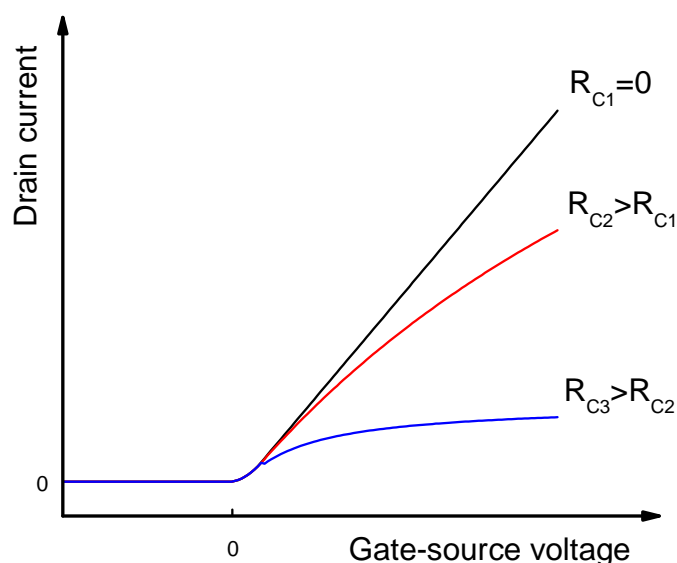
Fig. 7.4 The influence of the contact resistance on the thin film transistor performance in the linear regime of operation.

7.3 Thin film transistors materials

The state of the art of thin film transistors is based on amorphous silicon [3]. With the charge carrier mobility in the range of 0.5-1 cm^2/Vs, the on-off current ration exceeding 10^6, a-Si fulfils all requirements for the LCD manufacturers. The main problem of a-Si TFTs is the electrical instability of the transistor. Due to the continuously applied gate voltage, the threshold voltage of a thin film transistor shifts. The polycrystalline phase of silicone was studied as a material to substitute amorphous silicone [4]. Low temperature poly-Si TFTs can exceed the charge carrier mobility above 100 cm^2/Vs, and both n and p type transistor channels can be fabricated. The main disadvantages of poly-Si technology are high manufacturing costs and non-uniformity of processed transistors. Currently poly-Si TFTs are successfully used for large current driving in OLED displays and for small integrated displays.

With new applications of TFTs (flexible electronics, OLED displays, RFID tags, medical patches), new materials are investigated: organic semiconductors, metal oxides and nanomaterials.

Metal oxide semiconductors became of interest in the last decade, due to the charge carrier mobility (exceeding 100 cm^2/Vs) of these devices that are suitable for the display industry. Sputtered metal oxides (i.e. ZnO, InSnO, InGaO, ZnSnO, InZnO, GaInZnO) are commonly used, but many other materials have been studied [5].

Recently, nanowires have been investigated as potential material for making TFTs, and also devices with single nanowires have been investigated [6]. Silicon nanowires, carbon nanotubes and various oxide nanowires are promising candidates for a further shrinking of the device size.

Organic materials offer the possibility to process devices at low temperatures that are compatible with plastic flexible substrates [7]. Furthermore, manufacturing steps for fabrication organic thin film transistors are simple and inexpensive, which makes organic thin film transistors (OTFTs) an interesting candidate for the TFT industry. Many organic materials can be deposited from the solutions, which make manufacturing process compatible with printing systems. The charge carrier mobility of organic thin film transistors is below the range of a-Si devices (up to 1 cm^2/Vs). Currently most investigated organic semiconductors are small molecules (i.e. pentacene), and organic polymers (i.e. polythiophene family). Organic thin film transistors and their properties are studied in the next two chapters of the thesis.

7.4 Different configurations of thin film transistors

The thin film transistors can be designed in one of the configurations illustrated in Fig. 7.5. The convention is to classify the TFT structures according to the stacking order of the gate electrode, the channel layer and the source/drain contact electrodes. Therefore, top/bottom gate and top/bottom contact configurations are established [8]-[11].

The bottom gate structures are common in laboratory research because of commercially available Si/SiO2 wafers that can be used as the gate electrode and gate insulator respectively. The fabrication of a thin film transistor on such substrates

requires only one mask step for structuring source/drain electrical contacts. One of the possible upgrades of these structures is to use one more photolithography step in order to structure the channel region (the mesa structure) and to suppress the gate leakage current which often leads to overestimated extracted parameters of a thin film transistor (i.e. the charge carrier mobility, the subthreshold slope).
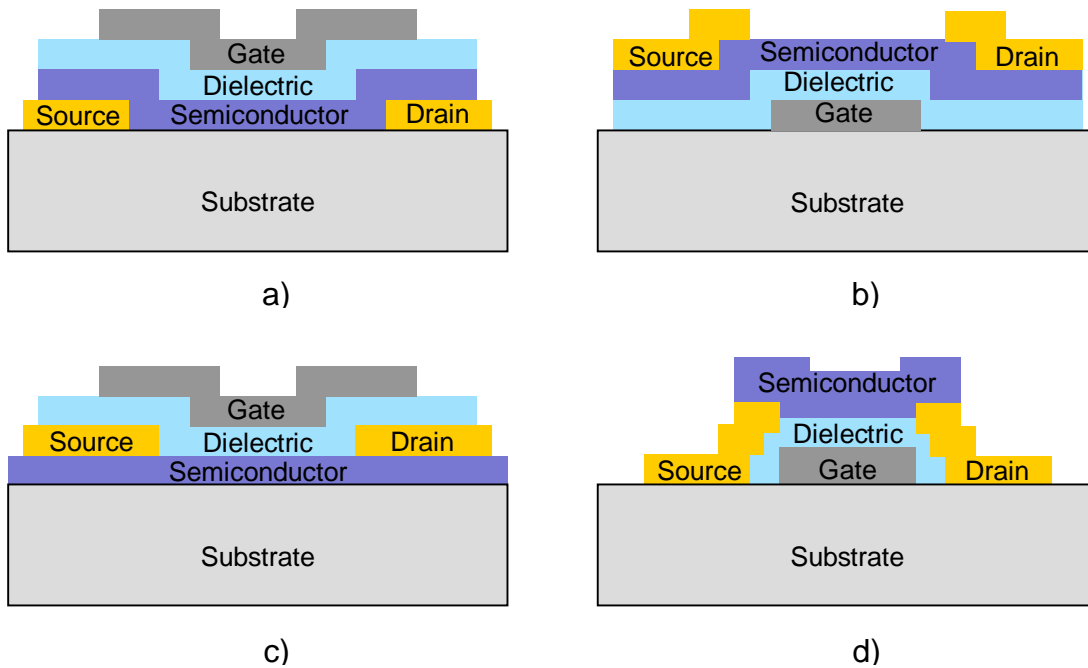

Fig. 7.5 The cross section illustration of a transistor in a) the top gate bottom contact, b) the bottom gate top contact, c) the top gate top contact and d) bottom gate bottom contact configuration.

The bottom gate structures shown in Fig. 7.5b and Fig. 7.5d have their own disadvantages. First, the semiconductor layer is exposed to the atmosphere, and therefore the TFT characteristics can be affected by oxygen, humidity and the presence of other gasses. Atmosphere gasses can be absorbed, desorbed or can simply diffuse in the semiconductor layer causing instability of devices. Another disadvantage of such geometries is coming from the gate to source/drain overlaps. Namely, the large overlaps between source/drain electrode and the gate electrode results in a large parasitic capacitance. The parasitic capacitance slows the response of devices and reduces their switching frequency [12]. Bottom gate configurations can be made with either top or bottom source/drain electrical contacts. The

advantage of the top contact configuration, shown in Fig. 7.5b, is that it can minimize the area of the semiconductor layer that is exposed to the atmosphere. The top contact configuration has the advantage of easily making accurate source/drain electrodes through shadow masks, which might not be the case for devices with bottom contacts. Hence, the devices made in bottom gate top contact configuration (staggered configuration) perform with a lower contact resistance than thin film transistors in bottom gate bottom contact configuration (coplanar structured devices). When the epitaxial semiconductor layer is used to form the channel of thin film transistors and when it is difficult to form good electrical contacts, the top gate top contact configuration is used, Fig. 7.5c [13]. The process requires at least two patterning masks. The advantage of a such structure is that the upper gate electrode and the gate insulator layer are also serving as a passivation layer, protecting the semiconductor layer from degradation due to atmospheric exposure. The top gate thin film transistor configuration can also be made with bottom source/drain electrical contacts, Fig. 7.5a. The top gate staggered configuration exhibits lower contact resistance than the top gate coplanar TFT structure.

In the top/bottom staggered thin film transistor configuration, the conducting channel in the active material is formed close to the interface with the insulator layer. The transfer of charges in and from the conducting channel of transistors uses the whole contact area, having electrical charges flow vertically in/from the surface of the electrical contacts towards the gate electrode.

On the other hand, the process of charge carrier injection in/extraction from the channel differs in the case of top/bottom gate coplanar configurations (where the gate and source/drain electrodes are deposited on the same side of the active layer). A transistor with coplanar configuration has a conducting channel located in the area between the source/drain electrodes. In that case, the current flows from the side of the electrical contacts directly to the semiconductor layer.

At the end, it is relevant to mention that bottom contact devices with evaporated organic semiconductors exhibit lower charge carrier mobility compared to the top contact ones. The reason for such behavior lies in a formation of trap infested regions around the contacts [14]. Nevertheless, bottom contact configurations are the best choice for downscaling device dimensions, because no shadow mask is used to form metal contacts.

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Chapter 8

Channel potential distribution in poly-3-hexylthiophene based thin film transistors

The new era of electronic devices came with a studious research of organic semiconductors. New functionalities of devices become possible with organic materials. Nowadays devices can be manufactured on flexible substrates, fabrication is possible on large areas with low cost techniques, consuming small amount of materials, which allows these devices to weigh comparatively little. The most promising organic devices between other candidates are organic thin film transistors and organic photovoltaic devices. An organic thin film transistor (OTFT) is a vital component of every electronic device, including displays and radio frequency identification (RFID) tags. Organic materials can be deposited on a substrate from a solution (organic polymers) or devices can be made by vapor deposition of small organic molecules. Thin film transistors based on vapor deposition of small molecules, perform with better properties in comparison with solution based processed transistors. However, very low fabrication costs of transistors with conjugated polymers are making these devices interesting and thus conjugated polymers are widely researched.

8.1 Charge transport in organic thin film transistors

Conjugated polymers are very promising materials as the active layer in thin film transistors (TFTs) for application in the low-end data storage, such as chip cards and identification tags. Such devices are produced with low production costs and a relatively easy processing of materials. Due to excellent mechanical properties, such as strength and flexibility, they can be fabricated on flexible substrates. The performance of organic electronic devices has already been demonstrated in ring oscillators [1], integrated circuits with programmable code generator [2], active matrix light emitting diode (LED), displays [3]-[4].

Conjugated polymers are soluble in a wide variety of solvents, and thin films are easily fabricated by very low cost techniques such as spin coating or dipping. These films exhibit amorphous structure and can be regarded as highly disorder systems. The transfer of charges occurs to happen by hopping process from one polymer chain to another polymer chain. The disordered structure in the polymer films limits the transport process, and thus processed devices perform with low charge carrier mobility for device applications. [5]-[7].

Thin film transistors based on polythiophene polymers have been studied in the last two decades. In contrast to inorganic semiconductors where atoms are bonded by strong covalent bonds, in organic semiconductors the molecules are weakly held by Van der Walls interactions. While in inorganic semiconductors the charge transport is happening in well defined electronic bands, charge carriers in organic semiconductors cannot move easily through the material. Large intermolecular distances between organic molecules make the charge transport difficult, which leads to lower charge carrier mobility as in inorganic semiconductors.

The charge transfer in organic semiconductors is related to carbon atoms, to the sp_2 hybridizations and p_z orbitals. The sp_2 orbitals are lying on the same plane, while p_z orbitals are perpendicular to it, Fig. 8.1. Two neighboring carbon atoms can have an overlap between their sp_2 orbitals. These bonds (named σ-bonds) are strong and lower in energy than original orbitals. Also at higher energy, an anti-bonding $σ^*$ orbital is formed that is left unoccupied. On the other hand, vertical p_z orbitals from neighboring carbon atoms are forming π-bonds that are relatively weak bonds. The

pair of electrons can be found in the bonding orbitals, or in different directions (spin up and down) in the case of anti-bonding orbitals (π^*). The highest occupied molecular orbital is called the HOMO, and the lowest unoccupied molecular orbital the LUMO. The distance between energetic levels HOMO and LUMO is defining the energy bandgap of an organic semiconductor material. The molecular chain of n carbon atoms with n participating atomic p_z orbitals obtain n/2 bonding π and n/2 anti-bonding π^* molecular orbitals. If n goes to infinity, the π and π^* energy levels will form a continuous band, where π and π^* band will represent the occupied "valence" and the unoccupied "conduction" band.
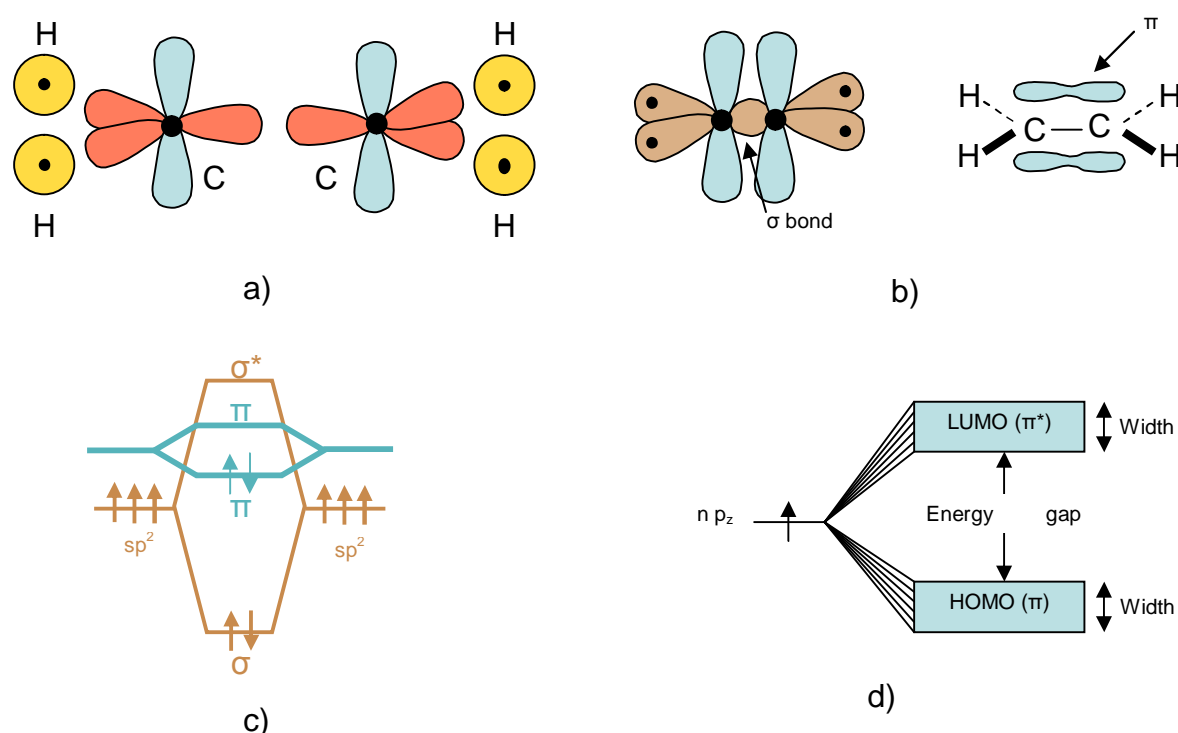

Fig. 8.1 Illustration of the sp_2 hybridization of C_2H_4 molecule a) before bonding, b) after bonding. c) An illustration of σ and π bonds in C_2H_4 molecule. d) Formation of the HOMO and LUMO energetic levels.

Similar to the single molecules, the conjugated polymers and their molecular orbitals will interact and overlap, too. The conjugated polymer has a rigid rod backbone which is made soluble by attaching flexible $(CH_2)_n$ alkyl side chains. When deposited from a solution, these polymers are forming polycrystalline films. The best known family is poly-3-hexyl thiophene (P3HT). With improved ordering of the film (regioregular form) the charge carrier mobility of thin film transistors is improved. Process parameters

(temperature, type of solvent…) can be used to improve crystallinity in the polymer films. [8]

The modeling of organic field effect transistors has been the focus of studies by many research groups, and due to several repelling factors there still is no consensus on a final model. First, the charge transport in organic semiconductors is still not completely understood. The general agreement is considering the transport of charges via a hopping process between localized states, although the exact behavior of these hops still is the topic of many scientific discussions. Second, organic field effect transistors made from different compounds exhibit different behavior. As an example, the polymer based devices perform differently from the ones fabricated with small molecules. Thus, many research groups assume that the charge transport in pentacene molecules is a band like transport with trap states. In such a case, the charge carrier mobility of devices is not gate voltage dependant, as in the case of polymer field effect transistors that assume hopping transport [9]. Finally, the fabrication process of devices appears to have a strong effect on its final performance.

In the last two decades, several theories have been proposed that explain experimental data of the charge transport in organic semiconductors (e.g. the delocalized band transport model, the multiple trapping and release model [10], the polaron hopping model [11], the tunneling model, Poole-Frenkel model [12]-[15]. The most accepted theory of charge transport is based on a percolation model of hopping between localized states, given by Vissenberg-Matters model [16]. This model is used successfully to fit the experimental temperature dependence of the field effect mobility of pentacene and polythienylene organic field effect transistors. Charge transport is described by a variable range hopping mechanism through an exponential density of states (DOS). The density of states of organic semiconductors is given by:

$$g(E) = \frac{N_t}{k_B T_0} \exp\left(\frac{E}{k_B T_0}\right)$$
(Eq. 8.1)

with energies $-\infty < E \leq 0$, and where N_t is the number of states per unit volume and k_B is the Boltzmann's constant. T_0 indicates the width of the density of states and also

is a measure of system disorder. The density of states increases with energy, E. The Vissenberg-Matters model assumes that an activated jump is more probable as more energy states are available for higher energies. Unlike the inorganic crystalline semiconductors, the mobility in organic polymer thin film transistors is not constant, but it is gate voltage dependant. By increasing the gate voltage of a transistor, the density of the induced charge carriers at the semiconductor-insulator interface is increased. The induced carriers first fill the lower lying states and any additional carriers would need lower activation energy to jump to the higher states which are more densely populated and have lower energy barriers between them. Hence, an increase of the gate voltage, increases carrier density and also charge carrier mobility. Vissenberg and Matters came up with an analytical expression for the field effect mobility of amorphous organic semiconductors:

$$\mu = \frac{\sigma_0}{e} \left(\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_C \Gamma(1 - T/T_0)\Gamma(1 + T/T_0)} \right)^{T_0/T} \left(\frac{(C_i V_g)^2}{2 k_B T_0 \varepsilon_S} \right)^{T_0/T - 1} , \qquad \text{(Eq. 8.2)}$$

where σ_0 is the semiconductor conductivity, e is the elementary free charge, α is the electronic wave function overlap parameter, B_C is the critical number indicating the onset of percolation, C_i is the gate insulator capacitance per unit area, V_g is the gate voltage, ε_S is the dielectric constant of the semiconductor and T is the temperature. At a given temperature T, the charge carrier mobility can be simplified to [17]-[18]:

$$\mu = \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{aa}} \right)^{\gamma} , \qquad \text{(Eq. 8.3)}$$

where $\gamma = 2\left(\frac{T_0}{T} - 1 \right)$ is indicative of the disorder in the system. μ_0 is the charge carrier mobility at $V_{aa} = V_{GS} - V_{th}$ where V_{aa} is chosen as needed.

8.2 Fabrication of poly-3-hexylthiophene TFTs

The contact resistance effect was studied for the P3HT thin film transistors fabricated on PET (polyethylen-terephthalat) foils in top gate bottom contact configuration. On PET foils, 30 nm thick gold source/drain electrical contacts were structured using standard photolithography with the lift-off process. Gold is chosen for source/drain electrodes because of its work function that is similar to the energy of the HOMO of most of the p type organic semiconductors. Thus, an ohmic contact is formed on the interface between source/drain electrodes and organic semiconductor film. If a small energy barrier existed between the contacts and the semiconductor, the negative applied gate voltage would lower this energy barrier.
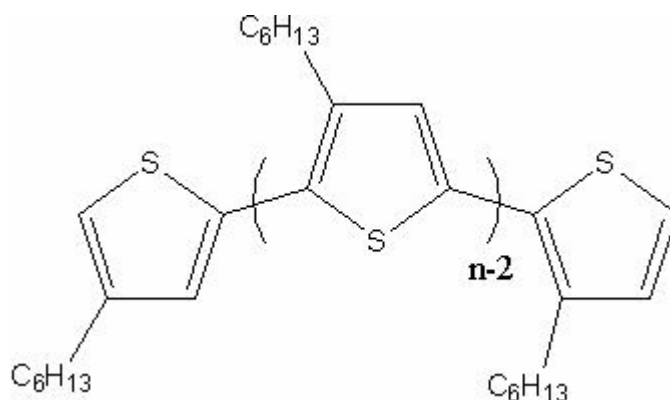

Fig. 8.2 The chemical structure of poly-3-hexylthiophene polymer.

Poly-3-hexylthiophene, P3HT (Fig. 8.2 shows the chemical structure of the polymer), is one of the polymeric semiconductors that have attracted the attention of researchers in recent years. In the carbon backbone of P3HT molecule, single bonds (also known as σ-bonds) and double bounds alternate along the molecule. Each of the double bonds consists of one σ-bond and one π-bond, and while there is a presence of π-bonds charge transport may occur in these molecules.

P3HT is high soluble material in solvent like toluene, dichlorobenzene, chloroform. In this work P3HT polymer was dissolved in chloroform. P3HT exhibits a molecular weight of 40000 g/mol, and a regioregularity of 94% (percentage of monomer that is derived from the same isomer unit). The concentration of P3HT in solutions was set to 1.0 wt%. Solutions were stirred on a magnetic stirrer at elevated temperature of 40 °C, until the solutions became clear. The filtered solutions of P3HT were spin-coated

on the cleaned substrate and heated on the hot plate for 30 seconds at 90 °C. Immediately after the temper treatment, samples were covered with an insulator. The insulator material, in this case PMMA (poly-methyl-methacrylate) was chosen because of its stable performance and beacause it has been used for various industrial applications for decades. PMMA was spin-coated and thermally treated on the hotplate for 5 minutes at 60 °C. The thickness of the insulator layer was measured with the DekTak profilometer and spin-coated films exhibited a thickness of 800 nm. Over the insulator layer, through the pre-structured shadow mask, the gate electrode was deposited. 150 nm of sputtered gold were used to form the gate electrode. Prepared transistors were measured in the dark under ambient conditions.

8.3 Electrical characterization and transmission line method

The typical transfer characteristics of the P3HT thin film transistor that operates in the linear and the saturation regime is shown in Fig. 8.3. The transfer characteristics were fitted with the Visenberg-Matters model and the charge carrier mobility of 0.04 cm^2/Vs (V_{aa}= 50 V) was obtained for devices with 125 µm channel length. The devices performed with a low bulk resistance, which was the limiting factor for the on/off ratio. The on/off ratio of devices was in the range of 40-100. Within the Visenberg-Matters model, the measure of the system disorder can be extracted. The spin coated film of poly-3-hexylthiophene performed with the γ value of 1.5.
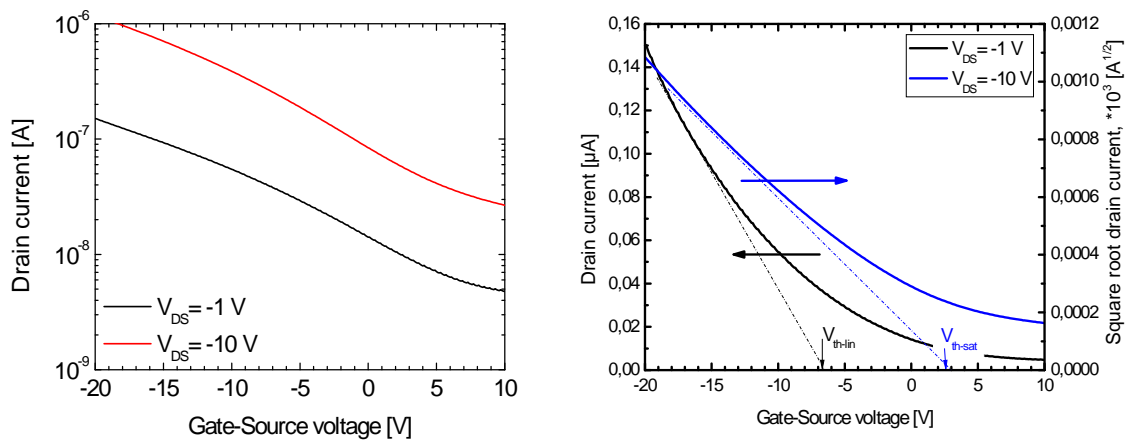

Fig. 8.3 The typical transfer characteristic of a poly-3-hexylthiophene thin film transistor in the bottom contact top gate configuration.

The contact resistance of a thin film transistor can be obtained by the transmission line method (TLM) [19]. The method consists of measuring the total resistance of thin film transistors with different channel lengths in the linear regime of operation. Besides the contact resistance between source/drain metal electrodes and semiconductor layer, one can also determine the channel resistance of a transistor. The TLM method assumes that the channel resistance is the same for different transistors. However, the performed experiments showed a variety of semiconductor film properties from sample to sample, that might lead to higher values of measurements' uncertainty.

The total resistance is calculated as:

$$R_T = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1}.$$

(Eq. 8.4)

According to the TLM method, the total resistance is equal to the sum of the channel resistance and the total contact resistance:

$$R_T = R_{CH} + R_C = \frac{L}{W\mu_0 C_{ox}\left(V_{GS} - V_{th} - V_{DS}\right)} + R_C.$$
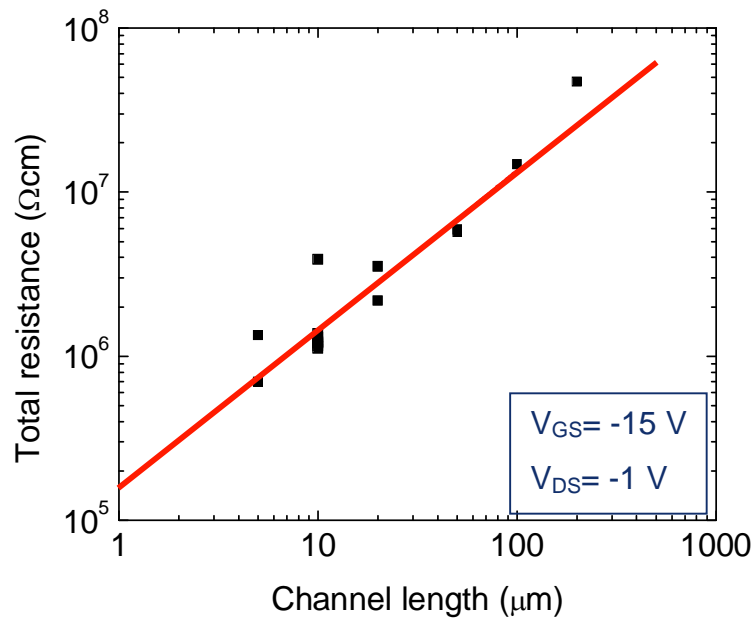
(Eq. 8.5)

Fig. 8.4 The transmission line method of poly-3-hexylthiophene thin film transistors.

The total contact resistance comprises the contact resistance on the source and the drain electrode, $R_C = R_{CS} + R_{CD}$, and can be defined as the total resistance of a transistor with zero channel length. Usually, the total contact resistance is normalized to the channel width of the transistor W, and it is represented within Ωcm units. The plot of the total resistance versus the transistor channel length is shown in Fig. 8.4. Determined data points of the resistance show the linear dependence on the transistor channel length. By making a linear fit through the obtained data, the intercept with the y-axis leads to the contact resistance value.

The normalized contact resistance exhibits the gate voltage dependence. In Fig. 8.5, the influence of the gate voltage on the normalized contact resistance is shown. For the gate-to-source voltage of 0 V, the normalized contact resistance takes the value just above 10^7 Ωcm. With a further decrease of the gate-to-source voltage, the transistor operates in the strong linear regime. Keeping the drain-to-source voltage constant at -1 V, the contact resistance of the devices is decreased. By reaching the gate-to-source voltage of -15 V, the normalized constant resistance has been reduced to the value of 10^5 Ωcm.
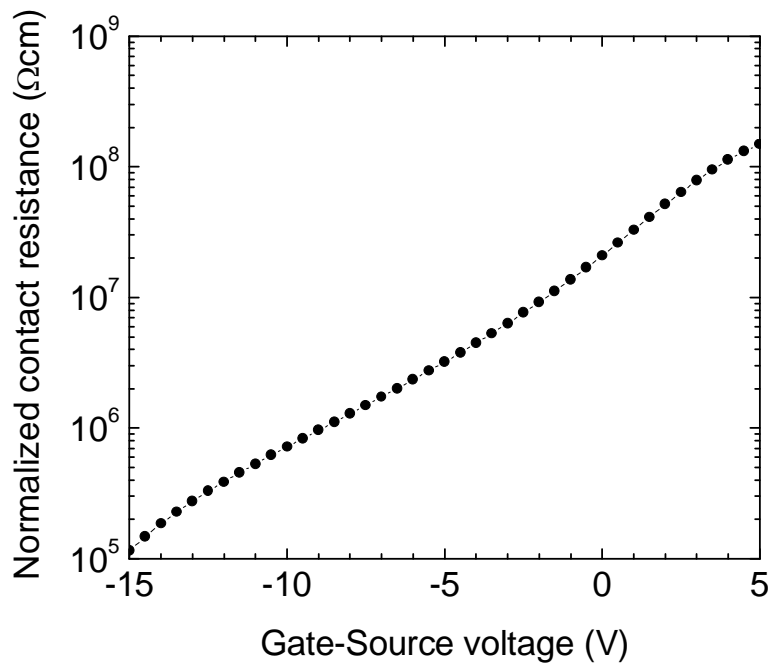

Fig. 8.5 The gate voltage dependence of the normalized total contact resistance. The drain to source voltage has been kept constant to -1 V.

The reason for such behavior of the contact resistance can be explained with the change of the transistor channel conductivity. With an absolute increase of the gate-to-source voltage the transistor channel becomes more conductive. In the other words, the sheet resistance of the semiconductor layer decreases. The contact resistance can also be calculated as:

$$R_C = \sqrt{\rho_C R_{Sh}} \ ,$$
(Eq. 8.6)

where ρ_C is the specific contact resistance, and R_{Sh} is the sheet resistance of the semiconductor layer. The reduction of the channel resistance of the thin film transistor is also visible through the reduction of the normalized contact resistance.

The transmission line method for determining the contact resistance of transistors is an easy way to study the electrical contact of thin film transistors. The method assumes the uniformity of the semiconductor films between different devices that is not the case all the time. Very often solution processed organic based thin film transistors that were fabricated on the same substrate, can exhibit films with different surface morphology or the film thickness. Due to these inconsistencies, the computational error in the TLM method occurs, and it can exceed the nominal value of the contact resistance. Furthermore, the transmission line method extracts the value of the total contact resistance, the sum of the drain and the source contact resistances. In comparison with inorganic devices, organic based thin film transistors suffer from high contact resistance. Closer studies of the charge injection process from the metal to the organic semiconductor (and vice versa) have to be done in order to improve the electrical properties of organic semiconductor materials. Hence, the contact resistances at the source and at the drain electrical contact should be separately monitored which is not possible with the TLM method.

8.4 Channel potential distribution mapping

The mapping of the potential distribution along the channel of thin film transistors has been successfully conducted using Scanning Kelvin Probe Microscopy (SKPM) [20]-[22]. With a SKPM technique, one can determine potential in the transistor channel

with a submicron resolution. The SKPM technique is only suitable for transistors where the channel is in direct contact with the scanning needle of the microscope. Thus, top gate configurations are not suitable for this method of measuring.

It is well known that organic thin film transistors suffer from environmental degradation [23], and thus transistors in the top gate configuration are of more interest to researchers. In such case, the top gate electrode is also used as an encapsulation layer of the active channel. The potential study of the transistor channel in this case can be investigated with a four-probe measurement technique [24]. A four-probe setup consists of two additional metal sense fingers that are buried in the transistor channel between the source and the drain electrodes. While the transistor is turned on, the potential of buried sense fingers is measured.

Potential mapping along the channel with corresponding current measurement in the channel should give a detailed picture on the charge distribution or the resistance in the channel with an estimation of the potential drop at the source and the drain electrode. The potential distribution along the channel for a p-type semiconductor is given as [25]:

$$V(x) = V_{GS} - V_{th} + \left[(V_{GS} - V_{th})^{\gamma+2}\left(1 - \frac{x}{L}\right) + (V_{GS} - V_{th} - V_{DS})^{\gamma+2}\frac{x}{L} \right]^{\frac{1}{\gamma+2}} . \qquad \text{(Eq. 8.7)}$$

The electric field in the channel of the transistor when no potential drop occurs at the contacts is given by:

$$E(x) = -\frac{1}{\gamma+2}\left[(V_{GS} - V_{th})^{\gamma+2}\left(1 - \frac{x}{L}\right) + (V_{GS} - V_{th} - V_{DS})^{\gamma+2}\frac{x}{L} \right]^{-\frac{\gamma+1}{\gamma+2}} .$$
$$\cdot \frac{1}{L}\left[(V_{GS} - V_{th} - V_{DS})^{\gamma+2} - (V_{GS} - V_{th})^{\gamma+2} \right] \qquad \text{(Eq. 8.8)}$$

The illustration of the potential and the electric field in the channel for different values of γ is shown in Fig. 8.6. The illustrated model assumes a transistor with the channel length of 125 µm and with the length of the source/drain electrodes of 10 µm. The threshold voltage is assumed to be 0 V.
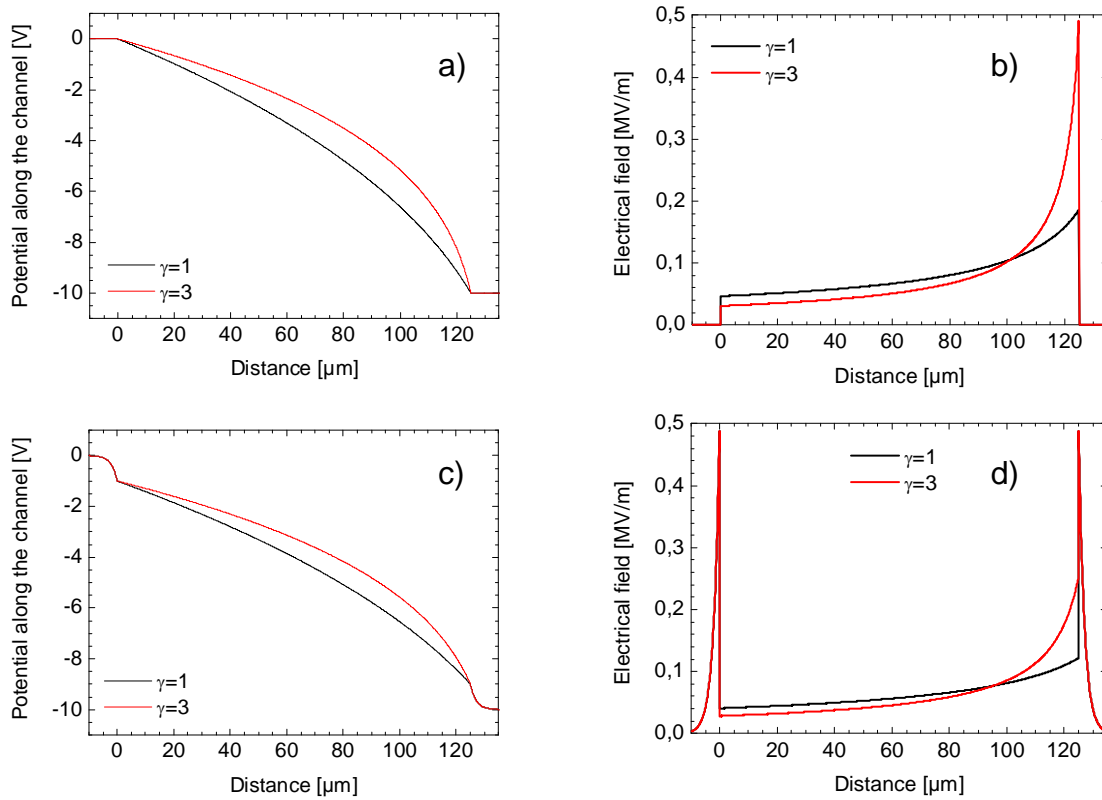
Fig. 8.6 The illustration of the channel potential along: a) an ideal thin film transistor and c) the transistor with an influence of contact resistance (according to the contact resistance model given in Chapter 2 of this thesis and the transfer length parameter of 2 μm). The contact resistance effect in the transistor was modeled with the assumption that the transfer length parameter is 2 μm. The electric field illustration along the transistor channel: b) in an ideal case and d) in the case of a contact resistance effect. The graphs are shown for two different values of the γ parameter. The length of the transistor channel was assumed to be 125 μm and the source/drain electrical contacts are modeled with 10 μm length.

For the films with small values of the disorder parameter, $\gamma=1$, the potential along the transistor channel that operates in the linear regime occurs with the constant drop from 0 V (the potential of the grounded source electrode) to the value of the drain potential, in this case -10 V, Fig. 8.6a. The potential along the semiconductor material that is located over the metal electrodes is constant. For the materials with higher values of the γ parameter, the curvature of the potential curve can be seen. The curvature in the channel potential profile at higher γ values is the consequence of

less available energetic states in disorder films. By studying the profile of the electrical field along the channel, Fig. 8.6b, the strong increase of the electrical field at the drain contact interface occurs as the semiconductor film becomes more disordered. At the same time, the slight drop of the electrical field at the source metal contact occurs.

The mapping of the transistor's channel potential is also used to determine the potential drops at the metal electrodes caused by the contact resistance at the source/drain electrical contacts in thin film transistors. Due to the contact effects the potential drops occur at the source and the drain electrical contacts. In the case the contact resistance may not be neglected, the equation 8.7 that is describing the potential along the channel has to be modified. The gate-to-source and drain-to-source voltages take the new form:

$$
\begin{aligned}
V_{GS} &\Rightarrow V_{GS} + dV_S \\
V_{DS} &\Rightarrow V_{DS} - dV_D + dV_S
\end{aligned}
\text{,}
$$

(Eq. 8.9)

where dV_D and dV_S are the potential drops occurred due to the contact resistance effect at drain and source electrode, respectively. The contact resistances at source and drain electrical contact can be determined as:

$$
\begin{aligned}
R_{CS} &= \frac{dV_S}{I(V_{DS}, V_{GS})} \cdot W \\
R_{CD} &= \frac{dV_D}{I(V_{DS}, V_{GS})} \cdot W
\end{aligned}
\text{.}
$$

(Eq. 8.10)

Fig. 8.6c shows the potential distribution along the transistor channel and also the distribution in the semiconductor material that is located over the metal electrodes. In the case where the contact resistance is not neglected, the potential distribution in the region above the metal contact differs from the case where there were no contact effects. The drop of the potential in this region is modeled with the resistive network as described in Chapter 2 of this thesis. The illustration assumes the voltage drop of 1 V and the transfer length parameter of 2 μm for both source and drain electrical contacts. The profile of the electrical field along the channel stays unchanged, while changes occur only in the region above the metal contacts. Because of the assumed equal potential drops at the source and the drain electrodes, the electrical field over these two contacts is the same.

In order to study the potential profile, the channel of the fabricated thin film transistors was enriched with additional buried sense fingers (electrodes) in the channel, as illustrated in Fig. 8.7a. An investigation of contact properties was done on transistors with the channel width of 10000 µm and the channel length of 125 µm. The sense fingers were structured in the same fabrication step as the source and the drain electrodes. In the transistor channel 12 sense finger electrodes (with a width of 5 µm) were structured on the distance from the source/drain electrodes of 7.5 µm, 17.5 µm, 27.5 µm, 37.5 µm, 47.5 µm, 57.5 µm, 67.5 µm, 77.5 µm, 87.5 µm, 97.5 µm, 107.5 µm and 117.5 µm. Each of these 12 sense fingers are connected to the voltage follower circuit with operational amplifiers, Fig. 8.7b. The high input impedance of the operational amplifiers of 10^{13} Ω, makes the input leakage current through the sense fingers several orders smaller than the actual drain current that is flowing through the device. The output signal from the operational amplifier is halved with the voltage divider before sending the signal to the ADC converter (Analog to Digital Converter). The ADC converter works with ±10 V supply voltage and the voltage divider allows the use of a wider range of applied drain to source voltages. Additional blocking capacitors were added to the circuit in order to minimize any oscillations of the sensed signals.
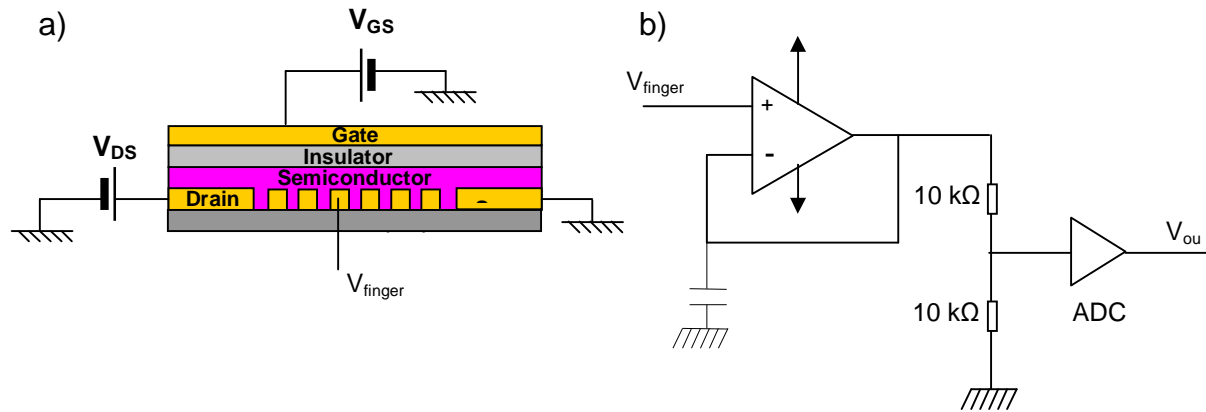

Fig. 8.7 a) The cross section schematic of a thin film transistor in the bottom contact top gate configuration with buried sense fingers along the transistor channel. b) The scheme of the electrical circuit used for measuring potential on the sense finger in the transistor channel.

In addition to the measurement of the transfer characteristic of a thin film transistor, the potentials of all twelve sense fingers are recorded simultaneously for all applied

gate voltages. The potential data is collected from the sense fingers for different combinations of applied drain to source and gate to source voltages. The potential profile of the transistor channel is made by plotting the obtained data. The obtained data is in agreement with theoretical values for the potential distribution given in the equation 8.7. Extraction of the voltage drop at the source and at the drain contact electrode is not simple and demands the numerical interpolation of measured data. The extraction of the voltage drops at source/drain electrodes was done numerically, by interpolating the measured data with equation 8.7. The numerical values of the interpolation function at the ends of the channel give the values of the potential drops that occur at the source/drain electrodes due to the presence of the contact resistance.
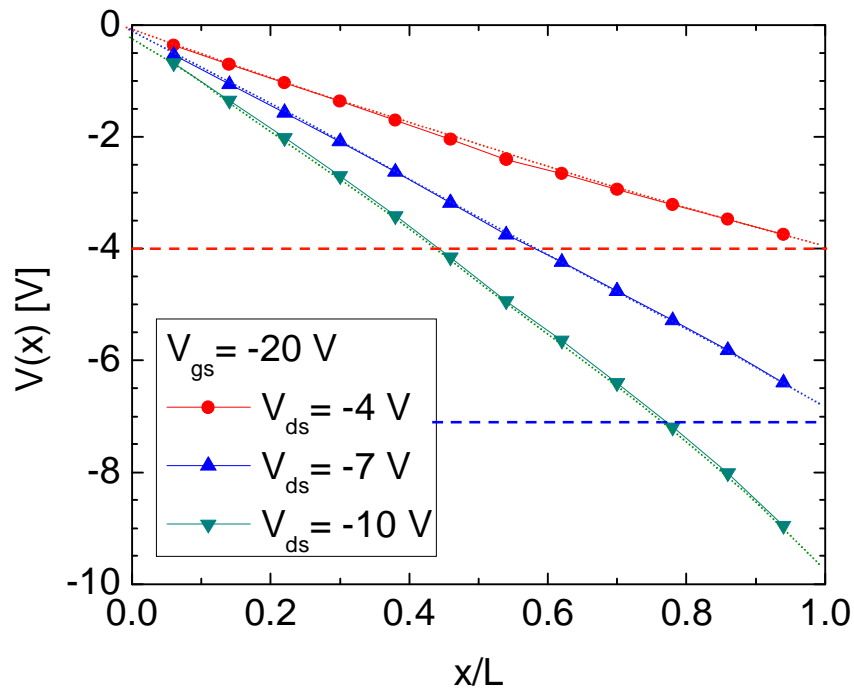

Fig. 8.8 The potential distribution along the channel of a poly-3-hexylthiophene (1,0 wt% in chloroform) thin film transistor when the transistor operates in the linear operation mode.

Fig. 8.8 shows the obtained measurements of potential mapping of P3HT thin film transistors for different applied drain voltages. The dots represent measured potential in the corresponding channel position, and the dashed lines are extrapolated values

for the potential profile along the channel obtained with the equation 8.7. As the drain voltage increases, the potential drop at the contact electrodes increases, as one may observe in Fig. 8.8. When the transistor operates in the strong linear regime (illustrated with red data points and the red line), the channel potential decreases linearly, as measured from the drain to the source contact. With an increase of the drain voltage, the transistor is approaching the pinch-off state (the green data points and the green extrapolated line), and the bending of the potential profile occurs.
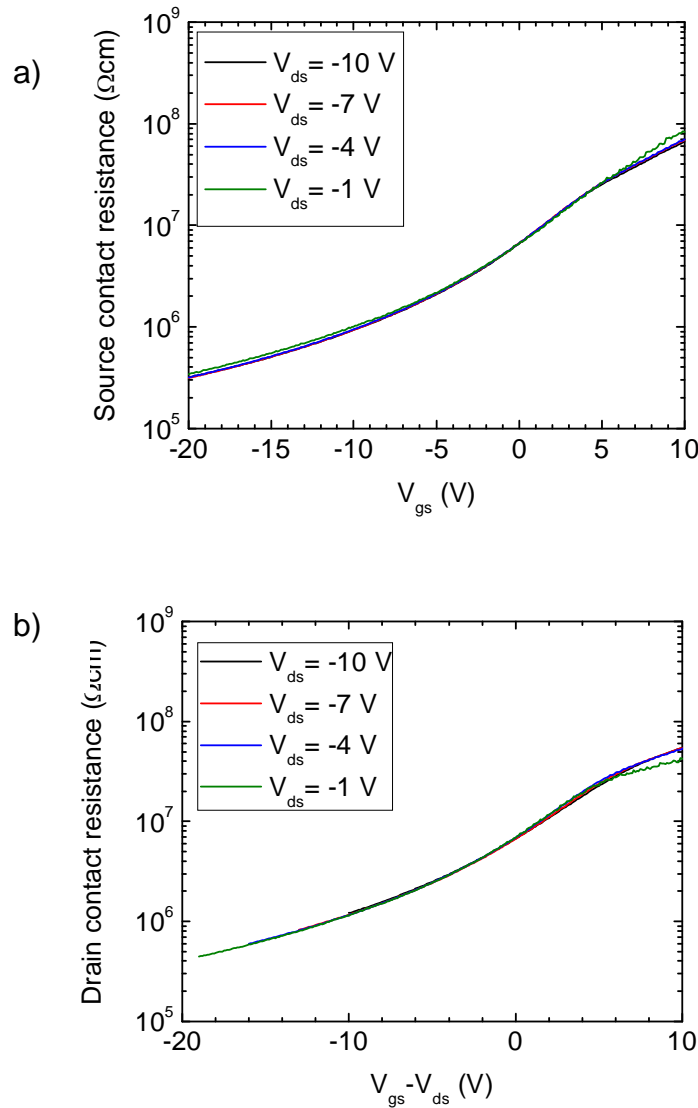

Fig. 8.9 The gate voltage dependence of the contact resistance of P3HT-Au electrical contacts. Figures a) and b) show the voltage dependences of the source and the drain contact resistance, respectively, of poly-3-hexylthiophene (1.0 wt% in chloroform) thin film transistors with gold electrical contacts.

Using the equation 8.10, the contact resistances between gold drain and source electrodes and semiconductor are obtained. Fig. 8.9 shows the influence of the applied drain to source and gate to source voltages on the contact resistances at the source and the drain electrode separately. The source contact resistance is reduced with an increase of the applied gate voltage, as a consequence of higher channel conductivity. Furthermore, the source contact resistance stayed independent on the increase of the drain to source applied voltage. The dependence of the drain contact resistance on applied gate and drain voltages is shown in Fig. 8.9b. In order to keep the electrical field independent of the applied drain voltage, the plot shows the contact resistance dependence on the gate to drain voltages ($V_{GD}=V_{GS}-V_{DS}$). As the gate voltage increases, the drain contact resistance reduces its value in a similar way as the source contact resistance. In addition, changes of the drain to source electrical field do not influence the change of the drain contact resistances. Thus, we may say that the total contact resistance of transistors in top gate bottom contact configuration is only gate voltage dependant.

Both source and drain contact resistances exhibit similar values. The sum of these two resistances gives the total resistance of the analyzed transistor. The total contact resistance value, obtain by conducting a potential mapping of the transistor channel is in the same range as the contact resistance obtained by the TLM method. This confirms that the potential mapping of the transistor channel may be used to determine the contact resistance and furthermore to determine the individual contributions of source and drain contact resistances.

The properties of electrical contacts are summarized in Fig. 8.10, where the drain current is plotted versus the potential drop at source/drain electrical contacts. The solid lines represent the contact behavior at the source, and the dashed lines stand for the drain electrical contact. The linearity of these plots indicates that gold source/drain electrodes make good ohmic contacts to poly-3-hexylthiophene semiconductor. Furthermore, the overlap between solid and dashed lines for low gate voltages (V_G= -1 V) indicates that the processes of injection and extraction of charges occur with similar properties at the source and the drain electrode. Increasing the gate voltage, curves plotted for the same applied voltages (plotted with the same color) start to branch from each other. As the gate potential increases within the absolute value, the slope of the line representing the electrical properties of the

source electrical contact becomes steeper than the one representing the electrical properties at the drain electrode. The reason for such behavior may be the numerical uncertainty of the extrapolation function within MATLAB programming, used for determining source/drain potential drops. Namely, the values of the potential drop determined at the drain contact were several times higher than those for the potential drop at source electrical contact. High values of extrapolated potential drop at drain electrical contact may lead to higher uncertainties in calculations for drain contact resistance compared to those for source contact resistance.
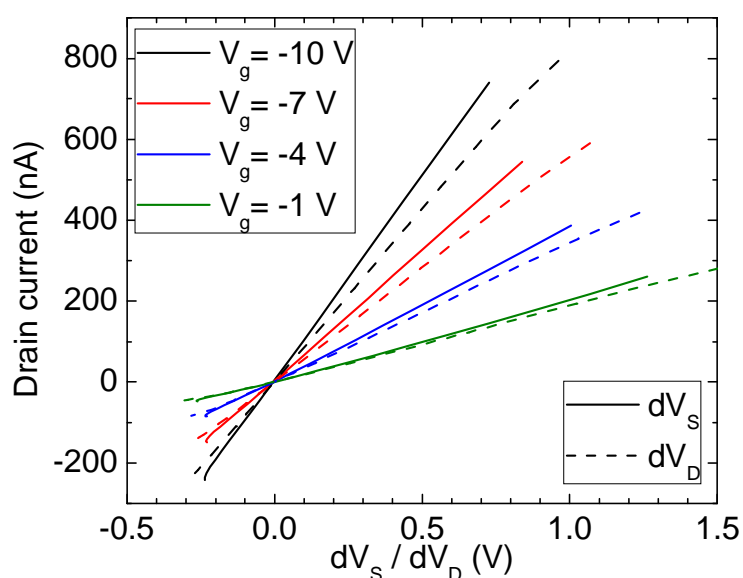

Fig. 8.10 The electrical properties of the gold/poly-3-hexylthiophene electrical contacts.

8.5 Influence of film thickness on contact resistance

The growth of organic semiconductor films plays a major role in the ordering of organic molecules on a substrate and also in the performance of charge transport in organic field effect transistors. In the next step, the film thickness of poly-3-hexylthiophene film was studied for its influence on the contact resistance. Poly-3-hexylthiophene was dissolved with different weight concentrations in chloroform

solution. The weight percentage of P3HT was varied from 0.1 wt% to 2.0 wt%. The solutions were spin coated on the PET foils with prestructured source/drain electrodes, and the deposited films differ within the film thicknesses and the film morphology. The highly diluted solutions, with 0.1 wt% of poly-3-hexylthiophene exhibited a film thickness of 18 nm with a small crystal size. With the increase of the concentration of poly-3-hexylthiophene chains in the solution, the film thickness becomes higher and the grain size of poly-3-hexylthiophene polymer increases. The solution of 1.0 wt% resulted in a film thickness of approximately 81 nm, while a film thickness of around 175 nm was achieved with the solution with 2.0 wt% of poly-3-hexylthiophene. The dependence of the charge carrier mobility on the concentration of the poly-3-hexylthiophene in the chloroform solution is shown in Fig. 8.11.
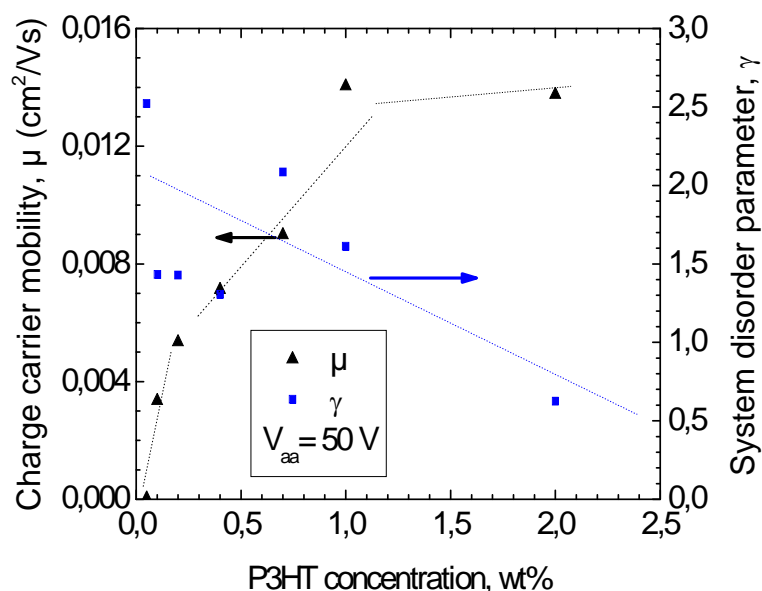

Fig. 8.11 The charge carrier mobility and the measure of disorder films dependence as a function of the concentration of the poly-3-hexylthiophene films in thin film transistors. Measured data points (dots) were averaged over 18 different devices. The dashed lines show the trend in the behavior of these two parameters.

As the weight concentration of P3HT solutions increases and the crystallinity of films improves, the charge carrier mobility of the spincoated films increases. The charge carrier mobility (at V_{aa}=50 V) of highly diluted films resulted in mobilities of below $5 \cdot 10^{-3}$ cm^2/Vs. The charge carrier mobility continues to increase with high concentrations of polymer in the film. For the films with concentrations above 1.0 wt%

the films performed with saturated values of the mobility of around $1.4 \cdot 10^{-2}$ cm^2/Vs. Sandberg et al. gave an explanation for the low charge carrier mobility in very thin films in bottom gate devices [26]. Due to interface strains, the order of molecules at the interface with the substrate is very poor causing devices with the small film thickness to perform with low charge carrier mobility. As the film thickness increases, higher layers of P3HT molecules may establish films with higher order and thus devices may perform with higher charge carrier mobility. As the film thickness increases further, the influence of the substrate becomes less dominant, and the charge carrier mobility of films saturates with its value.

Fig. 8.11 also shows the dependence of the measure of disordered films on the concentration of P3HT in chloroform solution. As the concentration of poly-3-hexylthiophene in the solutions increases, the influence of the substrate on the film growth decreases and films perform with higher order. The γ parameter reduces its values from 2.5 for the films with 0.05 wt% P3HT molecules, down to 0.55 for the films with 2.0 wt% concentration. Such a behavior is in agreement with the previous study of poly-3-hexylthiophene thin film morphology conducted by Gburek et al. [18].
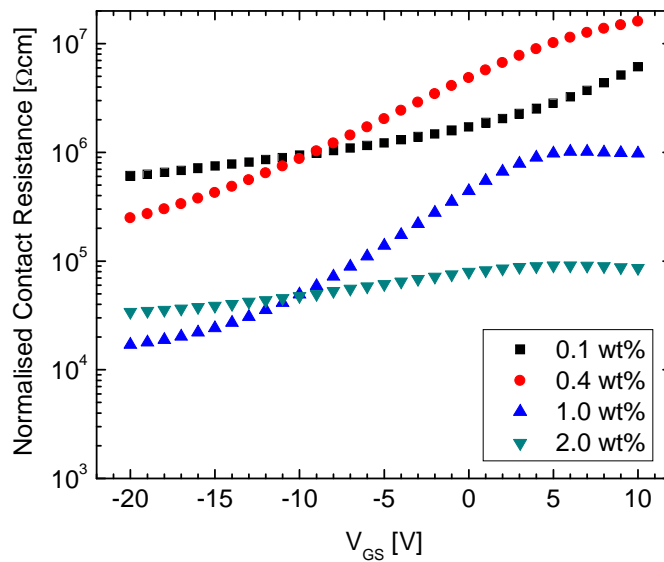

Fig. 8.12 The dependence of the normalized contact resistance on the gate to source voltage for different concentrations of poly-3-hexylthiophene solutions.

Furthermore, the contact resistance of the prepared samples was extracted with the transmission line method. The obtained results of the contact resistance were plotted

versus the gate-to-source voltage, Fig. 8.12. The drain to source voltage was kept constant during the experiment at V_{DS} = -1 V. General observation, as the gate voltage increases, the contact resistance of P3HT thin film transistors reduces for all fabricated samples from solutions with different weight concentrations of P3HT.

In the case of samples manufactured from highly diluted solutions (samples with 0.1 wt% and 0.4 wt%), the contact resistance of Au/P3HT electrical contacts decreases from 10^7 Ωcm to $5 \cdot 10^5$ Ωcm with a decrease of the gate voltage from 5 V to -20 V. For small gate-to-source voltages (below -5 V), the depletion width of the transistor channel takes the whole film thickness. The small variations between two curves (0.1 wt% and 0.4 wt%) may be attributed to an uncertainty of the TLM method. As P3HT concentration in the solution increases, the total contact resistance decreases. In the case of devices made from 1.0 wt% solution, they exhibit a film thickness of 80 nm that is higher than the height of the deposited gold electrodes. Thus, most of the charge transport occurs in the region above the metal electrodes, and a smaller amount of charges is transferred over the side of the electrodes, as it is in the case of thinner P3HT films. When the contact area between gold and P3HT is increased, the contact resistance between these two materials decreases.

With a further increase of the concentration in the P3HT solution, the thickness of the spincoated films is increased. Devices made of poly-3-hexylthiophene solution with 2.0 wt%, the contact resistance reduces its value down to 10^5 Ωcm and slightly reduces its value with an increase of the gate-to-source voltage. In this case P3HT film exhibits the film thickness of 175 nm that is higher than the thickness of sputtered drain/source metal contacts. Since thin film transistors are fabricated in bottom-contact top-gate configuration, the conductive channel is formed opposite to the source/drain contacts. Due to the higher thickness of the semiconductor film compared to 1.0 wt%, more charges overflow the contact area, which leads to the higher contact resistance. Thus, in the case of highly conductive channels (V_{GS}= -20 V), the contact resistance exhibits a higher value than in the case of 1.0 wt% solution.

In the next step, the potential distribution along the channel was measured in order to separately analyze contact resistance at the source and at the drain electrical contacts. The potential mapping technique was used to study the potential distribution along the transistor channel. The thin film transistors were processed

from solutions with different weight concentrations of poly-3-hexylthiophene. The thin film transistors were manufactured in the top gate bottom contact configuration with the buried sense fingers structure. Measuring the potential over the buried sense fingers electrodes, the map of potential distribution along the channel was made. Extrapolating measured data, the potential drops at the source and drain electrical contacts were determined. Fig. 8.13 shows the influence of the applied gate-to-source voltage on the source and drain contact resistances for V_{DS}= -10 V. The solutions with the higher concentrations of poly-3-hexylthiophene, above 1.0 wt%, coagulated during the process, and thus electrical properties of those devices couldn't be determined. Both contact resistances appear to be independent on the change of the drain electric field. However, the obtained results from the potential mapping method are not in agreement with the results obtained with the TLM method. The contact resistance obtained with 12-point setup is one magnitude higher than in the case of contact resistance values determined with the TLM method. The reason for that might be incorrect data acquisition from the operational amplifiers in the measurement setup.
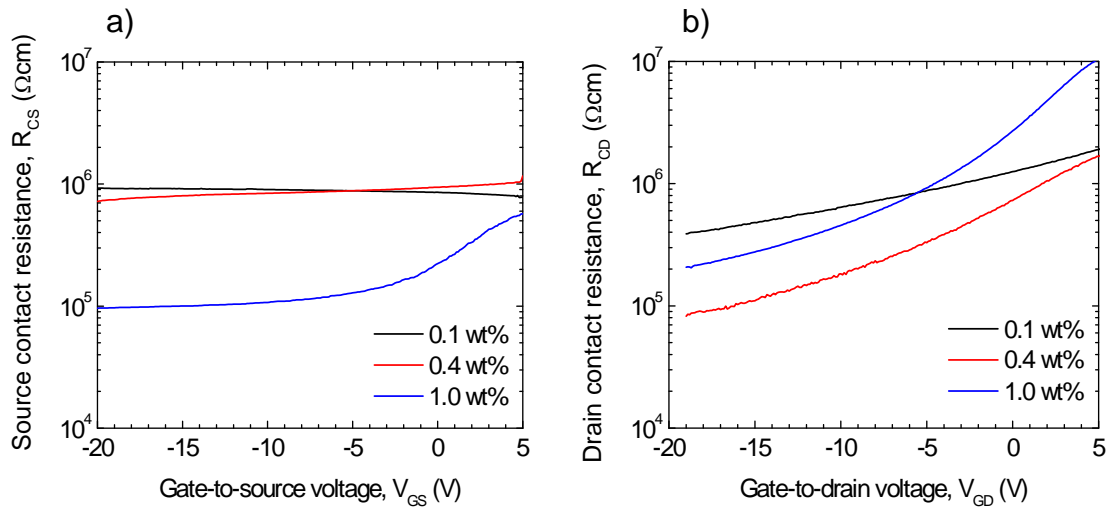

Fig. 8.13 a) Source and b) drain contact resistance of the poly-3-hexylthiophene-gold electrical contacts as a function of applied gate voltage and different semiconductor concentrations. The applied drain to source voltage was V_{DS}= -10 V.

For the devices made from the solution with small P3HT concentrations, the source contact resistance remains constant in the range of 10^6 Ωcm. The source contact

resistance remains unchanged when the concentration is increased from 0.1 wt% to 0.4 wt%, Fig. 8.13a. At the same time, the drain contact resistances of devices made from 0.1 wt% and 0.4 wt% solutions decrease, as the gate voltage increases, Fig. 8.13b. The decrease of the drain contact resistance is more prominent in the case of 0.4 wt% solution than for devices made from 0.1 wt% P3HT solutions, which may be attributed to the film with larger depletion region of the channel and larger effective contact area between Au and P3HT molecules.

With the higher concentrations of poly-3-hexylthiophene molecules in the chloroform solution (1.0 wt%), the film thickness increases, and the film overgrows the height of the metal electrodes. At this point, the current transfer from gold to the semiconductor film occurs not only through the side edges of the metal electrodes, but charges flow over the top surface of electrical contacts. As the gate voltage decreases from 5 V to -20 V, the source contact resistance reduces from $5 \cdot 10^5$ Ωcm to 10^5 Ωcm, and the drain contact resistance drops from 10^7 Ωcm to $2 \cdot 10^5$ Ωcm.

As the film thickness increases, the measure of disorder system, γ parameter, decreases from 2.5 to 1.5, and the charge carrier mobility is increased several times. Thus, one would expect an improvement in the contact resistance when the film morphology is improved. The drain contact resistance exhibits the variation of its value for a factor of 2-3 when different solution concentrations are used to make thin film transistors. This variation is not sufficient to explain the changes of the contact resistance to the film morphology. It is more likely that it is due to the uncertainty of numerical calculations.

In the case of transistors processed with 1.0 wt% P3HT solution, the obtained results of the drain contact resistance are in an agreement with the results presented in Fig. 8.9. On the other hand, values of the source contact resistance strongly deviate from the previous results shown in Fig. 8.9. Such trend of both contact resistances indicates possible problems with the measurement setup and the operational amplifiers which are used for sensing the potential inside of the transistor channel close to the source metal electrode.

Finally, the properties of the electrical contacts were studied through the plot of the drain current as a function of the potential drop that occurs over the electrodes. Fig. 8.14 shows the properties of the source electrical contact. The graph shows the strong linearity and passes through the origin. That leads to the conclusion that the

electrical contacts between gold and P3HT resulted with the ohmic behavior. The process of injection and extraction of charges in and from the channel are happening in similar manner since the line is symmetrical to the origin. Furthermore, one can see that the lines with lower solution concentrations, i.e. 0.1 wt% and 0.4 wt%, are overlapping and hence these samples exhibit similar values of contact resistances. The slope of the I_D-dV_S plot for the samples made from solutions with 0.1 wt% and 0.4 wt% is lower than the one for the samples based on 1.0 wt% P3HT solution. For the same voltage drop over the electrode, more current flows through the devices with thicker semiconductor films. As a consequence, these devices perform with lower contact resistance.
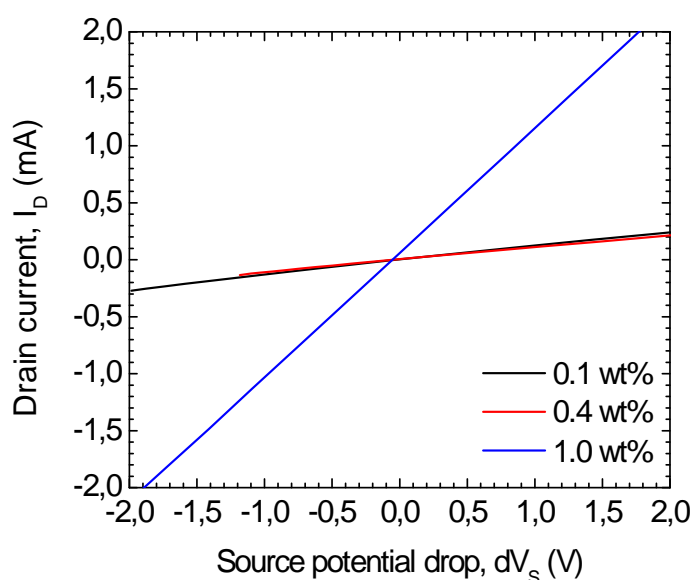

Fig. 8.14 The plot of the drain current versus the potential drop at the source electrical contact. The graph is given for different solution concentrations. The transistors were operating with the applied drain voltage of V_{DS}= -10 V.

8.6 Summary

Organic thin film transistors based on solution processed poly-3-hexylthiophene polymers were investigated, as well as the properties of gold electrical contacts in such devices. The influence of the contact resistance on the performance of the

devices in top-gate bottom-contact configuration was studied. Two different methods for determining the contact resistance were presented namely the conventional transmission line method (TLM) and the method of the potential mapping along the transistor's channel. The method of potential mapping is the superior method for determining the total contact resistance, as well as for determining separate influences of the source and the drain electrical contacts. The gold/poly-3-hexylthiophene electrical contacts exhibited Ohmic properties. The injection and extraction of charges from gold electrodes to the semiconductor material and vice versa are happening in a similar manner. Furthermore, the film thickness and morphology properties of the semiconductor material were studied for their influence on the contact resistance. When the film thickness is lower than the actual height of the metal contacts, the transfer of the charges on metal-semiconductor junctions are taking place on the side edges of the metal electrodes. For thin films, the contact resistance didn't show any dependence on the charge carrier mobility nor the film morphology. As the organic semiconductor is deposited to make thicker films with thicknesses higher than the actual height of metal electrodes, most of the charges are transferred from the semiconductor to the metal contact over the top surface of source/drain electrodes. With the further increase of the film thickness, more overflows of electrical charges occur in the region above the electrical contact, and the bulk current limits the performance of devices. In such case, determined values of the contact resistance are screened by the bulk resistance of the semiconductor.

8.7 References

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Chapter 9

Contact resistance model for organic thin film transistor based on small molecules

9.1 Introduction

Organic thin film transistors (OTFTs) have been the spotlight for both academic and industrial research in recent years [1]-[3]. With low fabrication costs, and possibility of fabrication on flexible materials, the field of organic electronic is expanding towards flexible displays, identification tags, etc [4], [5]. Efforts to enhance the mobility and increase the switching speed of transistors have opened interesting questions about limiting factors of organic transistors. A large number of small molecule semiconductors have been investigated, and it is fair to say that pentacene and sexithiophene molecules deposited through thermal evaporation are taking the prime spot in those studies. The charge carrier mobility of the pentacene thin film transistors has reached the charge carrier mobility comparable to the amorphous silicon. The value of 1-3 cm^2/Vs for the charge carrier mobility has been reached with a pentacene films with a grain size of 1-5 μm. The charge transport in the pentacene transistors is happening similarly to the transport in polymers, within one-two monolayers of the semiconductor material. With decreasing channel length of the transistors, the drain and source contact resistance becomes an important parameter limiting the device charge carrier mobility and the switching speed of transistors.

Strictly speaking, when the channel length is small enough that the contact resistance dominates over entire resistance of the transistor, there is limited practical benefit of further reduction of channel geometry. Therefore, understanding of electrical properties of the contacts, and their influence on the behavior of the transistors is essential to improve the performance of organic thin film transistors and circuits. Pentacene transistors with top drain and source contacts exhibit a distinctly lower contact resistance compared to transistors with bottom drain/source contacts. The electronic properties of the contacts strongly depend on the structural properties of the pentacene films. In this study the influence of contact effects on the properties of pentacene thin film transistors is investigated and the limits of device performance are identified. This chapter is dealing with a new model that helps to give a better understanding of contact problems in organic thin film transistors.

9.2 Fabrication of pentacene based thin film transistors

Contact resistance is considered as a voltage drop over the contacts, and it can be observed through the resistive network shown in Fig. 9.1. The schematic cross section of the realized pentacene thin film transistor in bottom gate coplanar configuration is shown in Fig. 9.1a. Devices were fabricated on a highly doped silicon wafer. The gate dielectric of the transistor was formed by a 100 nm thick thermally grown silicon oxide layer. Gold electrodes were deposited by optical lithography and the liftoff process in a way to define the bottom drain and source electrical contacts. To improve the adhesion of the gold drain and source contacts on the substrate, a 2-3 nm thick titanium film was evaporated preceding the gold film. Fabricated devices have the channel length varied from 1 μm to 100 μm and the channel width of 50mm. Before depositing the pentacene molecules, the gate oxide was treated with piranha solution and afterwards thermally treated with hexamethyldisilazane (HMDS) in order to make the surface of the silicon dioxide hydrophobic. The pentacene molecules were deposited by Organic Molecular Beam Deposition (OMBD) and the deposition rate was kept 1 nm/min. The final thickness of the pentacene films was determined to be 50 nm. Further details on the fabrication and the deposition of pentacene films can be found in [6] and [7]. Electrical measurements of fabricated devices were performed in darkness and at room temperature.
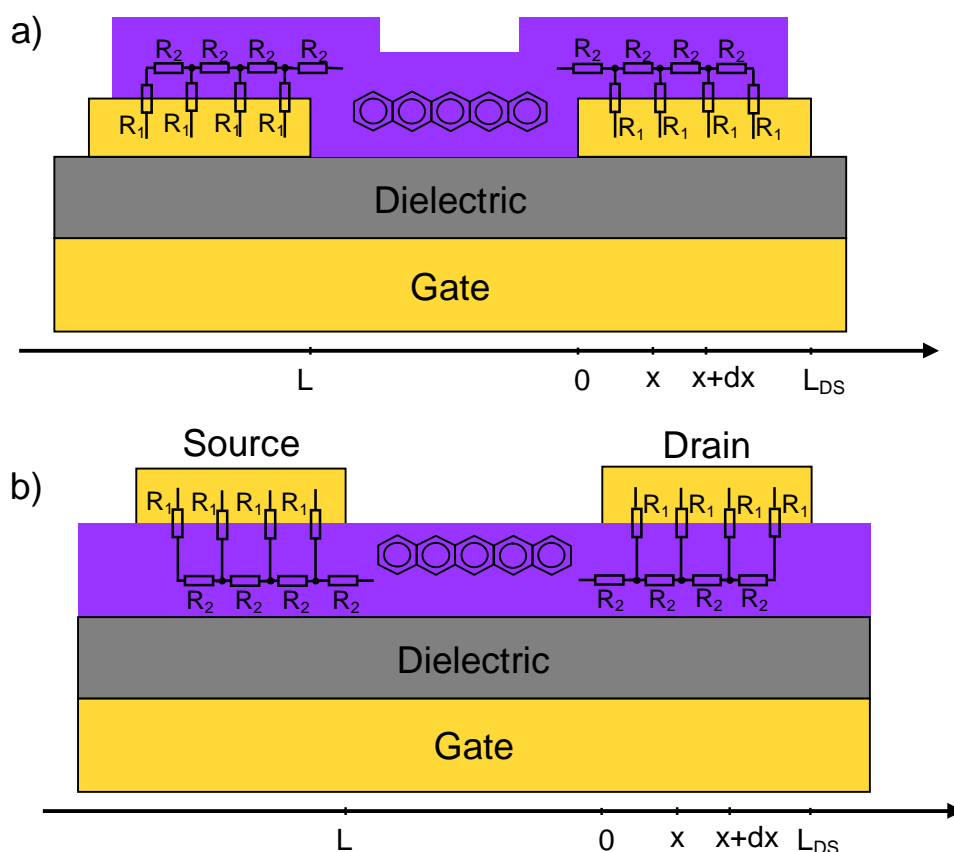
Fig. 9.1 Schematic cross-section of a) a bottom-gate inverse coplanar and b) a bottom-gate inverse staggered pentacene thin-film transistor.

In this chapter, the experimental results of the pentacene thin film transistors published by different research groups are collected in order to verify the model for the contact resistance. In addition to the results on the inverse coplanar geometry, the model can be used for analyzing the organic thin film transistors in the bottom gate staggered configuration as well, Fig. 9.1b.

9.3 Electrical properties of pentacene based thin film transistors

The performance of fabricated devices is analyzed through the transfer and output characteristics. The typical transfer and output characteristics of a transistor with the channel length of 5 µm are shown in Fig. 9.2. The pentacene thin film transistors performed with the subthreshold voltage of 2.7 V and the off current of the devices is measured to be in the range of 10^{-10} A. The devices performed with the on/off ratio of 6 orders of magnitude when the thin film transistors operate in the linear regime.

From the output characteristics one can see that the short channel devices exhibit the nonlinear behavior in the linear mode of operation. The nonlinear properties (also known as a "S-shape") in the output curves at low V_{DS} voltages are commonly seen for the short channel devices in the coplanar TFT configuration [8]. Such behavior is attributed to the effect of nonlinear contact resistance between source/drain electrodes and the organic semiconductor.
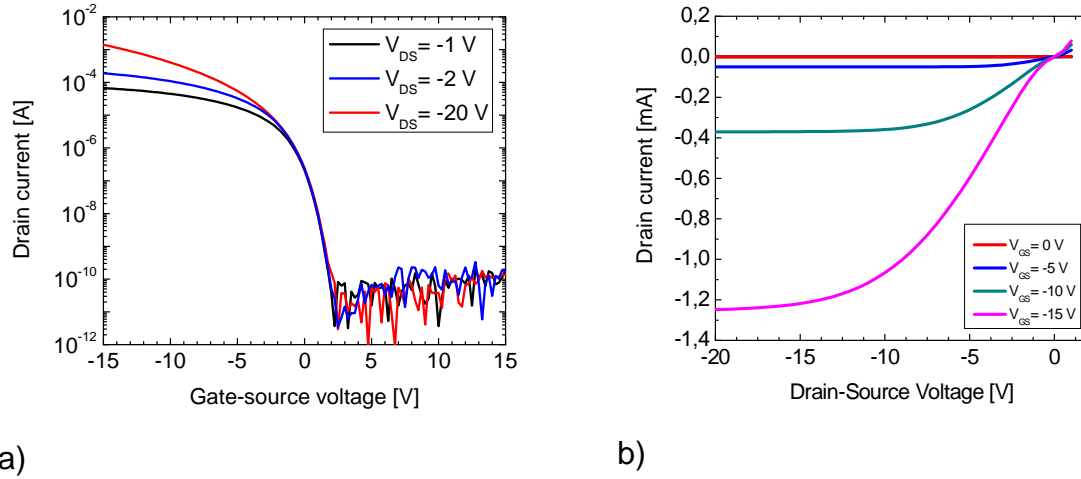

a)   b)

Fig. 9.2 a) The transfer and b) the output characteristics of a 5 µm pentacene thin film transistor and 50 mm channel width.

The device carrier mobilities of the measured pentacene thin film transistors were extracted from the transfer characteristics in the linear region of operation, and plotted as a function of the channel length in Fig. 9.3. In the linear regime of operation the drain current can be described by:

$$I_D = \frac{W}{L}\mu_{eff}C_G V_D \cdot \left(V_G - V_T - \frac{V_D}{2}\right),$$

(Eq. 9.1)

where μ_{eff} is the device carrier mobility, C_G is the gate capacitance per unit area, V_G, V_D and V_T are the gate, the drain and the threshold voltage, respectively, and L and W are the channel length and width of transistors, respectively. The device carrier mobility can be described by equation 9.2 taking into account the contact resistance, R_C [9]:

$$\mu_{eff} = \mu_0 \cdot \frac{L}{L + WC_G R_C \mu_0 \left(V_G - V_T - \dfrac{V_D}{2} \right)} ,$$

(Eq. 9.2)

where μ_0 is the intrinsic field effect mobility of the semiconductor. The device carrier mobility of the transistors drops with decreasing channel length. Using the equation 9.2, the intrinsic charge carrier mobility of 0.373 $cm^2V^{-1}s^{-1}$ for transistor with bottom drain and source contacts were extracted. Furthermore, the experimental data from literature are added to the graph. The experimental data of Jin *et. al.* and Gundlach *et. al.* were also fitted by equation 9.2 and a good agreement between the experimental data and the fit was observed [10]-[11].
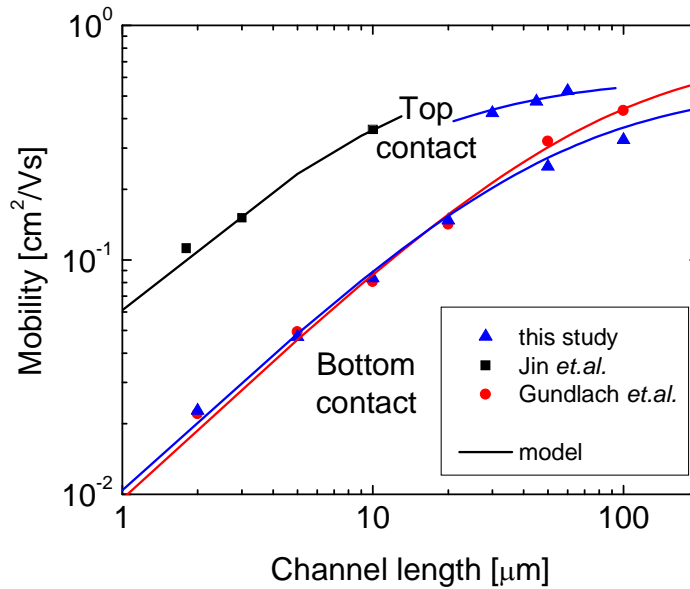
Fig. 9.3 Charge carrier mobility of pentacene thin film transistors as a function of the channel length. The solid lines represent the fits of the effective charge carrier mobility. Experimental data of Jin *et. al.* and Gundlach *et. al.* was taken from references [10] and [11].

For short transistor channels, the measured device carrier mobility of transistors in staggered contact configuration is higher than the one for transistors in inverse coplanar configuration. For longer transistor channels the device charge carrier mobility converges to similar values. The low device carrier mobility of the transistors in the bottom contact configuration is caused by a higher contact resistance.

However, the fit does not take the voltage dependence of the contact resistance into account.

The gate voltage dependence of the contact resistance can be measured by using the transmission line method (TLM) [12]. In general the contact resistance of a metal-semiconductor interface can be described by the resistive network shown in Fig. 9.1a and Fig. 9.1b. The contact region can be divided in infinitely small slices, and the contact resistance of each of the slice is represented by $R_1 = W\rho_c/dx$, where dx is the length of the infinitely small slice and ρ_c is the specific contact resistance between pentacene film and gold electrode. The resistance along the slice of the semiconductor can be described by $R_2 = R_{Sh}/Wdx$, where R_{Sh} is the sheet resistance of the pentacene film.

Based on this model the normalized contact resistance, r_c, is given by:

$$r_C = R_C W = \sqrt{\rho_c R_{Sh}} \coth\left(\frac{L_{DS}}{L_T}\right),$$
(Eq. 9.3)

where L_{DS} is the length of the metal electrodes. The parameter L_T, known as transfer length, defines the critical distance over which most of charges are transferred from the metal contacts to the semiconductor. The transfer length is given by:

$$L_T = \sqrt{\frac{\rho_c}{R_{Sh}}}.$$
(Eq. 9.4)

Since the length of the electrode can be assumed to be larger than the transfer length, equation 9.3 simplifies to

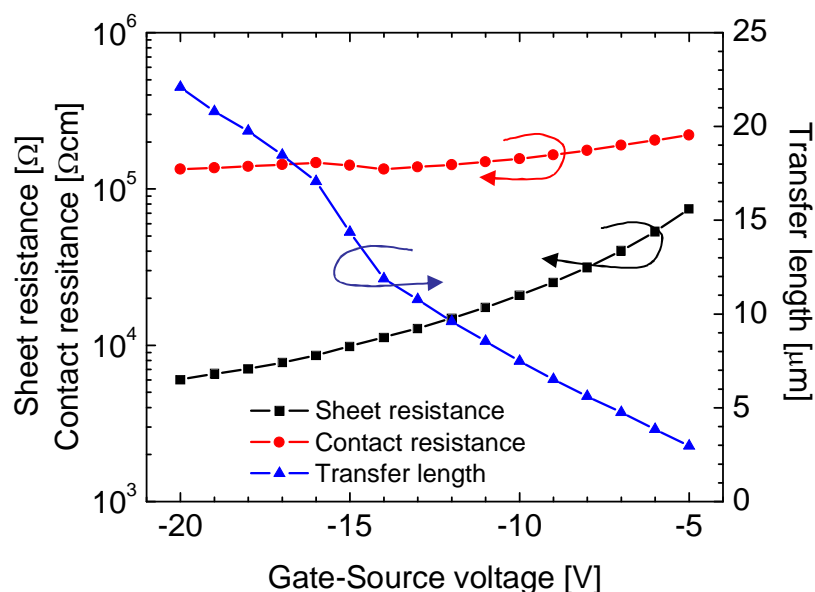$$r_C \approx \frac{\rho_c}{L_T}.$$
(Eq. 9.5)

Fig. 9.4 The contact resistance, the sheet resistance and the transfer length dependence on the applied gate-to-source voltage. Results obtained with the TLM method.

From the TLM method the sheet resistance, the contact resistance and the transfer length parameter are extracted. Their plot as the function of the applied gate-to-source voltage is shown in Fig. 9.4. As the applied voltage is increased (in the absolute values) the sheet resistance drops from 70000 Ω to 5000 Ω due to the increase of the charge carrier concentration in the transistor channel. The contact resistance also performed with a drop, and that behavior is going to be analyzed in more details in the following subchapters. On the contrary to these two parameters, the transfer length is increased as the gate voltage increases. The transfer length increases its value from 3 µm to 20 µm as the gate voltage changes from -5 V to -20 V. As the higher concentration of charges is in the channel, the more current has to be transfer to the metal electrodes. Hence, the distance on the metal electrodes, used for transferring these charges, increases with an increase of the gate-to-source voltage.
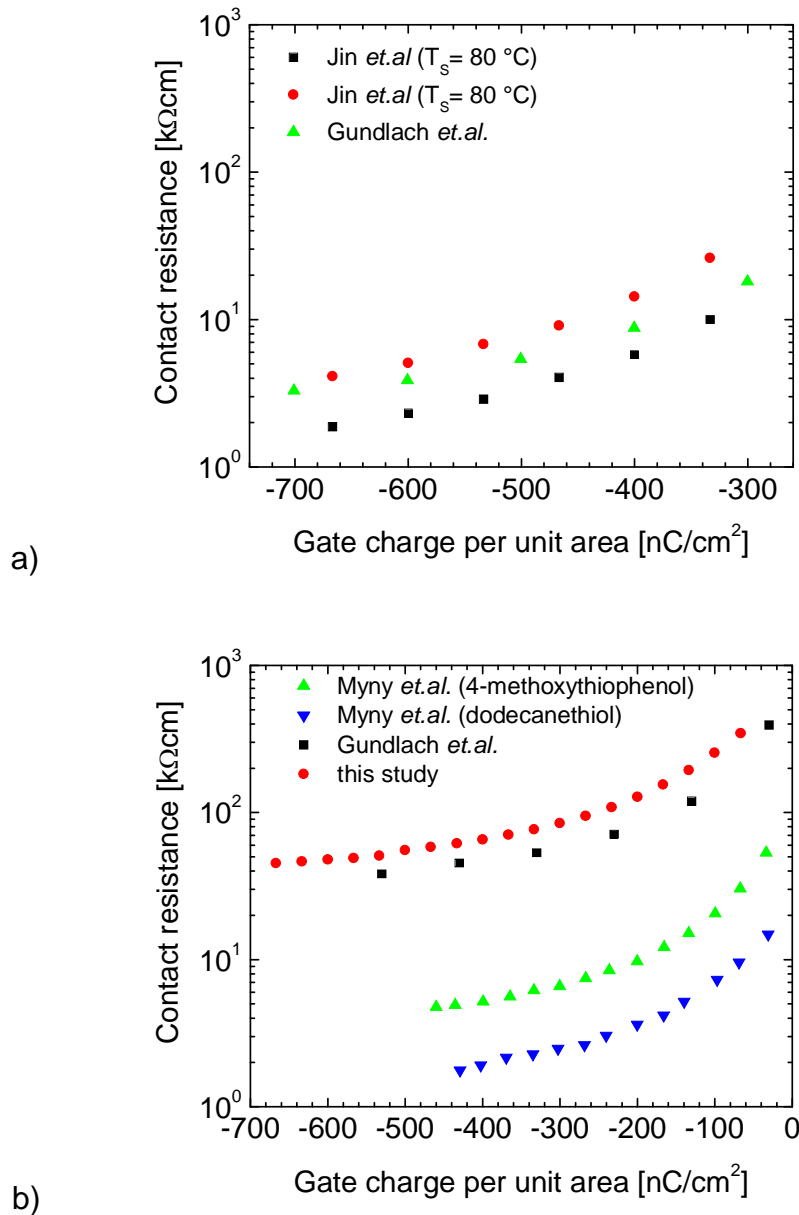
a)

b)

Fig. 9.5 Gate voltage dependent contact resistance of pentacene TFTs in a) the bottom-gate inverse staggered and b) the bottom-gate inverse coplanar configuration. Experimental data of Gundlach *et. al.*, Myny *et. al.* and Jin *et. al.* were taken from references [11], [13] and [14].

The gate voltage dependence of the measured contact resistance is shown in Fig. 9.5a and Fig. 9.5b for transistors with top and bottom drain/source contact configuration, respectively. The normalized contact resistance is plotted as a function of the gate charge per unit area (product of the gate voltage V_G and the gate capacitance C_G). This allows for a comparison of transistors with different transistor geometries. The marks in Fig. 9.5a and Fig. 9.5b represent the experimentally

determined normalized contact resistances. The lines are the fits of the experimental data. Our results are compared to experimental data measured and published by different research groups [11], [13] and [14]. The transistors in the inverse coplanar configuration, Fig. 9.5a, exhibit normalized contact resistances of approximately 50 kΩcm for high gate charges (gate voltages). Decreasing the charge on the gate leads to an increase of the normalized contact resistance. The transistors with top drain/source contacts exhibit normalized contact resistance of 5 kΩcm for high gate charges. The normalized contact resistance of TFTs in bottom drain/source contact configuration is shown in Fig. 9.5b. The contact resistance of the bottom contact transistors is approximately one order of magnitude higher than the contact resistance of transistors with top drain/source contacts. Drain/source contacts treated with thiol self-assembled monolayers exhibit a distinct drop of the contact resistance down to 3-5 kΩcm as it is shown for the experimental data of Myny *et. al.* in Fig. 9.5b. [13] For such devices the contact resistance is comparable to transistors with top drain/source contacts.

9.4 Contact resistance model of bottom gate staggered thin film transistors

The presented model for the contact resistance differs for different transistor configurations. First, the behavior of thin film transistors in the bottom gate top source/drain contacts configuration is explained. When the transistor operates in the linear regime, the sheet resistance in the contact area can be approximated by the sheet resistance of the transistor channel, which is given by:

$$R_{Sh-Top} = \frac{1}{\mu_0 \cdot C_G \cdot (V_G - V_T - V_D/2)}.$$
(Eq. 9.6)

Subsequently the following expression for the transfer length of a transistor with top drain/source contacts can be derived:

$$L_{T-Top} = \sqrt{\rho_c \mu_0 C_G (V_G - V_T - V_D/2)}.$$
(Eq. 9.7)

The sheet resistance is responsible for the change of the contact resistance as a function of the gate voltage. The experimental data determined by Jin *et. al.* and Gundlach *et. al.* in Fig. 9.5a was fitted by equation 9.5 [10], [11]. The measured data and the fits are shown in Fig. 9.6a. A good agreement of the experimental data and the fit is observed for the different transistor structures. A transfer length of 8.3 μm and an intrinsic charge carrier mobility, μ_0, of 0.80 $cm^2V^{-1}s^{-1}$ were determined for the experimental results obtained by Gundlach *et. al.* The specific contact resistance was determined to be 1.58 Ωcm^2. The two different samples by Jin *et. al.* were prepared at 20 °C and 80 °C substrate temperature, respectively. The pentacene transistor prepared at 20°C exhibits a device carrier mobility of 0.08 $cm^2V^{-1}s^{-1}$, whereas the film prepared at 80 °C shows a device carrier mobility of 0.25 $cm^2V^{-1}s^{-1}$. The specific contact resistance determined for both samples is identical, 2 Ωcm^2. The difference in the contact resistances between the two samples is caused by the different charge carrier mobilities in the transistor channel, which depends on the size of the pentacene crystals in the channel region of the transistor.
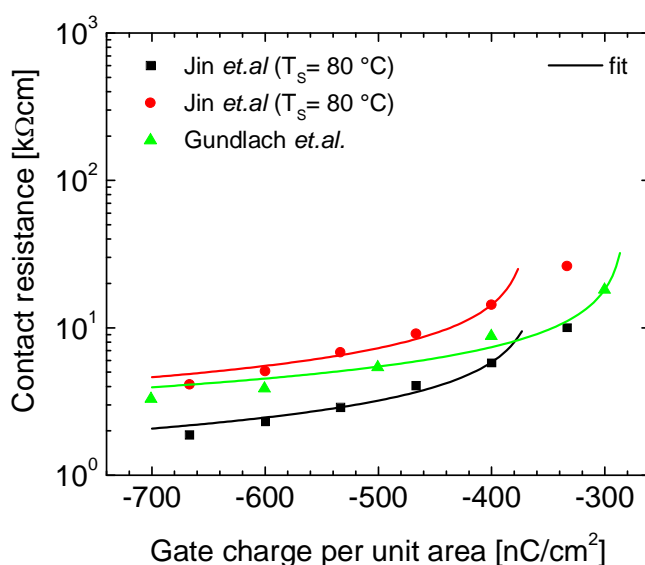

Fig. 9.6 The fit of experimental results with the model of the contact resistance of pentacene TFTs in the bottom-gate inverse staggered. Experimental data of Gundlach *et. al.* and Jin *et. al.* were taken from references [10] and [11].

In order to describe the influence of the transfer length and the specific contact resistance on the device carrier mobility, the expression of the contact resistance in the equation 9.2 can be substituted by equation 9.6. The new expression shows the gate voltage dependence of the device carrier mobility:

$$\mu_{eff} = \mu_0 \cdot \frac{L}{L + L_{0-Top}} \, .$$
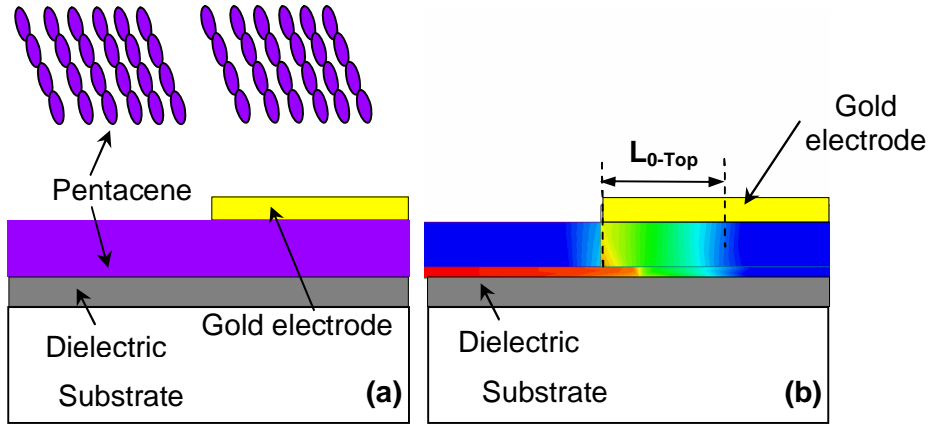
(Eq. 9.8)

Fig. 9.7 a) The schematic cross section of the transistor in the bottom gate top contact configuration with an illustration of the pentacene growth in the area between and under the electrodes. b) The electrostatic simulation of the current density distribution in the transistor channel.

L_{0-Top} represents an extension of the channel length caused by the contact resistance. In the case of top drain/source contacts L_{0-Top} is equal to the transfer length parameter given by equation 9.7. The spreading of the charges under the drain and source contact is qualitatively shown in Fig. 9.7b. The current density distributions in the transistor structures were modeled by using a simple electrostatic simulation tool. Only the conductivities of the individual regions were considered when modeling the current density distribution in the different regions of the device. The thin channel region of the transistor was described by a highly conductive sheet, whereas the rest of the pentacene layer was described by a distinctly lower conductivity. The model assumes that the growth of the pentacene molecules in the region between the metal electrodes and under the electrical contacts is the same, Fig. 9.7a. In the electrostatic simulations, the electrodes were treated as perfect conductors. The spreading of the charges under the drain/source contacts is clearly visible.

9.5 *Contact resistance model of bottom gate coplanar thin film transistors*

In the case of the transistor with the bottom drain/source electrical contacts it is often suggested that the mobile charges in the channel are injected from the edges of the drain and source electrodes. In the given experimental results, the drain and source gold electrodes have a thickness of 15 nm. A calculation of the contact resistances for such device geometry indicates that the contact resistance of transistors would be approximately 100 times larger than the measured one. Hence, majority of the mobile charges in the channel have to be injected from the top of the drain and source electrodes. Therefore, the equation 9.5 is used again to fit the experimental data in Fig. 9.5b and the results of the model fit are shown in Fig. 9.8.
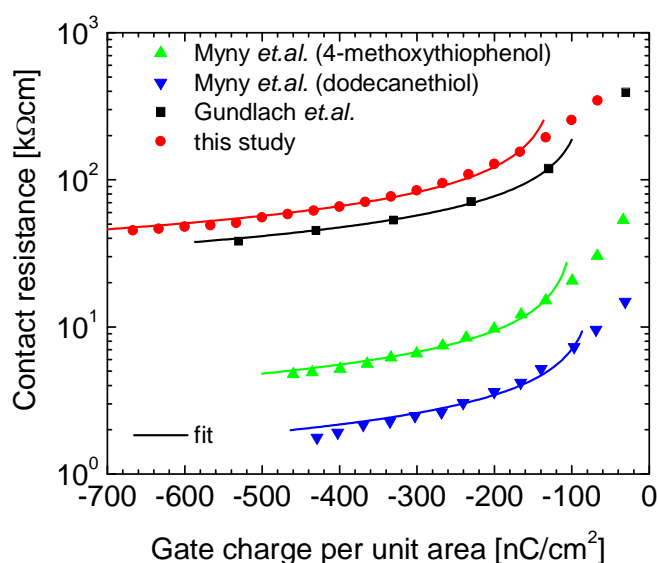

Fig. 9.8 Gate voltage dependent contact resistance of pentacene TFTs in the bottom-gate inverse coplanar configuration. Experimental data of Gundlach *et. al.* and Myny *et. al.* were taken from references [11] and [13].

Using the model of the contact resistance for devices prepared by our research group, the transfer length of 12 µm and the specific contact resistance of 410 Ωcm^2 were determined. However, extracting the transfer length and the specific contact resistance of transistors in the bottom drain/source configuration is more difficult than analyzing transistors in top drain/source contact configuration since the growth of the

pentacene molecules in the contact region of the bottom contact transistors is different from the growth of the molecules in the channel region.

The growth of pentacene molecules on a conductive surface leads to the formation of a disordered pentacene film, whereas the molecules grown on a dielectric surface (channel region) are highly ordered, Fig. 9.9c. Several studies have investigated the influence of the alignment of the pentacene molecules on the electronic structure of the pentacene film [15]-[16]. The difference in the energy alignment has a direct influence on the specific contact resistance, which can be described by thermionic emission. The specific contact resistance is proportional to

$$\rho_C \propto \exp\left(\frac{q\phi_B}{kT}\right)$$
(Eq. 9.9)

where k is the Boltzmann's constant, T the absolute temperature, q the elementary charge and Φ_B the barrier height. Treating the gold electrodes with a self assembled monolayer leads to a change of the work function by several hundreds of meV. However, the change of work function is not sufficient to explain the large change of the contact resistance. This observation is supported by investigations of Diao *et. al.* [17]. Diao and coworkers prepared pentacene-MSM (metal-semiconductor-metal) structures, which act as double Schottky barriers. Measurements of the current voltage characteristic show a very symmetric behavior indicating that the band alignment and the injection of charges in the organic semiconductor has to be symmetric even though the two metal/organic interfaces were prepared in opposite order.

Subsequently the specific contact resistance has to be similar for forward and reverse bias. A barrier height of 0.51 eV for gold-pentacene contacts is determined [17]. Therefore, the specific contact resistance in the top and the bottom drain/source transistor configurations was assumed to have similar values. Based on the fit of the contact resistance, the sheet resistance of the organic material in the contact region has been determined, which is 30-100 higher than the contact resistance of transistors with top drain and source contacts. The corresponding charge carrier mobility was 0.001 – 0.03 $cm^2V^{-1}s^{-1}$. This is consistent with measurements of thin film transistors with amorphous or disordered pentacene layers [7]. The treatment of gold electrodes with a self assembled monolayer (SAM) changes the growth conditions of

the pentacene film, so that the pentacene film on the electrical contacts is ordered as shown in Fig. 9.9f. The average size of the pentacene crystals and the lateral conductivity of the film in the contact region are increased. As a consequence, the charge carrier mobility in the contact area is increased and the contact resistance is reduced.
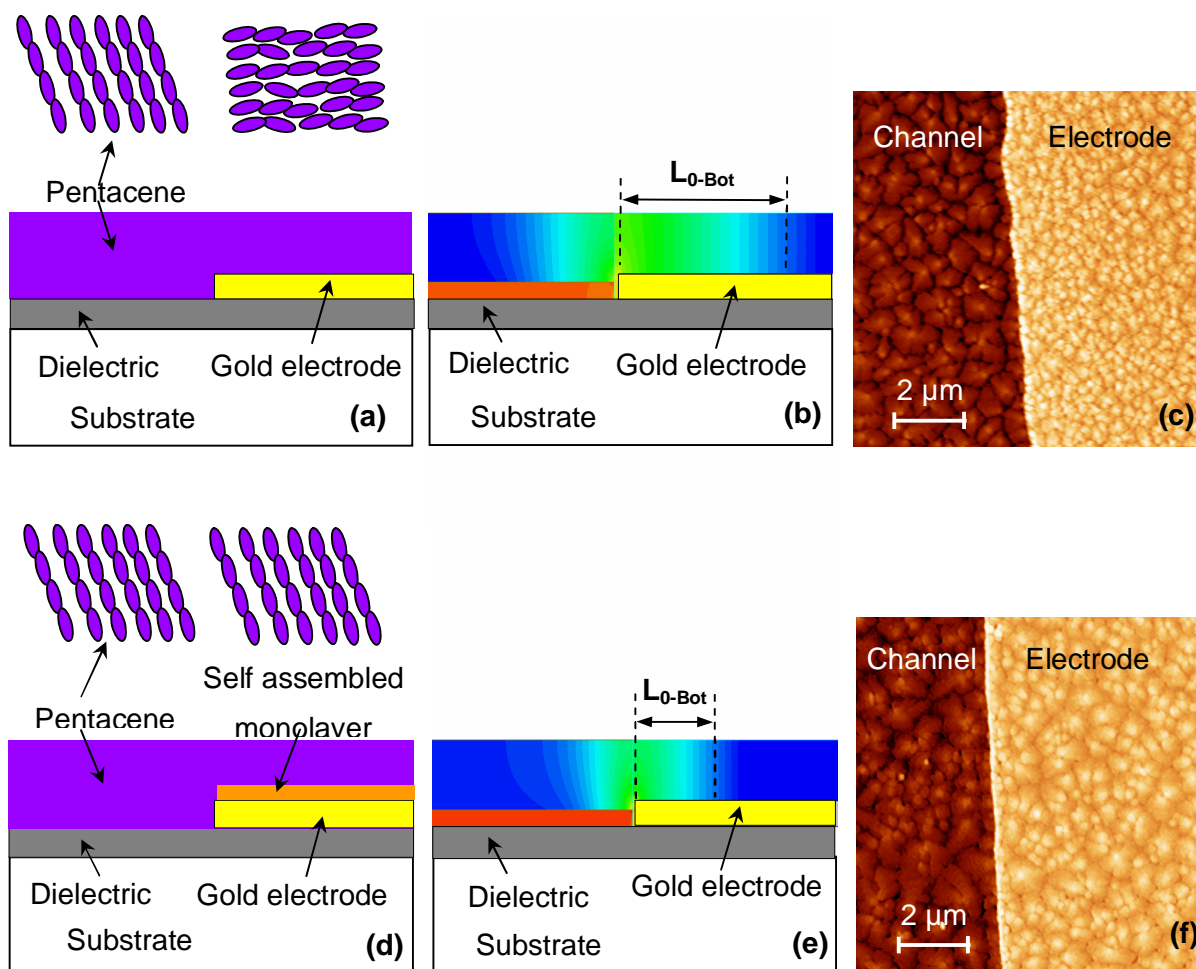

Fig. 9.9 Schematic cross sections of pentacene thin film transistors in the bottom contact configuration, illustrations of the current density distribution, and atomic force microscope images of pentacene films (a, b, c) prepared on a silicon dioxide substrate on pure gold drain/source electrodes and (d, e, f) on 2-Mercapto-5-nitrobenzimidazole (MNB) self-assembled monolayer (SAM) pretreated gold drain/source electrodes, respectively.

In the case of thin film transistors with bottom drain/source contacts the gate electric field is screened by the metal electrodes and the equation 9.6 has to be modified. The electric field in the region above the metal electrodes is controlled only by the drain voltage. Hence the distribution of charges is also controlled only with the

electric field coming from the applied drain-to-source voltage. Using the continuity equation, the distribution of electric charges in the region above the electrical contacts is given by:

$$p(x) = p_0 \exp\left(-\frac{x}{\mu \tau_p E}\right).$$

(Eq. 9.10)

Where p_0 is the concentration of charges at the edge of the electrical contact, E is the lateral electric field and τ is the lifetime constant of the electric charge. The equation 9.11 can be rewritten in different form by combining the expression for mobility from the Einstein's relation, $\mu = \frac{qD_p}{kT}$, and the identity for the average distance that the charge travels during the lifetime, $L_p = \sqrt{D_p \tau_p}$. The expression for the charge distribution in the contact region becomes:

$$p(x) = p_0 \exp\left(-\frac{kTx}{L_p^2 qE}\right).$$

(Eq. 9.11)

Knowing the concentration of charges, the sheet resistance of the semiconductor film in the region above the electrical contacts can be calculated as:

$$R_{Sh} = \frac{1}{t\sigma} = \frac{1}{qt(n\mu_n + p\mu_p)} \approx \frac{1}{qtp\mu_p},$$

(Eq. 9.12)

where t stands for the semiconductor film thickness. By substituting the expression for the concentration of charges, equation 9.12, in the equation 9.13, the sheet resistance becomes:

$$R_{Sh}(x) \approx \frac{1}{qt\mu_p p_0 \exp\left(-\frac{kTx}{qL_p^2 E}\right)}.$$

(Eq. 9.13)

The electric field in the contact region can be replaced with the ratio of the potential drop that occurs over the metal electrode, V_c, and the transfer length parameter, L_T, while the most of current is transferred to the metal within this distance.

$$E = \frac{V_c}{L_T}.$$

(Eq. 9.14)

The potential drop over the electrode, V_c, is calculated as the potential divider of the applied drain-to-source voltage. The mobility of semiconductor film is not unique along the whole semiconductor film. In the channel region, the charge carrier mobility of the thin film transistor takes values of μ_0. The mobility of semiconductor film differs when it comes to the contact region. Due to the different condition growth of the small molecules, the charge carrier mobility of pentacene films differs whether the pentacene molecules were deposited on silicon-dioxide or on gold electrode. Hence, the mobility of the pentacene film in the contact region has to be replaced by μ_c. Finally, the electric field becomes the function of the applied drain-to-source voltage, the channel length L, the transfer length parameter and the charge carrier mobility:

$$E = \frac{V_c}{L_T} = \frac{L_T/\mu_c}{L/\mu_0 + L_T/\mu_c} \cdot \frac{V_D}{L_T} = \frac{L_T \mu_0}{L\mu_C + L_T \mu_0} \cdot \frac{V_D}{L_T}.$$

(Eq. 9.15)

The concentration of charges at the point x=0, can be determined as the accumulated gate charge when the drain-to-source and the gate-to-source voltages are applied on the transistor, $qtp_0 = C_G\left(V_G - V_T - V_D/2\right)$. By integrating over the entire area used for the current transfer and normalizing the integral, the sheet resistance becomes:

$$R_{Sh} \approx \frac{1}{\mu_c C_G\left(V_G - V_T - V_D/2\right)} \exp\left(\frac{L_T^2}{L_p^2} \cdot \frac{kT/q}{V_D} \cdot \frac{L\mu_c + L_T \mu_0}{L_T \mu_0}\right).$$

(Eq. 9.16)

The drain current in the linear mode of transistor operation is:

$$I_D = \frac{W}{L} \mu_{eff} C_g\left(V_G - V_T - V_D/2\right)V_D,$$

(Eq. 9.17)

where the effective charge carrier mobility is defined as:

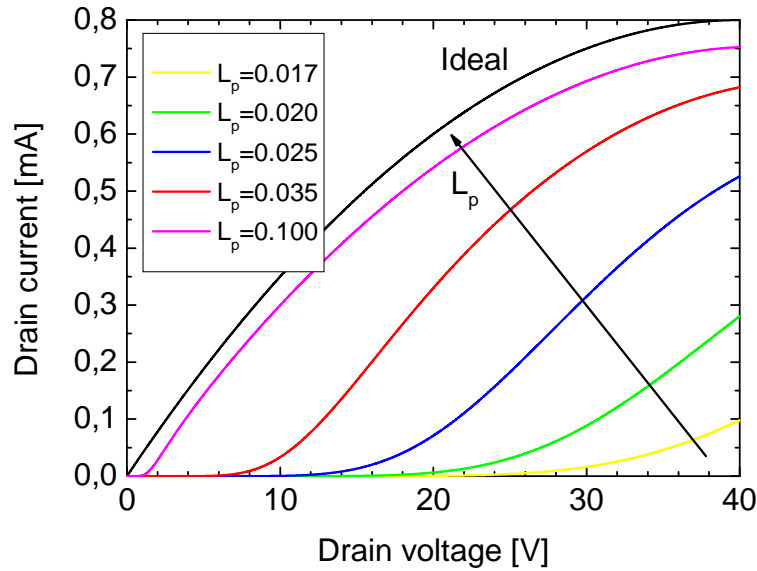$$\mu_{eff} = \frac{L}{L + r_c \mu_0 C_g (V_G - V_T)}.$$

(Eq. 9.18)

Fig. 9.10 The model of the output characteristic of a thin film transistor designed in the bottom gate bottom contact configuration. The model of the transistor assumes the channel width of 1000 μm, the channel length of 10 μm, the applied gate voltage of 40 V, the gate oxide capacitance of 10 nF/cm^2, the charge carrier mobility in the transistor channel of 1 cm^2/Vs, and the mobility in the contact region that is 10 times lower than the one in the channel region. The values of the L_p parameter are given in μm.

Substituting the normalized contact resistance, r_c, as $r_C = \sqrt{\rho_c R_{Sh}}$ where the sheet resistance is given by equation 9.16, the drain current can be modeled. Fig. 9.10 shows the behavior of the output transistor characteristic of a TFT device with the bottom gate coplanar configuration. The drain current is modeled according to the model presented here and for the different values of the L_p. For the high values of the L_p parameter, the output characteristic is becoming close to the ideal case of the drain current, the case of the staggered configuration. For lower values of the L_p parameter (below 0.1 μm), the current crowding effect takes place in the contact region. The crowding effect becomes visible for the small applied drain-to-source

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voltages. In the output characteristics of the transistor, one can see the curvature of the modeled characteristic. The nonlinear behavior of the contact resistance for the coplanar transistors is commonly observed, and it is well known as the 'S-shape' behavior.

The plot of the transfer length as the function of the applied drain-to-source voltage is shown in Fig. 9.11. In the case of the staggered transistor configuration, the transfer length takes the value independent on the applied drain-to-source voltage. In the case of the coplanar transistor configuration, the transfer length is strongly controlled by the lateral drain electric field. As the drain voltage is increased, the distance used for the transferring charges to the metal contact is also increased.
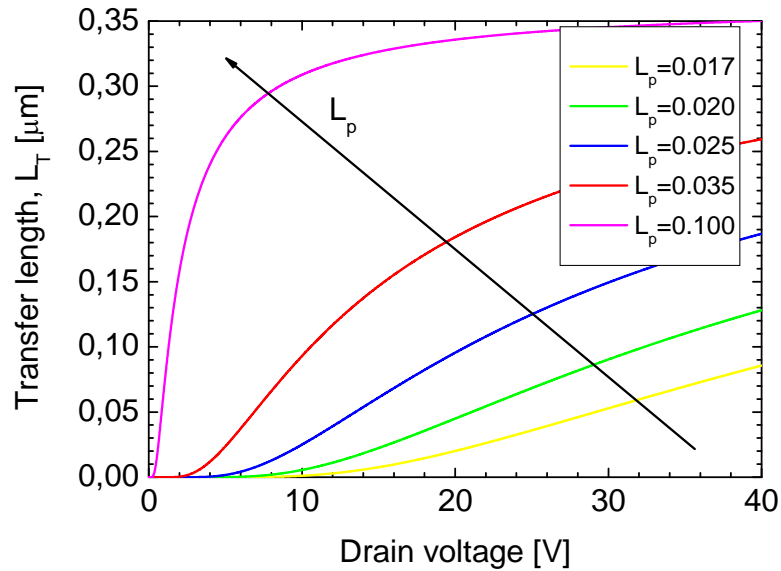

Fig. 9.11 The model of the transfer length parameter as the function of the applied drain-to-source voltage and the L_p parameter. The model assumes the same parameters as the one used in the model in Fig. 9.10.

The influence of the L_p parameter on the transfer length is shown in the Fig. 9.11. As the charge carrier mobility of the semiconductor film in the contact region is reduced, the average distance that the charge carrier passes during its lifetime (the L_p parameter) is reduced. Consequentially, the distance used for the current transfer from the semiconductor film to the electrical contact is also reduced. For SAM treated drain/source contacts the mobility in the contact region, μ_c, is approaching the mobility in the channel region, μ_0. In that case, the transfer length of such contacts is approaching to the transfer length of the top contact configuration, and the contact

resistance becomes lower. The contact resistance model is confirmed by electrostatic simulations of transistors without and with treated drain/source contacts, Fig. 9.9b and Fig. 9.9e respectively. The disordered pentacene film in the contact region is described by a low lateral conductivity which is proportional to μ_c. For the SAM treated contacts the lateral conductivity is assumed to be proportional to μ_0. With increasing lateral conductivity the extension length in bottom drain/source configuration drops and the contact resistance decreases.

9.6 Contact resistance model for charge carrier mobility

As the consequence of the contact resistance model, the effective charge carrier mobility of devices in top contact staggered configuration may be modeled as:

$$\mu_{eff-TC} = \mu_0 \cdot \frac{L}{L + L_T \coth\left(\dfrac{L_{DS}}{L_T}\right)} . \qquad \text{(Eq. 9.19)}$$

where L_{DS} stands for the width of the drain/source metal electrodes. In the experimental part of this chapter, the width of the metal electrodes was 10 µm. In the case of thin film transistors designed in bottom gate bottom contact configuration, the width of the drain/source electrodes do not play role in the contact resistance model. Hence, the effective charge carrier mobility for coplanar devices may be modeled as:

$$\mu_{eff-BC} = \mu_0 \cdot \frac{L}{L + L_T} . \qquad \text{(Eq. 9.20)}$$

Fig. 9.12 shows the dependence of the charge carrier mobility as a function of the transistor channel length, according to the presented model. The graph contains experimental data of the charge carrier mobility for devices in the top contact configuration, as well as the obtained results from the bottom contact devices.

In the case of the top contact configuration, experimental data are fitted with the equation 9.19, and values for the transfer length of 11,68 µm and the intrinsic charge carrier mobility of 0.686 cm^2/Vs are obtained. An increase of the charge carrier

mobility of top contact devices is possible with an increase of the width of the source/drain electrical contacts. If the electrodes would take an infinite width, the effective charge carrier mobility would reach its maximal values for the current value of the transfer length. In the case of device with 20 µm channel length, as the width of the metal electrodes would be increased from 10 µm to an infinite value, the charge carrier mobility would increase from 0.35 cm^2/Vs to 0.45 cm^2/Vs. Further increase in mobility would be possible with reduction of the specific contact resistance on metal-semiconductor interface.
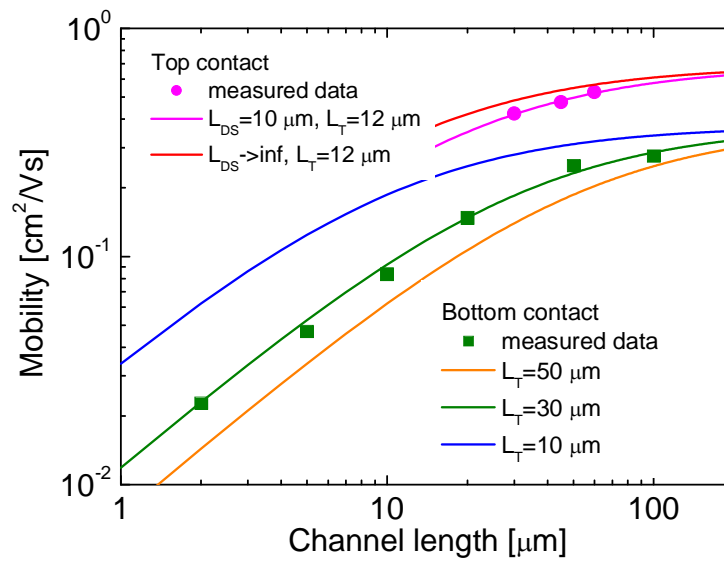
Fig. 9.12 Model of the charge carrier mobility of top contact and bottom contact thin film transistors.

In the case of bottom contact coplanar thin film transistors, the obtained data of charge carrier mobility of devices with different channel lengths are fitted with the equation 9.20. From the fit, the intrinsic charge carrier mobility of 0.373 cm^2/Vs and the transfer length of 30.48 µm are obtained. If TFT devices would perform with the higher contact resistance and therefore higher transfer length, the effective charge carrier mobility would be reduced. As the transfer length increases from 30 µm to 50 µm, devices with the channel length of 10 µm would exhibit reduction of the mobility from 0.09 cm^2/Vs to 0.06 cm^2/Vs. If the contact effects of metal-semiconductor interface would be improved, the devices with bottom gate bottom contact configuration would exhibit reduction in the transfer length parameter. The charge

carrier mobility of such devices would be increased, and devices with 10 µm channel length would exhibit an increase in mobility from 0.09 cm^2/Vs to 0.19 cm^2/Vs.

9.7 Summary

In this chapter, the model that describes the voltage dependent contact resistance of thin film transistors is presented. The model was used to investigate the contact behavior of pentacene thin film transistors with top and bottom drain/source contact configurations. Both types of transistors can be well described by the given model. The contact resistance of the transistors with top drain/source contact is approximately one order of magnitude lower than the contact resistance of bottom drain/source devices. The contact resistance of the bottom drain/source contact is higher due to the reduced lateral conductivity of the pentacene film in the contact area. The inverse coplanar thin film transistor with self-assembly treated gold electrodes showed a decrease in the contact resistance and a higher device carrier mobility.

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Conclusions

In this thesis the contact effects in thin film devices were studied. The focus of the research was in the first part on the contact effect in the chalcopyrite CuInSe thin film solar cells, while the second part of the thesis deals with the contact effects in the organic based thin film transistors.

The formation of the front electrical contacts in the thin film solar cells in the substrate configuration was analyzed. The front electrical contact on the solar cells were formed by screen printing metal silver paste which was followed with the thermal treatment of printed contacts. The thermal treatment of the screen printed electrodes may reduce the contact resistance of the front contact grid of a solar cell. It was shown that the surface roughness of the zinc oxide window layer of CIS solar cells is the main cause for high contact resistance of silver-zinc oxide interfaces. Although the surface roughness of a thin film solar cell is necessary in order to improve the light trapping mechanism of the solar cell, rough solar cells may exhibit higher contact resistance. For relatively rough surfaces of CIS solar cells (with the RMS roughness of ZnO window layer above 50 nm), thermal treatments of front electrical contacts printed with conventional silver paste did not lead to a reduction of front contact grid resistance. Using the silver nanoparticles, the contact resistance may be reduced, as well as the series resistance of a solar cell. Metal pastes with various average sizes of silver particles (from 5 nm to 1 µm) were analyzed as a candidate for satisfactory front electrical contacts of thin film solar cells. When using the pastes with lower average size of silver particles, the front contact grid resistance is reduced. The best performance was observed with the silver paste that contains silver nanoparticles with an average size of around 5 nm. The better surface coverage with the silver nanoparticles led to lower contact resistance.

Before entering the market, solar cells undergo several standard tests. Together with the efficiency of solar cells, other parameters of solar cells are studied, including front contact grid resistance. The screen printed electrical contacts have to satisfy several criteria before being used as front electrical contacts of solar cells. The accelerated aging test (the damp heat test) is the standard industrial test in order to test electrical devices for aging effects. The printed contacts were exposed to elevated temperature and humidity (85 °C and 85% RH) for 1000 hours. The increase in the contact resistance occurs after exposing samples to the new environment. The size of the silver particles in the paste is the crucial element in order to have low contact resistance on the thin film solar cells after a long operating time. The slowest increase of the specific contact resistance occurred for the nanoparticles silver paste. Reducing the size of silver particles in the metal paste the screen printed films become denser. Hence the screen printed silver nanoparticles films are better protected from the influence of the humidity on the aging of front electrical contacts of CIS solar cells. Furthermore, electrical contacts that are thermally treated over a longer time and at higher temperatures exhibit lower contact resistance due to the lower amount of organic residuals in printed films. However, longer thermal treatments and higher annealing temperatures lead to faster degradations of the active layer of CIS solar cells. Therefore, the formation process of front electrical contacts of CIS solar cells has to be optimized through the annealing parameters in order to avoid high contact resistance (at low process temperatures) and faster degradation of solar cell parameters (at high process temperatures).

In the second part of the thesis, contact effects in organic based thin film transistors were studied. Poly-3-hexylthiophene based thin film transistors were fabricated in the top-gate bottom-contact configuration with gold as source/drain metal electrodes. The contact resistance was determined with the conventional transmission line method, and it showed the gate voltage dependence as was expected. In addition to the TLM method, the novel method of determining contact resistance was presented. This method is based on mapping of potential along the transistor channel, and may be applicable for all transistor configurations. Through the buried sense fingers, contact resistances at the drain and the source electrodes were separately determined. Thin film transistors exhibited symmetrical ohmic contact behavior at both electrical contacts, showing that the injection and the extraction of charges

in/from the channel are occurring in the same manner. The contact resistance of P3HT-Au electrical contacts determined with the new method showed agreement with the results obtained in the conventional way. Electrical contacts were shown to be independent of changes of drain-to-source voltages, which is in agreement with the presented theory of staggered contact configuration.

Furthermore, the gate voltage dependant contact resistance is studied in thin film transistors based on small molecules. The contact resistance model of the thin film transistors with staggered and coplanar configurations was presented. The model was confirmed with the experimental results obtained by different research groups. The staggered transistor configurations exhibit lower contact resistance than the transistors in coplanar configuration. The reason for higher contact resistance in coplanar devices is the reduction of the lateral conductivity in the contact region. The gate electric field is in that case screened by the source/drain electrodes. The model shows that most of the current is not transferred over the side edges of the metal electrodes, but over the horizontal surface of electrodes. The contact resistance model is the first presented model that is able to explain the "S shape" curvature in output curves of the organic based thin film transistors.

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Хвала вам најдражи моји.

During all these years I was encouraged by my mother Dragana and sister Katarina, and all other family members were with me when support was needed. Your support is the most important to me, and this success is also your success. Thank you!

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