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Analysis and modelling of charge transport properties in organic field-effect transistors

by

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Abstract

Printed organic electronics for flexible, low-cost and large-area applications require solution-processable semiconductors with sufficiently high performance. Many of these soluble semiconductors are organic polymers. Charge transport mechanisms in these disordered systems differ from those in crystalline semiconductors, and various models exist for their description. In this work, top-gate organic field-effect transistors (OFETs) on flexible and transparent plastic foil substrates with solution-processed organic gate insulator are used to investigate on charge transport features in the widely used poly-thiophene P3HT (poly(3-hexyl thiophene)). In addition to standard transistor parameters such as charge carrier mobility and threshold voltage, the modeling takes into account features like bulk current and the charge carrier density dependence of the mobility. These parameters are analyzed upon their variation with temperature, semiconductor layer thickness or changes in the composure of the insulator and its solvent, in order to achieve a comprehensive description. In addition, a model is elaborated and experimentally verified that predicts, from the charge carrier mobility and the contact resistance as well as the parasitic capacitances, the maximum frequency of an OFET, a crucial parameter for any application. Having been realized in the frame of an industrial cooperation aiming for suitable materials for printed electronics, the thesis includes the implementation of a high-quality material test and analysis setup, with which different semiconductor/insulator systems are evaluated, also with respect to the parameters found to be crucial in the modeling section, with the goal of achieving not only high mobility for good on-current, but also suitable threshold voltage and bulk conductivity for low off-current.

Figure 1: Flexible and transparent plastic foil substrate with top-gate organic field-effect transistors.

1 Introduction

1.1 Organic electronics - the large perspective

Organic electronics has gone through a tremendous development in the last decades. The first conducting polymers were reported in 1977 by Alan J. Heeger, Alan MacDiarmid and Hideki Shirakawa [1], for which the discoverers were awarded the Nobel prize in chemistry in 2000 [2], and the first organic field-effect transistor (OFET) was built in 1986 [3]. It was known from the beginning that the low molecular interaction in such polymers and also in conductive organic oligomers, both soon referred to under the umbrella term "organic semiconductors", does not allow for the formation of delocalized energy bands as in crystalline inorganic semiconductors like gallium arsenide or silicon [4]. Therefore it was clear that organic semiconductors would never be able to replace modern silicon electronics, as the electrical performance would always remain lower by several orders of magnitude [5]. Nevertheless, in the following decades a whole new field of research, "organic electronics", involving physics, chemistry and electrical engineering, arose under the perspective of completely new electronic applications, where lower performance is sufficient and which are impossible to achieve with state-of-the-art silicon technology: While the latter requires ultra high vacuum [6] and high temperatures during the fabrication process [7], organic materials can be applied at room temperature and atmospheric conditions in wet-chemical processes such as spin-coating or dip-coating, stamping and printing [8]. Therefore, organic electronics open the field of low-cost electronics, large area electronics and electronics on low-weight, flexible and transparent materials such as plastic foil, paper or clothes [9].

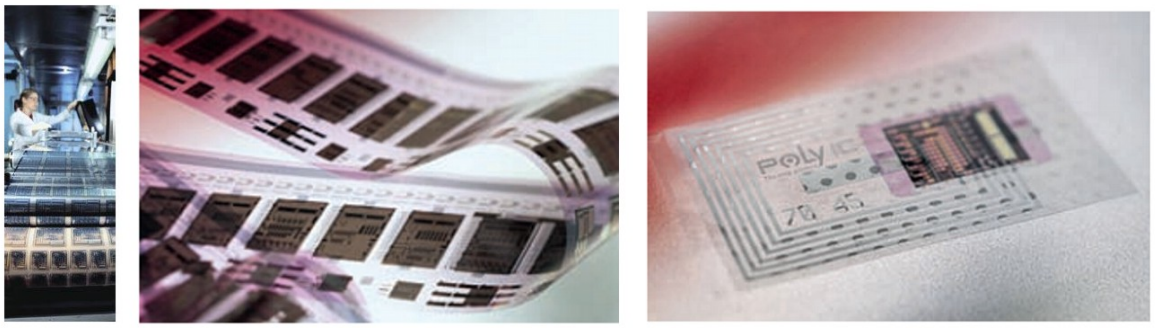

Figure 2: Printed radio frequency identification (RFID) tags (PolyIC).

During the first years, research focused mainly on the search for new materials which can drive higher currents, i.e. they have high charge carrier mobility μ, which became *the* key parameter in organic electronics research. At the same time, research of deposition techniques and surface treatment strongly enhanced the ordering of organic layers and thereby increased the mobility of existing materials [10]. With a large variety of high-performance materials known, three distinguished research fields emerged from the organic electronics field: research of organic light-emitting diodes (OLEDs), with the goal of achieving low-cost light sources that can be applied on large areas of basically any shape and produce natural light or any desired color at low energy consumption [11]. Applications range from whole-wall lighting that replaces today's point light sources with daylight-like illumination, to all kinds of decorative light elements and to flexible screens and displays with brilliant colors, which can be stored in very small space and produce perfect pictures in all environmental conditions from darkness to sunlight, with a large possible viewing angle. Second, organic photovoltaics (OPV), aiming at low-cost solar cells with reasonable efficiency which can be applied almost anywhere, e.g. included in house wall paintings or clothing, and can be produced with much less energy input than today's inorganic solar cells [12]. Third, organic field-effect transistors (OFETs) or more generally organic circuits, where the whole circuitry can be printed in large scale e.g. on plastic foil, for large-area, low-cost and flexible applications including electronic paper, radio frequency identification (RFID) tags, organic FET backplanes for above-mentioned flexible displays, organic memory, organic sensors [13] or smart textiles [14] [15].

1.2 From the first industrial products to a mass market

With a large variety of materials described for different purposes, charge carrier mobility having reached the mobility order of amorphous silicon and a lot of research done on device issues, organic electronics reached the threshold to first products and more and more industrial companies entered the field with the hope of becoming part of a new lucrative market. Today (December 2009) the Organic Electronics Association (oe-a) has 129 member companies from large chemical companies over production / printing equipment manufacturers to electronics companies. A market growth to 57 billion US-$ is expected for organic and printed electronics in the next ten years, until 2019, with a potential for a 300 billion US-$ market volume, which is the same as today's silicon electronics market [9]. Today many products have been demonstrated technically and have entered the market recently or will do so very soon, and are expected to be available in large volumes for the mass market in 2 to 4 years. Figure 3 shows already existing products: A rollable e-reader with OFET backplane, an OLED designer lamp and roll-to-roll printed flexible solar cells for mobile phone charging. More efficient and long-time stable solar cells, OLED lighting for more general use and

flexible OLED displays are expected in the upcoming years, and also printed RFID tags should be in general commercial use by 2011 [9]. However, a lot of research is still necessary to achieve materials and processes for e.g. higher circuit frequencies, larger efficiency and lifetime for OLEDs and solar cells and generally lower production costs.

Figure 3: Some of the first commercially available organic electronic products: E-reader with rollable electrophoretic display (Polymer Vision, left); OLED designer lamp (OSRAM Opto Semiconductors, middle); roll-to-roll production of organic photovoltaic modules (Konarka, right).

The work of this PhD thesis was also performed in the frame of an industrial research project. October 2007 saw the start of the MaDriX project, financed by the German Ministry of Education and Research (Bundesministerium für Bildung und Forschung, BMBF), under the leadership of PolyIC GmbH & Co. KG, a joint venture company by electronics producer Siemens AG and foil printing company KURZ Stiftung & Co. KG. In cooperation with the industrial partners BASF AG, Evonik Degussa GmbH, ELANTAS Beck GmbH and Siemens, the goal of the project is a new generation of printed electronics, with new materials - semiconductors and insulators - which combine high electrical performance with the requirements of the printing process (solubility in non-aggressive solvents, low temperature processing) and a quality testing process which allows for quality control within the printing process. In the project, each of the industry partners collaborate with partners from universities and research institutes. Our workgroup AG Wagner at Jacobs University Bremen is partner of PolyIC in two work packages: First, the elaboration of a standardized lab test for testing new semiconductor and insulator materials in a test environment so that new

materials can be tested at different places with reproducible and reliable results which offer good comparability to other tests. Second, the modeling of charge transport in those disordered organic materials, including verification of existing charge transport models and further development towards a consistent model of charge transport.

1.3 The search for optimized materials

The requirements for materials in printed electronics applications are multiple: From the technical point of view, the semiconductor has to be neither harmful to the environment nor hazardous for health, and it must be soluble in solvents that are non-explosive. From the performance point of view, high transistor on-currents and high switching frequencies are necessary as well as low off-currents. While on-current and switching frequency are proportional to the mobility, low off-currents require that the threshold voltage is close to zero or even negative (p-type semiconductors), and that the bulk current is low.

In addition to the semiconductor, the insulator plays a crucial role in the performance of an organic field-effect transistor. For high OFET performance, the demands to the insulator are manifold:

- Of course, it has to provide good insulation, i.e. very low leakage current, in order to prevent power loss and to assure a high production throughput with only very few transistors which have to be sorted out due to short circuits through the gate insulator.
- In order to achieve high transistor current at reasonable gate voltages, a high insulator capacitance is needed (see equation 2). With the insulator capacitance per unit area being
$$C_i = \frac{\epsilon \cdot \epsilon_0}{d} \tag{1}$$
a small insulator thickness d and / or a high dielectric constant ϵ are necessary.
- As in a top-gate setup, the insulator is deposited on top of the semiconductor, the insulator solvent must be complementary to the semiconductor, not destroying or deteriorating the semiconductor performance upon exposure to the insulator solvent.
- The conductive channel, where the charge transport takes place in an organic field-effect transistor, is located in the organic semiconductor, directly at the interface to the insulator. Therefore, the quality of this interface is of crucial importance for the OFET performance. Any interface roughness, stored charges,

ions, trap states at the interface or close by can dramatically reduce the performance by reducing the charge carrier mobility, shifting the threshold voltage or causing / increasing a parallel current that still persists even beyond the threshold voltage.

- In a top-gate setup, the insulator also serves as encapsulation for the insulator. Thus for semiconductors which are sensitive to oxygen and / or humidity, like P3HT, the insulator has to be impermeable to moisture and air.

Therefore, in order to have a high quality setup for the investigations on charge transport properties in this work, as well as for the test and comparison of semiconductor materials for the MaDriX project (see chapter 4.2), different insulator materials were tested with a variety of solvents.

In chapter 4, many different material systems are analyzed with respect to their performance in PET foil substrate transistors, including mobility and its dependence on gate voltage, the threshold voltage, bulk current and on-off ratio. As p-type semiconductors, different types of poly(3-hexylthiophene) (P3HT) were tested with different solvents. As more complex electronic circuits, with e.g. CMOS inverters as basic element, consist of p- and n-type field-effect transistors, electron-conducting organic semiconductors with similar performance to their p-type counterparts are necessary. A brief study of PDI8CN2 shows that wet-chemically processed high-performance n-type OFETs have been realized successfully in the frame of this work, with the same substrates as used with the p-type OFETs and with the same organic insulator, which demonstrates the feasibility of organic CMOS within the standard setup used. The investigated insulator materials were poly(methyl methacrylate) (PMMA) and polystyrene (PS) with a large variety of solvents for investigations on the complex and multiple interdependency with the semiconductor with respect to the transistor performance.

Chapter 4.2 will show that high charge carrier mobility alone does not necessarily make a good organic semiconductor, as high switching quality, expressed by high on/off ratio, does not only necessitate high on-current, but also low off-current. The latter requires a suitable threshold voltage and low bulk conductivity. As will be shown in chapter 4.3, all these parameters do not depend on the semiconductor and its solvent alone, but are crucially influenced by the choice of the insulator and the insulator solvent. In this respect, achieving good transistor performance with low off-current is not just a technical question of material tryout, but is strongly interconnected with fundamental physical questions. For example, the threshold voltage can be shifted by tuning the number of charge carriers in the channel as well as in the bulk via special interface treatment, as will be shown in detail in chapter 5.4.

1.4 Charge transport in disordered organic semiconductors - Models and open questions

While the establishment of a reliable material test, as well as the characterization of different organic semiconductor, insulator and solvent systems, forms part of this thesis the main focus of this work lies on the modeling of charge transport in these systems from experimental data, which is in many cases interwoven with the materials topic.

The widely used term "organic semiconductors" is quite misleading, as actually they do not have a lot in common with classic semiconductors and their concept of an electronic bandstructure with free, delocalized electrons (or holes) travelling in these extended bands, only hindered by lattice vibrations (phonons), whose number increases with higher temperature and makes charge carrier mobility lower with increasing temperature. The bands are either completely filled or completely empty and separated by energy gaps of several eV. This makes them intrinsically unconductive, and either charge carriers have to be excited thermally or with light into the empty bands to make them conductive, or dopants have to be brought into the material which provide additional levels in the gap. Hence the term *semi*-conductor.

The situation in organic "semiconductors" is very different. Molecules are only weakly bound to each other (mainly van der Waals forces), and no extended band structure can form. The charge carriers are localized to their sites and have to "hop" from site to site to enable charge transport. Unlike in the case of band transport, this "hopping" is aided by phonons, which causes mobility to increase with temperature. To describe these physical processes, at first existing models from amorphous inorganic semiconductors, like hydrogenated amorphous silicon (a-Si:H) were used and transferred to the organic systems. Also, most models which exist nowadays are based on such charge transport descriptions. Thus in the last decades, starting from different approaches, many models for charge transport in organic semiconductors were developed, resulting in different predictions of the charge carrier mobility. In the publications that present the models, all of them were checked on experimental data for the mobility variation with temperature, and were proven to hold true for the respective material system tested. In many models, the mobility was shown to depend not only on temperature, but on more parameters like electric field strength or charge carrier density, and related to this on parameters like ordering and the shape and width of the density of states.

However, almost all experimental studies focus on how "the mobility" changes with the variation of certain parameters, be it temperature, surface treatment, molecular weight and regio-regularity of the semiconductor, bias stress or many others. Other parameters like the shape of the transfer or output curves are completely neglected. This mobility is determined by a linear or quadratic fit to transfer curves, whose shape

is most often not linear or quadratic at all. Therefore the fitting region is drastically limited, generally to the highest drain and gate voltages used in the experiment. The mobility determined in this way is also the key parameter presented in most studies on new or modified material systems.

This focus on a single mobility value has two essential drawbacks: First, the comparison is very difficult. When the mobility is dependent on field strength and carrier density, mobilities determined using different drain and gate voltages with different insulator materials and thicknesses can not be compared with each other. Second, with this focus on a simple mobility value, no other information can be extracted from the measurements, not even a meaningful value of the threshold voltage. A lot of valuable physical information is not paid attention to, which is not contained in the simple mobility value, but in the way this value depends on e.g. carrier concentration, i.e. in the shape of the transfer curves, and then in the variation of this shape upon parameter variation. Therefore, in this thesis such parameters have always been included in the investigations on different materials or on parameter variations like temperature or semiconductor thickness, with the goal of achieving a more complete picture of the physical causes of the observed phenomena.

The thesis is arranged in the following structure: Chapter 2 gives a theoretical description of the principle of organic field-effect transistors, followed by an overview over existing models for charge transport in disordered organic semiconductors, and the most interesting of these models are presented in more detail. After a brief summary of the experimental conditions of sample preparation and electrical measurement, chapter 4 defines the standard test used for material characterization and presents a detailed study of various semiconductor and insulator systems, analyzing the various correlations of the materials and their impact on device characteristics. Chapter 5 features a detailed analysis on the dependence of electrical transistor characteristics on the active layer thickness, on temperature, as well as on semiconductor and insulator solvent, focussing on the charge carrier mobility as well as on features like carrier concentration dependence of the mobility, threshold voltage and the off-current that remains at gate voltages beyond the threshold. With the conclusions drawn from these studies, a more comprehensive picture of charge transport in the investigated material systems is attempted. Finally, in the concluding chapter 6 a model is elaborated and experimentally verified which predicts the maximum operation frequency of an OFET from its DC characteristics. It includes the transistor channel geometry and the charge carrier mobility extracted from DC transfer curves, as well as parasitic capacitances between the drain and source electrodes and the gate and the contact resistance determined via transfer line method from measurements of transistors with different channel lengths.

2 Charge Transport in Disordered Organic Semiconductors

2.1 General OFET theory

Field-effect transistors are among the most important switching devices in electronics and the most widely used element for building logic circuits. In contrast to a bipolar transistor, where a small current at one terminal, the basis, is used to control the current between two other terminals, called collector and emitter, the controlling element in a field-effect transistor is a voltage and the electric field resulting from it, hence the name. This is also the big advantage of the field-effect transistor over the bipolar transistor: As the current is just switched by an electric field and not by a current, the power loss upon switching with an FET is almost zero.

In a field-effect transistor, the current between two electrodes, called *source* (S) and *drain* (D), is controlled via the potential between a third electrode, the *gate* (G), and the source and the electric field resulting from it. The gate electrode is always electrically insulated from the transistor channel between drain and source. A common type of field-effect transistor is the MISFET (Metal-insulator-semiconductor FET). As the name indicates, in this type of FET the gate electrode (metal) is separated from the semiconductor by an insulator layer. As in many cases silicon oxide or another oxide is used to make this insulator layer, another frequent name for the MISFET is MOSFET (Metal-oxide-semiconductor FET) [16].

The working principle [17] of an organic field-effect transistor (OFET) is similar to that of a MISFET: the current between source and drain through the organic semiconductor is controlled by the voltage applied to the gate electrode, which is separated from the organic semiconductor by an insulator layer. In contrast to the inorganic MISFET, the OFET does not operate in inversion, but in accumulation regime. In an OFET with p-type semiconductor and negative threshold voltage, no current can flow between the source and the drain electrodes when there is no voltage applied to the gate. When a negative voltage is applied, at a certain point - the threshold voltage - enough charge carriers are accumulated to form a conducting channel close to the interface to the gate dielectric. By further increasing the electric field at the gate, more and more charge carriers are injected to the channel and the current between source and drain increases linearly with the gate voltage:

$$I = -\frac{W}{L} \cdot \mu \cdot C_i \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \tag{2}$$

In a p-type OFET with positive threshold voltage, even with no gate field applied, enough charge carriers are present to form a conducting channel, and a positive voltage has to be applied in order to deplete the OFET from mobile carriers and switch the transistor off.

In the *linear regime*, i.e. $|V_{DS}| \ll |V_{GS} - V_{th}|$, equation 2 can be approximated as

$$I = -\frac{W}{L} \cdot \mu \cdot C_i \left(V_{GS} - V_{th}\right) V_{DS}, \tag{3}$$

whereas in the *saturation regime*, at $|V_{DS}| > |V_{GS} - V_{th}|$, the current is not changed with further increase of V_{DS} and has a quadratic dependence on V_{GS}:

$$I = -\frac{W}{L} \cdot \mu \cdot C_i \left(V_{GS} - V_{th}\right)^2 \tag{4}$$

There are four possible geometries of an organic field-effect transistor as shown in figure 4: The source and drain electrodes can either be on the substrate and the semiconductor deposited onto them (bottom-contact configuration), or they are structured on top of the semiconductor (top-contact configuration). The same applies to the gate electrode, which is, in bottom-gate configuration, integrated in the substrate or deposited on it and the semiconductor is processed on the gate dielectric. In top-gate configuration, the gate insulator is applied on the semiconductor. The gate electrode is then deposited onto the dielectric as a last step.

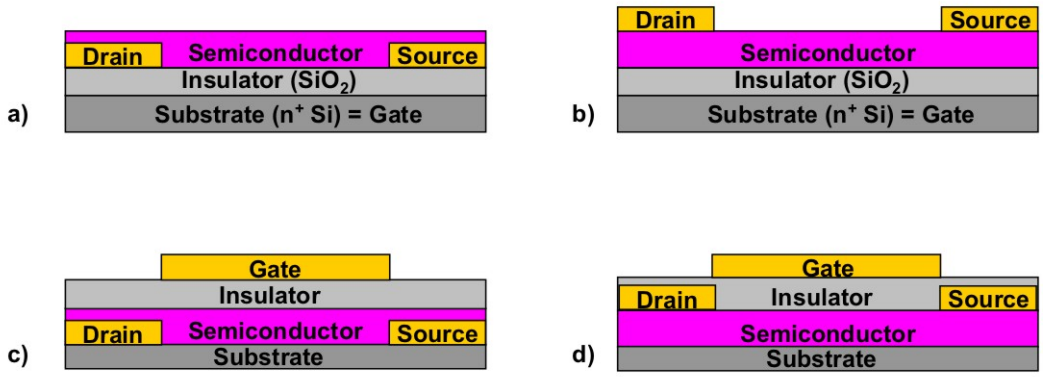

Figure 4: Sketches of organic field-effect transistors in a) bottom-gate and bottom-contact, b) bottom-gate and top-contact, c) top-gate and bottom-contact and d) top-gate and top-contact configuration. The bottom-gate picture shows the example of a silicon substrate, where the substrate also serves as gate electrode and the insulator is usually the silicon surface, which was thermally oxidized. Bottom-gate devices with patterned gate electrodes like those shown in the top-gate sketches are also possible.

Top-gate transistors bear the advantage that the gate insulator also serves as encapsulation for the semiconductor, whereas without additional encapsulation, in bottom-gate setup the semiconductor layer is exposed to air and moisture, which is detrimental to the performance of many organic semiconductors [18]. However, in top-gate configuration the gate dielectric has to be processed onto the semiconductor, which poses strong restrictions on the solvent that can be used for the insulator without harm to the semiconductor performance.

An equally ambiguous picture is valid for the question of top- or bottom contact setup [19]. While bottom-contacts hinder the regular growth of the semiconductor layer, the deposition of top-contacts onto the semiconductor may cause thermal stress and thereby decrease the device performance. An additional drawback of the bottom-gate, bottom-contact approach is that the contact area between the electrodes and the conducting channel close to the interface is very small, which may cause increased contact resistance. On the other hand, in top-contact, bottom-gate and in bottom-contact, top-gate configuration, the charge carriers have to cross an area of reduced charge carrier density on their way from the contacts to the conducting channel, which can also reduce the overall conductivity, especially in thick semiconductor films.

Bottom-gates and top-gates can either be common gates for several transistors on one substrate or patterned so that there is an individual gate electrode for each

transistor, preferably with no or little overlap with source and drain. While the first case is convenient in many cases, like in silicon substrates where the whole substrate directly serves as common gate electrode, the maximum frequency that can be achieved in AC applications is dramatically reduced, due to the additional capacitances between gate and drain / source. This will be presented in detail in chapter 6. Therefore, in any AC application, patterned gate electrodes with reduced overlap to the source and drain electrodes are highly preferable.

2.2 Principles of charge transport in organic semiconductors

Charge transport in organic semiconductors can not be described in the same way as charge transport in crystalline inorganic semiconductors such as silicon or germanium. The reason is that due to their low molecular interaction, they do not form regular three-dimensional crystal lattices like their inorganic counterparts. In those materials, the atoms are strongly coupled to one another, which leads to the formation of a crystalline lattice with long-range order. This causes the energy states of the single atoms to merge into delocalized energy bands. The empty conduction band is separated from the filled valence band by an energy gap. Any additional charge carrier which is e.g. thermally excited into the conduction band or coming from doping states close to the band is delocalized in the band and can move with a long mean free path (left part of figure 5). The mean free path is limited by scattering at crystal defects and at lattice vibrations (phonons). Phonons do not play a big role at small temperatures, so that the influence of the defects dominates in this regime. Scattering decreases with higher temperature, as the interaction with the charge carrier decreases due to their higher thermal velocity, and the mobility is proportional to $T^{3/2}$. The number of phonons, however, increases with increasing temperature. Thus at elevated temperatures, the conductivity of a crystalline semiconductor decreases again with increasing temperature, and the mobility is proportional to $T^{-3/2}$ [20].

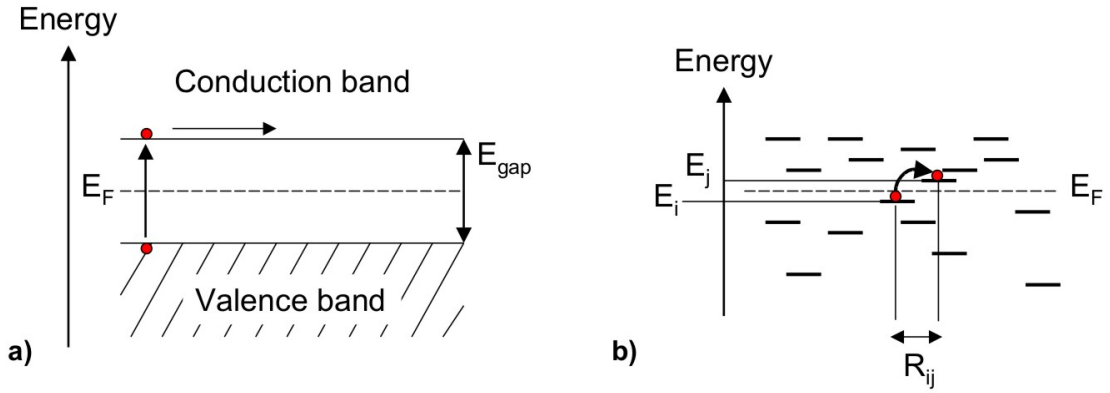

Figure 5: a) Sketch of charge transport in a crystalline semiconductor with broad, delocalized bands. Charge carriers which are thermally excited from the valence band (or from dopant levels) travel in the conduction band with a large free mean path. b) Sketch of hopping transport between the localized states in a disordered semiconductor system. Charge carriers tunnel from a state i with energy E_i to a state j with energy E_j over a distance of R_{ij}.

In organic semiconductors with less crystalline order such as conjugated polymers like P3HT, the situation is a completely different one. Because of the low crystallinity due to the small interaction between the molecules, which consists only of weak van der Waals forces, there are no extended bands and hence no delocalized charge transport [21]. In contrast, the charge carriers are located on localized states, and charge transport is only possible by "*hopping*" between those localized states, as depicted in the right part of figure 5, resulting in charge carrier mobilities which are orders of magnitude lower than those of crystalline semiconductors [22]. This "hopping" consists of tunneling between those localized states. This transport mechanism has long been known from amorphous hydrogenated silicon as well [23], which, unlike crystalline silicon, also has a distribution of localized energy states in the band gap. The charge carrier mobility is therefore orders of magnitude lower than in crystalline silicon, unless with a high gate voltage applied, the localized states are filled and the Fermi level gets closer and closer to the delocalized band.

In contrast to transport in crystalline semiconductors, the hopping transport is assisted by phonons and therefore the conductivity increases with increasing temperature. The hopping rate $\nu_{i\to j}$ from an occupied state i to an unoccupied state j depends on the distance R_{ij} between the sites and, if j is higher in energy than i, also on the energetic difference between the states. This energy difference is overcome more easily

at higher temperatures:

$$\nu_{i\to j} = \nu_0 \cdot exp\left(-2\alpha R_{ij}\right) \tag{5}$$

if $E_j < E_i$

$$\nu_{i\to j} = \nu_0 \cdot exp\left(-2\alpha R_{ij}\right) exp\left(-\frac{E_j - E_i}{k_B T}\right) \tag{6}$$

if $E_j > E_i$

with the attempt frequency ν_0, the inverse of the decay length of the localized wave functions α and the Boltzmann constant k_B. These formulations are often referred to as *Miller-Abrahams hopping rates*, as they were first presented by Allen Miller and Elihu Abrahams in a publication on hopping transport in silicon from 1960 [24].

With low doping levels, the average distance between two sites is very high, and therefore, only hops to the nearest neighbor are possible. This is called "fixed range hopping". In contrast, the "variable range hopping" model (VRH), developed by Mott [23] and Davis [25], presumes that with enough hopping states present, hopping over a large distance to a site at similar energy can be favored over a short distance jump with large energy difference, especially at low temperatures. So in VRH, hopping can take place either over a small distance with high activation energy or over a large distance with low activation energy. This holds true especially for a uniform density of states, as supposed by Mott. In this model, the charge carrier mobility increases with temperature according to the following relation:

$$\mu = \mu_0 \cdot exp\left[-\left(\frac{T_0}{T}\right)^{\frac{1}{4}}\right] \tag{7}$$

In disordered organic semiconductors however, the density of states is not uniform, but assumed to be exponential [26] or Gaussian [27]. In these cases, there are more states available at higher energies than at lower energy. So with increasing carrier density, it becomes easier to find an energetically close state in the near vicinity, and hops to the nearest neighbors become dominating again. The charge carrier mobility in the case of such a DOS does not depend on the temperature only, but also on the charge carrier concentration. Models which describe this situation are presented in chapters 2.3.3 to 2.3.6.

2.3 Literature models of charge transport in disordered systems

2.3.1 Multiple Trapping and Release

The multiple trapping and release or MTR model [28] is a model which combines transport in a (narrow) delocalized band with a large concentration of localized states. It has been applied to well-ordered organic semiconductor systems like vacuum-grown oligomers (e.g. oligothiophenes), which exhibit much better ordering than polymers, but are far from undisturbed delocalized band transport as in crystalline inorganic semiconductors like silicon.

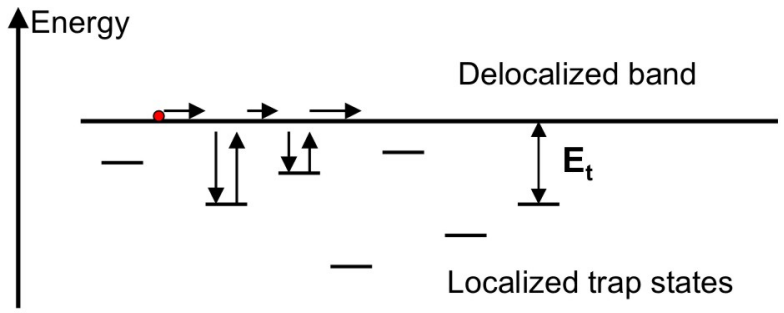

Figure 6: Sketch of the energy levels in the MTR model. Charge transport takes place in a delocalized band, but charge carriers are frequently trapped in states with depth E_t, from which they are thermally excited back into the band.

The model assumes that charge carriers can travel in a delocalized band, but with a large concentration of localized trap states below the band, as depicted in figure 6. Charge carriers which get into contact with such a trap state are immediately "trapped" in these states, which happens very frequently, due to the high trap state concentration. The release out of the trap and back into the band is thermally activated, so that the resulting charge carrier mobility increases with temperature:

$$\mu_{MTR} = \mu_0 \cdot a \cdot exp\left(-\frac{E_t}{k_B T}\right) \tag{8}$$

where μ_0 is the undisturbed mobility in the band and a the ratio between the density of states at the band edge and the trap state concentration. E_t is the "depth"

of the traps, the energy difference between the band edge and the trap levels. If these levels are not all equal in energy, but form a distribution as in figure 6, it signifies a kind of effective average trap level.

2.3.2 Dependence on Electric Field

In addition to the mobility dependence on temperature and charge carrier concentration, the charge carrier mobility was also found to depend on the electric field between source and drain. The explanation is the Poole-Frenkel mechanism [29]. Due to the applied electric field the Coulomb potential around the charged localized state is changed (see figure 7), and the tunnel rate between the different states is increased. The resulting charge carrier mobility is then discribed as

$$\mu(F) = \mu(0) \cdot exp\left(\frac{q}{k_B T}\beta\sqrt{F}\right) \tag{9}$$

with the electric field F, the mobility $\mu(0)$ with no electric field applied and the Poole-Frenkel factor $\beta = \sqrt{\frac{q}{\pi\epsilon}}$.

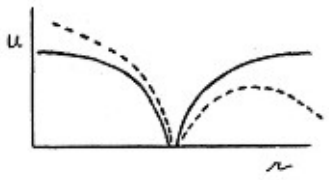

Figure 7: Potential energy as a function of the distance to a localized ion, without external field (full line) and with an external field applied (original drawing from [29]).

2.3.3 Vissenberg-Matters

The localized states, between which the hopping transport takes place, are often presumed to be described by a Gaussian density of states (DOS):

$$DOS_{Gauss}(E) = \frac{N_t}{2\pi\sigma_{DOS}} exp\left(-\frac{E^2}{2\sigma_{DOS}^2}\right) \tag{10}$$

with the total density of states N_t and the width of the Gaussian distribution σ_{DOS}. The Fermi level is generally somewhere in the tail of the distribution, where the DOS

increases with energy. Therefore, at higher energies, there are more energy states available than at lower energies. This means that additional charges to those already present in the system, as those induced by a gate voltage, which will occupy states at higher energies, need in average less energy to jump to neighboring sites, due to the higher density of states in their vicinity (see figure 8). This results in an increased charge carrier mobility. As a result, the charge carrier mobility is not constant, but increases with the charge carrier concentration, i.e. with the gate-source voltage.

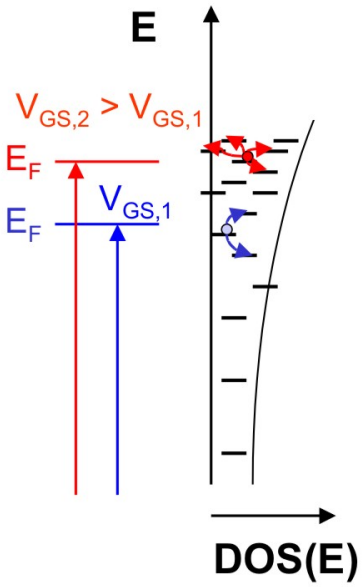

Figure 8: Reason for gate-voltage dependent mobility. With a higher gate voltage, more charges are accumulated, which occupy energy states that are higher in energy so that the Fermi energy is increased. Due to the shape of the density of states, at such higher energy there are more empty states available close to a carrier at the Fermi energy, which facilitates the hopping.

Based on this assumption, Vissenberg and Matters developed a model for charge transport in amorphous OFETs [26]. In this model, the tail states of above described Gaussian density of states are approximated by an exponential distribution:

$$DOS_{exp}(E) = \frac{N_t}{k_B T_0} exp\left(\frac{E}{k_B T_0}\right) \tag{11}$$

where T_0 indicates the width of the distribution, like σ in equation 10 ($\sigma = k_B T_0$).

The occupation of these states is governed by the Fermi-Dirac distribution f(E,E_F), so that the fraction δ of the states which is occupied follows as

$$\delta = \frac{1}{N_t} \int dEDOS(E) f(E, E_F) \tag{12}$$

To obtain the conductivity from these assumptions, the Vissenberg and Matters model uses percolation theory. In an energy landscape with different conductance between all the sites, the critical percolation conductance is then the minimal conductance between two sites in the network when the first infinite percolation cluster just forms. The critical average number of bonds per site so that this percolation criterion is just fulfilled is called B_c and is 2.8 in an amorphous three-dimensional system.

From these criteria, the conductivity of the system can be determined and is expressed as:

$$\sigma(\delta, T) = \sigma_0 \left(\frac{\delta N_t (T_0/T)^4 sin\left(\pi \frac{T}{T_0}\right)}{(2a)^3 B_c} \right)^{T_0/T} \tag{13}$$

and the non-linear dependence on the charge carrier density can well be seen:

$$\sigma \propto \delta^{T_0/T} \tag{14}$$

in contrast to gradual channel approximation, where the conductivity is just proportional to the carrier density. The charge carrier mobility $\mu = \sigma/(\delta \cdot \mathrm{e})$ in a field-effect transistor is therefore not constant, but has the following expression:

$$\mu = \frac{\sigma_0}{e} \left(\frac{(T_0/T)^4 sin\left(\pi \frac{T}{T_0}\right)}{(2a)^3 B_c} \right)^{T_0/T} \cdot \left(\frac{(C_i(V_{GS} - V_{th}))^2}{2 k_B T_0 \epsilon} \right)^{\frac{T_0}{T}-1} \tag{15}$$

with ϵ the dielectric constant of the gate insulator and C_i the insulator capacitance per unit area. For a given temperature, transistor characteristics can then be fitted with a gate-voltage dependent mobility which simply reads as follows [30]:

$$\mu = \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{aa}} \right)^{\gamma} \tag{16}$$

with the exponent

$$\gamma = 2\left(\frac{T_0}{T} - 1\right) \tag{17}$$

which expresses the dependence of the mobility on the gate voltage and which is directly related to the width of the density of states, T_0.

2.3.4 Limketkai

The Vissenberg-Matters model presented in the previous section gives a description of the hopping transport in dependence on temperature and charge carrier concentration, adjusted by the gate field. However, the model implies no electric field dependence of the charge carrier mobility as shown in chapter 2.3.2. In order to combine these two approaches, Limketkai et al. presented a model which is an extension of the Vissenberg-Matters model by an electric field dependence [31].

In Limketkai's approach, the energy the charge carrier is provided with by the electric field is added to its thermal energy. Thus the thermal energy kT the carrier possesses and which enables it to overcome the energetic difference to the next hopping site is enlarged by an energy kT_F defined as follows:

$$kT_F = \frac{qF}{2\alpha} \tag{18}$$

with the electric field F and α as the inverse of the localization length, as in equation 5.

The charge carriers have then an "effective temperature"

$$T_{eff} \leq T + T_F \tag{19}$$

At sufficiently small electric fields or high temperatures ($T_F < T$), where the influence of the electric field can be regarded as small perturbation, the two terms can simply be added:

$$T_{eff} \approx T + T_F \tag{20}$$

This is valid for a quite big range of temperatures and electric fields. For example, at a temperature as low as 100 K, it holds true for electric fields as high as $10^6\ \frac{V}{cm}$.

With this adjustment of the thermal energy, the charge carrier mobility then becomes:

$$\mu = \frac{\sigma_0}{q}\left(\frac{16\pi}{B_c}\frac{T_0^3}{(2\alpha)^3}\frac{T+T_F}{(2T+T_F)^2(2T+3T_F)^2}\right)^{\frac{T_0}{T+T_F}} \cdot n(x)^{\frac{T_0}{T+T_F}-1} \tag{21}$$

with the charge carrier density n:

$$n = \frac{C_i^2\,(V_{GS}-Vth)^2}{2k_BT_0\epsilon} \tag{22}$$

Limketkai et al. fitted experimental data from Brütting et al. [32] with this model, but only obtained accordance with the fit at high electric field. Good agreement between data and fit could be achieved, however, by presuming a voltage offset of 2 V. This was explained by a 2 V voltage drop at the contacts due to contact effects.

2.3.5 Bässler and related models

A model for charge transport in disordered organic systems, presented by Bässler et al. already in 1993 [33], is based on a Gaussian-shaped density of hopping states as shown in equation 10, and therefore also referred to as *Gaussian Disorder Model* (GDM). Hopping between those sites takes place according to the Miller-Abrahams formalism shown in equation 5 and 6. As the charge transport in this model can not be calculated analytically, Bässler et al. used Monte-Carlo simulations to calculate the conductivity in the organic semiconductor. The model also takes into account the fact that hopping is facilitated in the direction of the electric field due to the lowering of the Coulomb potential as described above in section 2.3.2 of this chapter. The resulting field- and temperature-dependent charge carrier mobility in this model is then:

$$\mu_{GDM} = \mu_\infty \cdot exp\left[-\left(\frac{2\sigma}{3k_BT}\right)^2\right] \cdot exp\left[C\left(\left(\frac{\sigma}{k_BT}\right)^2 - \Sigma^2\right)\sqrt{F}\right] \tag{23}$$

with μ_∞ the mobility in the high temperature limit, C a constant that depends on site spacing, and Σ the degree of positional disorder (in the case of $\Sigma < 1.5$, Σ^2 is replaced by 2.5). Interesting to note is the $exp\left(-\left(\frac{1}{T}\right)^2\right)$ temperature dependence of the mobility.

A big disadvantage of this model is that it is only valid for very high fields larger than $10^6\ \frac{V}{cm}$. Therefore the model was improved into what is called the *Correlated*

Disorder Model (CDM) [34]. In this model, the energies of the different sites are correlated, and this over a much larger length than the hopping distances, due to long-range charge-dipole interactions in the material. In this model the empirical expression of the mobility in organic materials is:

$$\mu_{CDM} = \mu_\infty \cdot exp\left[-\left(\frac{3\sigma}{5k_BT}\right)^2\right] \cdot exp\left[C_0\left(\left(\frac{\sigma}{k_BT}\right)^{3/2} - 2\right)\sqrt{\frac{eaF}{\sigma}}\right] \tag{24}$$

with the intersite separation a, and C_0 is 0.78. The main difference to the Gaussian Disorder Model is the temperature dependence of the field dependence. The CDM has been used to describe hole mobility more successfully than the GDM [35].

Up to now, all models presented neglect the effect of polarons. A polaron is a quasi-particle which is produced by an electric charge and the deformation of the surrounding lattice that this charge induces via electric forces. In polythiophenes for example, an additional charge in a polymer chain creates a geometrical change in its chain structure, accompanied by a change in the chemical structure, showing itself as a reversal of the single- / double-bond alternation over five thiophene rings and the creation of two localized polaron states [36]. Bässler et al. include polarons in their model by giving an estimation on how large their effect on the observed transport phenomena should be. In their consideration, the total activation energy for the charge transport is the sum of a disorder and a polaron contribution. So there is no clear border between hopping and polaron transport models, but the question is just, which of the two contributions are more important. The conclusion of their examination is that polarons with a typical binding energy of meV do not have an effect that can be distinguished in the transport analysis. Hence the hopping transport in the disorder model is considered as a sufficient description of charge transport [33].

2.3.6 Coehoorn

In a review published by Reinder Coehoorn et al. [37], the authors analyze and compare a number of models on hopping transport in disordered systems. In addition to the Vissenberg-Matters model [26], these models are the Movaghar-Schirmacher model [38], the Arkhipov model [39], the Martens model [40], and the Roichman-Tessler model [41]. All models are either made for a Gaussian-shaped density of states, or, in case they were developed for a different DOS, like the Vissenberg-Matters model, they were modified by the authors in order to be applied to a Gaussian DOS. The authors demonstrate that all of these models lead to similar dependences of the charge carrier mobility on temperature and charge carrier concentration, at least over the biggest

part of the parameter range. Only at very high charge carrier concentration are there major deviations, when the question, if a state where a carrier can potentially hop to, is occupied or not starts to play a major role.

Based on this similarity of the different models, Coehoorn et al. propose the following unified description of the charge carrier mobility:

$$\mu \cong \frac{e\nu_0}{N_t^{2/3} k_B T} \Phi \cdot exp\left[-p_0 - lnc - \left(a - \frac{E_F}{\sigma_{DOS}}\right)\frac{\sigma_{DOS}}{k_B T} + \frac{d}{p_0}\left(\frac{\sigma_{DOS}}{k_B T}\right)^2\right] \tag{25}$$

where Φ is a function that may slightly depend on temperature and carrier concentration, p_0 is function of the site density, c is the charge carrier concentration expressed as the ratio between occupied and totally available sites, and a and d are numerical constants. In addition to the direct mobility dependence on c, the Fermi energy, too, is a function of the charge carrier concentration and the temperature. At sufficiently high charge carrier concentration, the $1/T$ term dominates over the $1/T^2$ term, so that the mobility increase with temperature goes as $exp(-1/T)$. However, a $exp(-1/T^2)$ dependence as predicted by the Gaussian Disorder Model from Bässler et al. can be found, but only within the limit of very low carrier concentration.

2.3.7 Numerical Master Equation Approach

In contrast to these analytical models, Pasveer et al. [42] calculated the mobility numerically as solution of the *master equation*

$$\sum_{j \neq i} \left[W_{ij} p_i \left(1 - p_j\right) - W_{ji} p_j \left(1 - p_i\right)\right] = 0 \tag{26}$$

where W_{ij} is the transition rate for hopping from site i to j and p_i is the occupation probability of site i. For the calculation, the Miller-Abrahams equations 5 and 6 are considered as the transition rates for hopping in a regular cubic lattice with lattice constant a. The energy states are presumed to be disordered within a Gaussian density of states. The charge carrier mobility is then found to be described by a carrier density independent prefactor which depends on the electric field and a field-independent term:

$$\mu(T, p, E) \approx f(T, E) \cdot \mu(T, p) \tag{27}$$

The prefactor can be written as

$$f(T,E) = exp\left[0.44\left(\left(\frac{\sigma}{k_BT}\right)^{\frac{3}{2}} - 2.2\right)\left(\sqrt{1+0.8\left(\frac{Eea}{\sigma}\right)^2} - 1\right)\right] \tag{28}$$

and $\mu(T,p)$ as

$$\mu(T,p) = \mu_0(T)exp\left[\frac{1}{2}\left(\left(\frac{\sigma}{k_BT}\right)^2 - \frac{\sigma}{k_BT}\right)(2pa^3)^\delta\right] \tag{29}$$

with

$$\delta = 2\frac{ln\left(\left(\frac{\sigma}{k_BT}\right)^2 - \frac{\sigma}{k_BT}\right) - ln(ln4)}{\left(\frac{\sigma}{k_BT}\right)^2} \tag{30}$$

and

$$\mu_0(T) = \mu_0 \cdot c_1 \cdot exp\left[-c_2\left(\frac{\sigma}{k_BT}\right)^2\right] \tag{31}$$

$$\mu_0 = \frac{a^2\nu_0 e}{\sigma} \tag{32}$$

$$c_1 = 1.8 \cdot 10^{-9} \tag{33}$$

$$c_2 = 0.42 \tag{34}$$

The result is that in most cases the charge carrier mobility can be described very well without consideration of the dependence on the electric field, which only leads to a considerable deviation in the limit of very high fields at low temperature. For vanishing charge carrier density, the model yields the $exp(-1/T^2)$ dependence of the Bässler model. From the fact that the numerical solution obtained agrees well with measurements on organic LEDs, the authors conclude that the Miller-Abrahams hopping rates are a good description and that an uncorrelated Gaussian Disorder Model is sufficient and a Correlated Disorder Model as described in section 2.3.5 is not necessary.

3 Experimental

3.1 Preparation of samples

Except for the few samples which were prepared on silicon substrates for special purposes, all transistors used in this work were fabricated on flexible and transparent plastic foils, thus very closely to applications in printable electronics. The foil used was polyethylene terephthalate (PET, see figure 9) foil (exact specifications given in [43]). A bottom-contact and top-gate setup (see figure 10) was used, where the source and drain electrodes were structured on the plastic substrates by means of optical lithography. The organic semiconductor was deposited by spin-coating from solution, followed by an organic insulator, which thus encapsulates the semiconductor, protecting it from degradation through contact with air and humidity. The last step in the preparation was the deposition of the gate electrode .

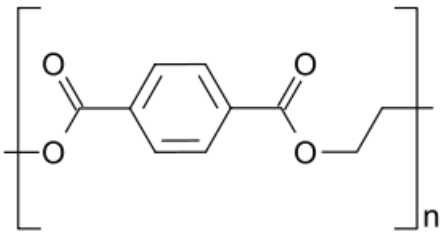

Figure 9: Structural formula of polyethylene terephthalate (PET).

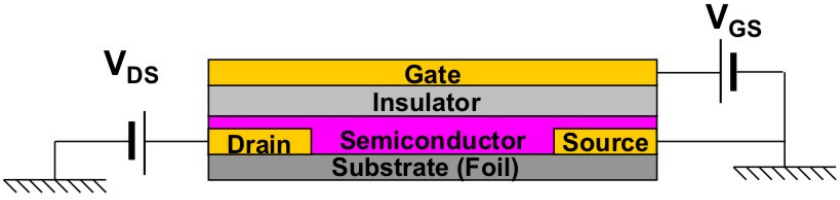

Figure 10: Scheme of an organic field-effect transistor in bottom-contact and top-gate structure, as used in this work.

One standard *MaDriX / StaLa* sample contains in total 87 transistors. 48 of them have the same channel geometry with channel length L of 10 μm and a W/L ratio of 1000 (abbreviation *K10*) and can be used for statistical analysis. The remaining transistors vary in channel length and width and are designed for the determination of contact resistance with the transfer line method (TLM). All source, drain and gate electrodes have prolongations for contacting them in plugs as described in the following section 3.2. The complete sample design with all details is available in [43].

3.1.1 Optical Lithography

The source and drain electrodes were patterned on the PET substrates by means of optical lithography, either in our cleanroom or by *PolyIC* and later by the *Fraunhofer-Institut für Physikalische Messtechnik IPM*, Freiburg (Breisgau), in the framework of the *MaDriX* project. For one sample, a piece of PET foil was cut out and, for enhanced stability during the entire preparation process, fixed on a microscope glass slide of the same size by the help of an adhesion foil. The foil was thoroughly cleaned by rinsing it abundantly with acetone and wiping it with an acetone-soaked, very soft cleanroom towel.

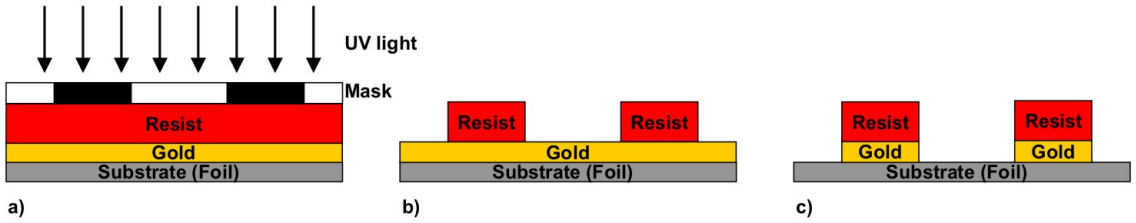

Figure 11: Optical lithography involving an etching process. a) The whole substrate is covered with gold and a photo resist, which is selectively exposed to UV light. b) The exposed parts of the resist are removed in the developer. c) The gold is etched away except of the parts which are covered by the remaining resist. For more details, see text.

In a sputter-coater, the foil was then covered with a 30-35 nm thick gold layer. Afterwards, the gold was covered with a photo resist by spin-coating at 4000 rounds per minute (rpm), followed by a one-minute bake-out at 100°C. The photo resist was exposed to UV light during 2.3 seconds in a Suss mask aligner through a glass mask which is dark in all places where the gold is to remain on the sample, and transparent

in all other places (figure 11a). All parts of the photoresist that were exposed to the UV light are then dissolved in a 25 s bath in the developer, a weak base. The sample is then washed in water and dried in nitrogen flow. After this procedure, the gold layer is covered by the remaining resist at the electrode positions, whereas all the rest of the gold is uncovered (figure 11b). Those parts are therefore etched away upon soaking the sample in an etchant during one minute (figure 11c). After washing the sample again in water and drying it in nitrogen flow, the optical lithography is finished.

3.1.2 Spin-coating of semiconductor and insulator

Before the deposition of the semiconductor, the sample was cleaned in order to remove the remaining resist on top of the electrodes and all other impurities, by the same procedure as described above in chapter 3.1.1. Solution and spin-coating parameters for the preparation of standard *MaDriX* samples with 30-35 nm thick P3HT layer and an insulator thickness of 350 nm are given in [43]. For other purposes different materials, concentrations, times and speeds were chosen.

As even very small particles on the samples can cause increased leakage and even short circuits in the insulator, extreme care was taken of clean working and short waiting times during the entire spin-coating process. To avoid particles coming from the solutions themselves, they were filtered through a 450 nm particle filter directly before the procedure.

After the deposition of the insulator, a 100 nm thick gate electrode was deposited through a shadow mask in the sputter-coater.

3.2 Electrical Measurement in the StaLa Measurement Setup

After the preparation of the transistor samples, they were stored in darkness for at least eight hours before the electrical measurements took place in the StaLa measurement setup, which was designed and built at the beginning of the MaDriX project by the Wagner group at Jacobs University Bremen for the comfortable and reliable characterisation of a big number of transistors on plastic substrates. For the measurements, the transistor blocks were cut out of the substrate and plugged into small plug-boards as shown in the upper left of figure 12. For the measurement, these plugs were inserted into the drawer-boards shown in the lower left, which were then covered to avoid any light influence during the measurement. The whole StaLa machine contains three drawers with two boards each, so that, with each board containing four plug-board sockets, 24 sample blocks with a maximum of 144 transistors can be measured at a time. The transistor is selected via a *Keithley 3706* switchboard. Gate and Drain voltages are

applied and the currents measured with a *Keithley 2612* dual sourcemeter. The *StaLa* software allows to create an individual measurement menu including basic contact and leakage checks, on/off measurements, transfer and output characteristics, hysteresis loops, and long-time measurements with constant voltages applied. Every menu point can be executed for either all transistors available, for individually selected ones or for automatically selected transistors according to current limits and / or average on/off ratio values. All measurement data are stored in ASCII tables as well as in Microsoft Excel files.

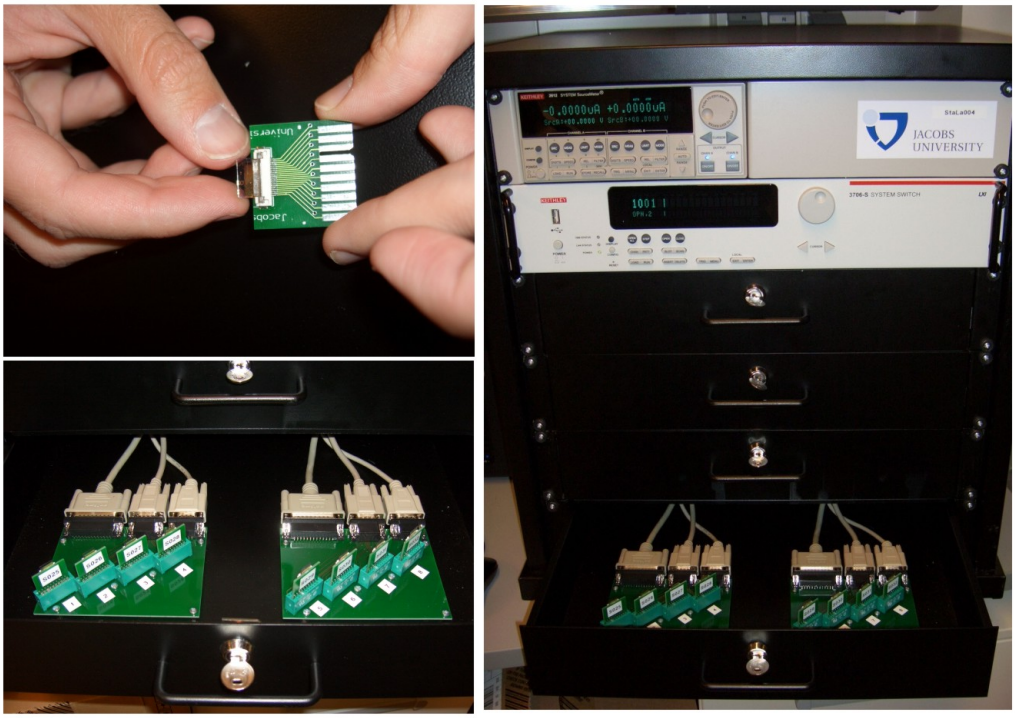

Figure 12: The StaLa measurement setup. The right part shows the whole setup with the *Keithley 2612* dual sourcemeter in the top left, the *Keithley 3706* switchboard below, followed by an empty drawer for storing and three drawers like the one opened, each containing two drawer-boards with four sockets each, as shown in the lower left part of the picture. The cut sample blocks are plugged into plug-boards like those shown in the upper left, which are plugged into the drawer-boards.

4 Material Screening and Optimization

4.1 Establishment of a standardized material test

In order to qualify different materials, such as semiconductors, semiconductor solvents, insulators and insulator solvents, a standardized test was established also designed for the characterization of potential new materials developed during the MaDriX project. In a short version, this test was focused mainly on the on- and off-currents, defined as the currents measured at V_{GS} = - 20 V and 0 V, respectively (at V_{DS} = - 20 V), and the resulting on / off ratio. This test was also implemented into the StaLa software as a fixed measurement routine. It consists of the following measurements:

Measurement	V_{DS}	V_{GS}
On / off ratio	- 20 V	0 V (off) - 20 V (on)
Transfer curves	- 20 V - 1 V	+ 5 V → - 20 V 0.5 V steps
Output curves	0 V → - 20 V 0.5 V steps	0 V → - 20 V 2 V steps
Hysteresis	- 20 V	0 V → - 20 V and back 3 cycles
Time dependence	- 20 V	0 V - 20 V 20 s each

Figure 13: Parameters of a standard test.

For most purposes of this work, not only the on and off currents, but especially the charge carrier mobility, the exponent γ of its dependence on the charge carrier density (and thus on the gate voltage), the threshold voltage and the bulk current were of interest (see chapter 5.1 on how they were extracted). Therefore, usually transfer curves were recorded for all transistors of one sample, or at least all *K10* transistors, at V_{DS} = -1 and -20 V, with the gate voltage varied from + 20 to - 20 V and back again. In the case of thicker insulators, even higher gate voltages than ± 20 V were applied. In addition, as a leakage test, an additional "transfer curve" was taken from every transistor, where the gate voltage was swept over the same voltage range as for the transfer curves, but the drain voltage was kept at zero. Transistors that showed

a significant leakage current to the drain, and not just to the common source, in this measurement were taken out of the analysis.

For the data evaluation, usually average values of the charge carrier mobility prefactor μ_0, the threshold voltage V_{th}, the exponent γ of the dependence of the mobility on the gate voltage, and the bulk resistance were considered, averaged over all *K10* devices which had no significant leakage between the gate and the drain electrodes.

4.2 Semiconductors

4.2.1 Poly(3-hexylthiophene)

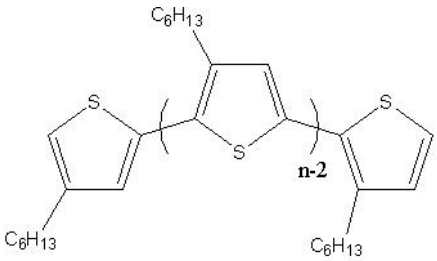

Figure 14: Structural formula of poly(3-hexylthiophene) (P3HT).

Poly(3-hexylthiophene) (P3HT, figure 14) is one of the most commonly investigated polymeric semiconductors. In the molecular structure of its carbon backbone, single bonds are always alternating with double bonds. A polymer with this feature is called a *conjugated polymer* [44]. The electrons of the single bonds, also called σ-bonds, are highly localized. A double bond consists of a σ- and a π-bond, which is the overlap of the p_z electrons of the neighboring carbon atoms. In a conjugated molecule with alternating single and double bonds, the electrons in the π-bonds are delocalized above and below the plane of the molecule. Therefore they can contribute to charge transport quite easily. Other well-studied conjugated molecules are e.g. poly(phenylene vinylene) (PPV) [45] or anthracene and pentacene [46], all known for their relatively high charge carrier mobility.

Thiophenes exist in an enormous variety of materials, e.g. as oligomers, dimers, polymers and copolymers [47]. Thiophenes like DHnT [48] or DDnT [49] belong to the most investigated oligomers as well as those with the highest mobilities [50]. This is also due to the conjugated π-electron system of their thiophene rings. In addition, these π-electrons cause good ordering of the oligothiophenes, furthermore increasing

the mobility and making it an interesting material for growth and cristallinity studies in vacuum deposited films of these hardly soluble materials [51]. Also the polythiophenes exhibit a tendency to not entirely disordered film structure, but there is a certain cristallinity, making P3HT a very attractive material for structural studies, e.g. in dependence of the molecular weight [52] [53] or the regio-regularity [54].

In addition, P3HT is well soluble in solvents like chloroform, toluene, dichlorobenzene among others and exhibits charge carrier mobilities of up to 0.1 cm^2/Vs, which is among the highest for polymers. Polymers with good solubility and even better performance have been reported, but those, as e.g. pBTTT [55], require a much more difficult chemical synthesis, which increases their price dramatically and eliminates them from the candidates for low-cost applications. Therefore, P3HT can be counted among today's commercially available materials which are closest to the requirements for low-cost applications in terms of performance, solubility and price.

In most experiments in this work, a P3HT was used which was produced by *BASF*, Ludwigshafen, for use within the MaDriX project. It is named *Sepiolid PX MaDriX* according to the BASF naming conventions. Rather low regio-regularity does not allow for record mobility, however, the rather cheap production costs on a high scale and the good solubility make it a material close to the requirements for printed circuits, the major aim of the MaDriX project. In addition to *Sepiolid PX MaDriX*, a very highly (>98 %) regio-regular P3HT, also produced by BASF under the name of *Sepiolid P 200*, was used for comparison.

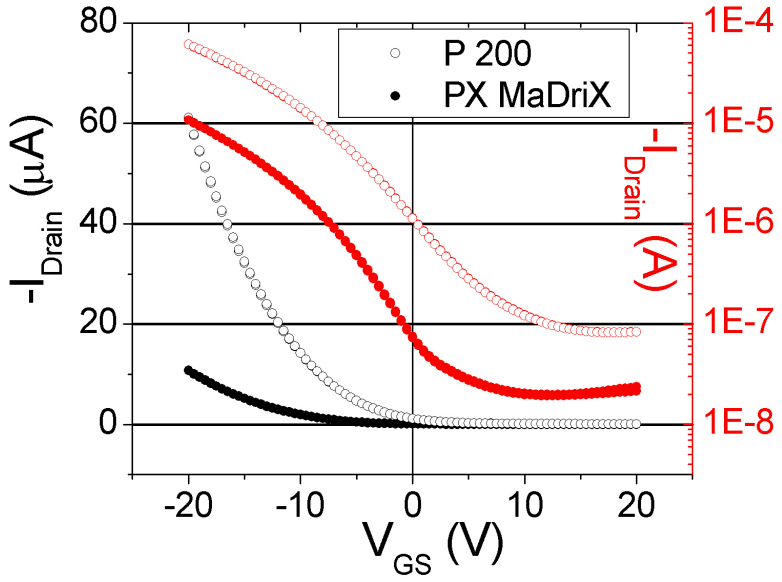

Figure 15: Transfer curves (linear (black) and logarithmic (red) plot) of two average *K10* transistors with 30 nm thick *Sepiolid PX MaDriX* (full points) and *Sepiolid P 200* (open points) as semiconductor, spin-coated from solution in toluene, at V_{DS} = -20 V. The insulator is 350 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 4* (batch 2), in both cases. The only difference in the preparation of the two samples was the different kind of P3HT used.

Figure 15 shows the difference in performance between those two different kinds of P3HT. Two standard MaDriX samples were prepared in the same way, with the only difference that in one sample, P3HT *Sepiolid PX MaDriX* was used as semiconductor (full points), and in the other sample, shown by the open points, P3HT *Sepiolid P 200*. The transistors shown are transistors which were very close to the average mobility, threshold voltage, gamma and bulk resistance values. While at V_{aa} = 20 V the average mobility prefactor μ_0 is $5.0{\cdot}10^{-3}$ cm^2/Vs in the case of *Sepiolid PX MaDriX*, it is increased to $1.7{\cdot}10^{-2}$ cm^2/Vs with the use of *Sepiolid P 200*. The threshold voltage however is shifted from 3.3 to 7.0 V and the bulk resistance lowered from 2.8 to 0.4 GΩ, while γ increases from 1.1 to 1.3. So due to the higher regio-regularity, which causes higher cristallinity in the P3HT layer, the on-current and the mobility are increased by more than a factor of 3. However, the off-current is also increased, by a shift in the threshold voltage as well as by an increase in the bulk current, which results in a lower on/off ratio between the current at V_{GS} = - 20 V and the current at V_{GS} = 0 V: While it is 157 in the case of sample bgm073 with *Sepiolid PX MaDriX*, it is

reduced to only 59 in the case of sample bgm066 with *Sepiolid P 200*. Depending on the purpose, higher regio-regularity thus does not necessarily mean better performance, as the higher charge carrier mobility coincides with high conductivity even without any applied gate voltage, which results in a quite poor on/off switching behavior.

4.2.2 Solvent for P3HT

Not only do the characteristic molecular properties of the organic semiconductor itself have tremendous impact on the device performance, but also the solvent in which the material is dissolved for spin-coating plays an important role. As explained above in chapter 4.2.1, the good charge transport properties of P3HT originate in its comparably high ordering in the film. From oligothiophenes it is known that the molecular layers are better ordered when they have more time to do so, i.e. at decreased evaporation speed. In the case of wet-chemically processed semiconductor films, higher times for film formation and thus for improved molecular ordering can be achieved by using solvents with higher boiling point. In this case, the time until the complete evaporation of the solvent is extended, which gives the polymer chains more time to assemble in quasi-crystalline grains.

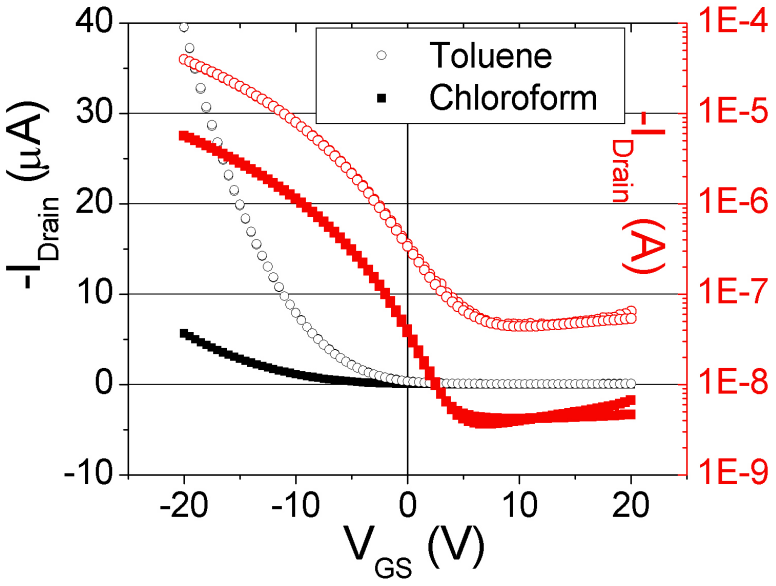

Figure 16: Transfer curves (linear (black) and logarithmic (red) plot) of two average *K10* transistors with 30 nm thick *Sepiolid P 200* as semiconductor, spin-coated from solution in chloroform (filled points) and toluene (open points), at V_{DS} = -20 V. The insulator is 350 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 4* (batch 1), in both cases. The only difference in the preparation of the two samples was the different semiconductor solvent.

The tremendous improvement caused by the use of a slowly evaporating high boiling point solvent is demonstrated in figure 16, which shows average transfer curves of *K10* transistors from sample bgm065 and bgm067. Both samples have a 30 nm thick layer of P3HT *Sepiolid P200* as semiconductor and the same insulator prepared in the same way. For sample bgm067, the semiconductor was applied from solution in chloroform (boiling point 61°C), the solvent used for sample bgm065 was toluene, with a boiling point of 111°C. The difference in performance is enormous: While the average mobility prefactor of the transistors from bgm067 is just $2.2 \cdot 10^{-3}$ cm^2/Vs at V_{aa} = 20 V, bgm065 has an average mobility of $1.7 \cdot 10^{-2}$ cm^2/Vs. The average on current at V_{GS} = -20 V is hereby increased from 5 to 37 μA. As the threshold voltage remains almost the same (5.3 compared to 5.5 V), the on/off ratio is similar in both samples, around 100. The better ordering of the P3HT layer upon the use of toluene is also reflected in a slightly reduced gamma exponent of 1.0 instead of 1.2.

4.2.3 PDI8CN2

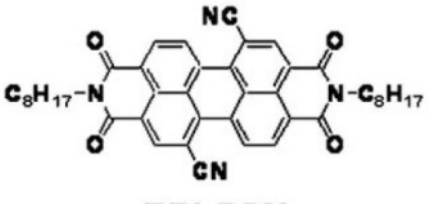

Figure 17: Structural formula of "*N100*".

Many applications including organic CMOS require not only good p-type semiconductors, but also n-type semiconductors with comparable performance (see chapter 1.3). However, n-type organic semiconductors have been lagging behind their p-type counterparts for a long time [56] [57]. There are still not many solution-processable n-type semiconductors available. One which was developed quite recently is N,N-Dioctyldicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI8CN2 - figure 17), sold by BASF under the name of *Sepiolid N100*. It is not a polymer, but a small molecule, but can be processed by spin-coating from solution e.g. in chloroform. Figure 18 shows transfer and output curves from sample bgm055. With V_{aa} = 20 V, the average μ_0 at V_{DS} = 20 V is just $4.1{\cdot}10^{-4}$ cm^2/Vs with an average on-current of only 750 nA, but due to low parallel current and a very good threshold voltage of -0.1 V, the material reaches a high average on/off ratio of 99. Typical for a small molecule in comparison to a polymer is the gate voltage independent charge carrier mobility: From the fits, the average gamma is determined as 0.2.

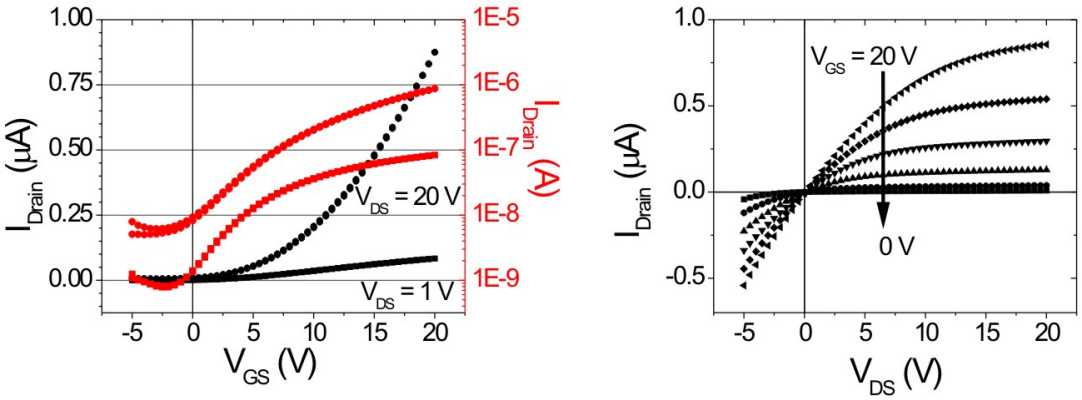

Figure 18: Transfer curves (linear (black) and logarithmic (red) plot) of an average *K10* transistor with ca. 20 nm thick *Sepiolid N 100* as semiconductor, spin-coated from solution in chloroform, at V_{DS} = 1 V and 20 V, as well as its output characteristics. The insulator is 350 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 4* (batch 1).

The result proves that with the flexible PET foil substrates used in the project, with gold source and drain electrodes, n-channel OFETs with solution-processed organic semiconductor and insulator are possible, the prerequisite for any organic circuitry. With this material setup, organic CMOS inverters have been realized [58].

4.3 Insulators

In the organic electronics research field, a wide multitude of materials is used as gate insulators in organic field-effect transistors [59]. According to equation 2 and as shown in the introduction (chapter 1.3), a higher dielectric constant of the insulator increases the transistor current, or the same transistor current is driven by lower operation voltages. Therefore, many research groups focus on finding suitable *"high-k dielectrics"* [60] [61]. However, other studies claim that low-k insulator materials generally cause better OFET performance [62].

While in fundamental research silicon wafers are frequently used as smooth, defect-free transistor substrates, with thermally grown silicon oxide as gate insulator, flexible devices and printing processes require flexible, solution-processable insulators. Among many others [63], commonly used polymeric insulators include [10]: poly(vinyl phenol) (PVP) [64], polyvinyl alcohol (PVA) [65] [66], polyvinylidenfluoride (PVDF) [67],

polystyrene (PS) [68] [69], and poly(methyl methacrylate) (PMMA) [70]. From these different materials, two were chosen for the analysis which fulfill the requirements listed in chapter 1.3: PMMA and polystyrene.

4.3.1 Poly(methyl methacrylate)

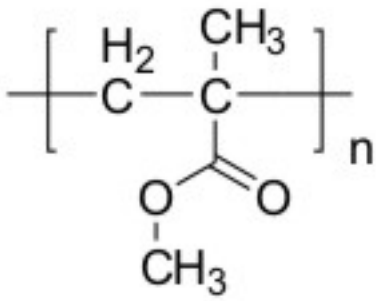

Figure 19: Structural formula of poly(methyl methacrylate) (PMMA).

Figure 19 shows the structural formula of poly(methyl methacrylate) (PMMA). PMMA has been known and produced on a large scale for decades, as a light, stable and transparent replacement for glass ("Plexiglas") with multiple applications in industry, manufacturing, optics, medicine and art, among others [71]. In micro- and nanostructuring, it is used as resist in electron beam lithography. As an electrical insulator, it has a dielectric constant of 3.8, the same as silicon dioxide.

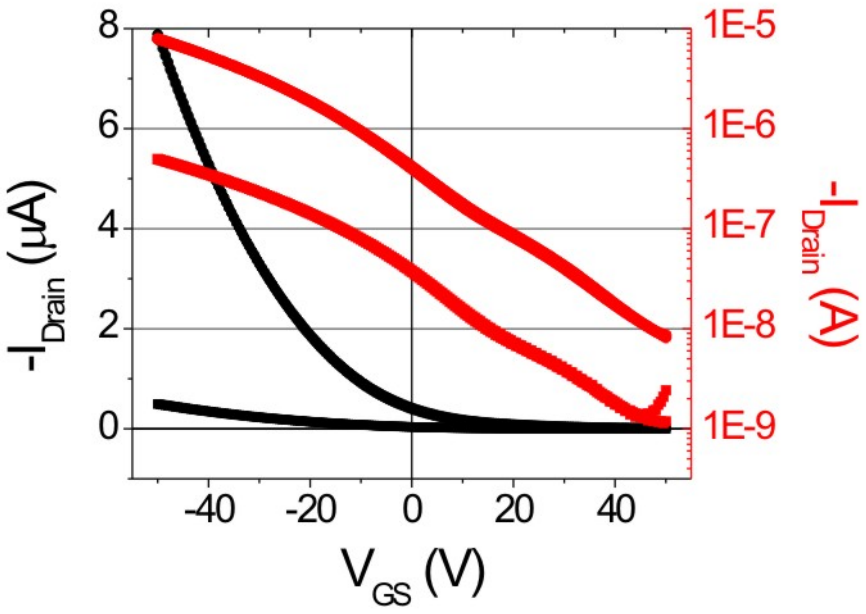

Figure 20: Transfer curves (linear (black) and logarithmic (red) plot) of an average *K20* transistor with 39 nm thick P3HT as semiconductor, spin-coated from solution in chloroform, at V_{DS} = -1 V and -20 V. The insulator is 860 nm thick poly(methyl methacrylate) (PMMA), spin-coated from solution in methyl-ethyl ketone (MEK).

Figure 20 shows transfer curves from sample bgm030, fabricated with a PMMA with a molecular weight of 1250 kDa from *Evonik degussa*, spin-coated from 5 wt-% solution in butanone (methyl-ethyl ketone, MEK). Due to high fallout rates because of leakage, such high concentration was chosen, which results in a layer thickness of 860 nm. For V_{DS} = -20 V, the average mobility prefactor μ_0 at V_{aa} = 80 V is $1.3 \cdot 10^{-3} cm^2/Vs$, V_{th} is 37 V, and γ 2.0. Due to the very high positive threshold voltage (even if calculated to a thinner insulator thickness), the off current at V_{GS} = 0 V is around 400 nA and the on/off ratio, even for V_{GS} = -50 V / 0 V, is just 20, for V_{GS} = -20 V / 0 V even less than 5.

4.3.2 Polystyrene

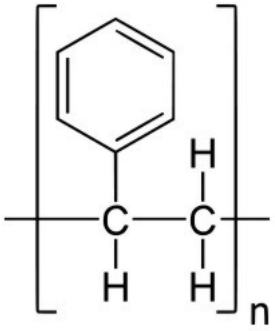

Figure 21: Structural formula of polystyrene.

Because of these unsufficient results with the non-optimized PMMA as gate insulator in OFETs, another insulator material, a polystyrene (see figure 21) derivative, was used. It was received from *PolyIC* in the frame of the *MaDriX* project and is therefore called *PolyIC insulator* in the following. While it was possible to demonstrate that better performance is indeed achievable with this material, it is also a good example of how variations in the preparation process, like the change of the insulator solvent, largely affect the OFET properties, especially the insulation quality of the insulator and the electrical performance of the devices.

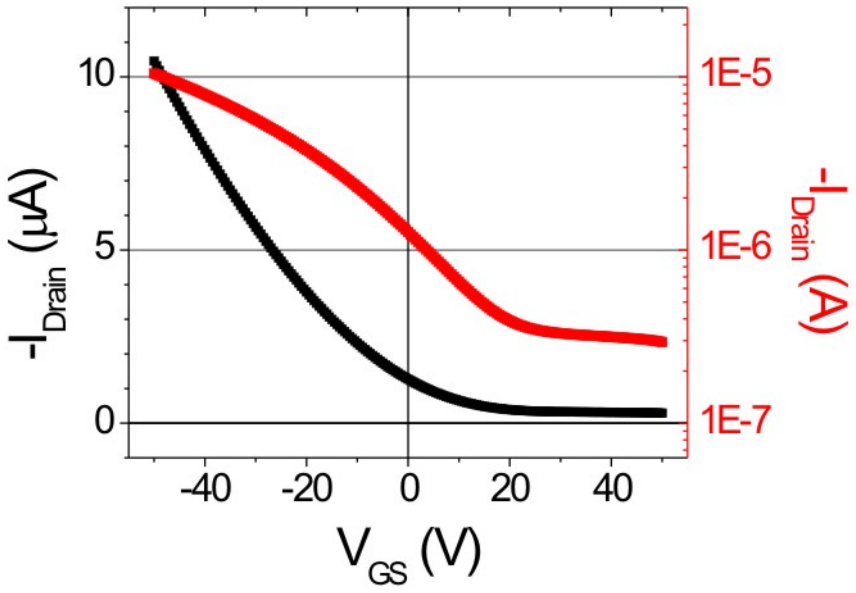

Figure 22: Transfer curves (linear (black) and logarithmic (red) plot) of a *K20* transistor with ca. 50 nm thick P3HT as semiconductor, spin-coated from solution in chloroform, at V_{DS} = -20 V. The insulator is 840 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 1*.

In preliminary experiments on glass substrates, *solvent 1* (see [43]) had been proven to be a good solvent for the *PolyIC insulator*. However, in spite of big efforts, no good transistors could ever be built successfully with this solvent on PET substrates. With the aimed insulator thickness of 300 - 400 nm, the success rate was very close to 0, as more than 95 % of all transistors featured a short circuit through the insulator. Only at very high insulator thickness of 840 nm was it possible to obtain working transistors like the one shown in figure 22, but with no improvement in performance compared to the PMMA devices shown above in section 4.3.1. With a threshold voltage V_{th} of 30 V and a bulk resistivity of just 61 MΩ, the off current is even more than 1 μA and the on/off ratio below 10. A slightly increased mobility prefactor μ_0 at V_{aa} = 80 V of $2.0 \cdot 10^{-3} cm^2/Vs$ is mainly due to a slightly higher P3HT thickness used in this sample. Only the considerably reduced gamma exponent of 0.95 shows some improvement, being the sign of apparently higher molecular ordering at the interface.

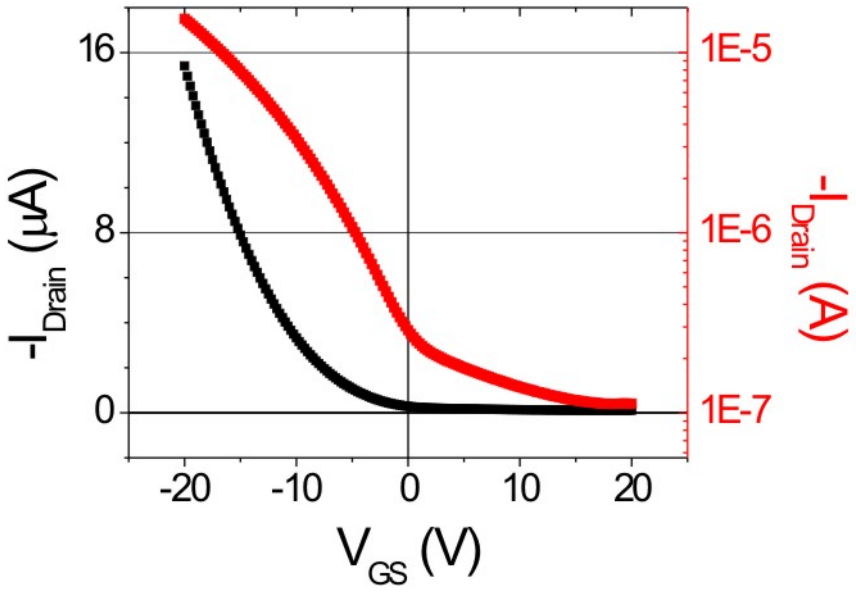

Figure 23: Transfer curves (linear (black) and logarithmic (red) plot) of a *K20* transistor with ca. 30 nm thick P3HT as semiconductor, spin-coated from solution in toluene, at V_{DS} = -20 V. The insulator is 350 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 2*.

The use of *solvent 2* for the *PolyIC insulator* drastically improves the performance. Even at an insulator thickness of 350 nm, which reduces dramatically the voltages needed for operation, the rate of working devices is higher than 80 %. Even with the use of toluene as P3HT solvent, which exhibits larger currents than P3HT processed from solution in chloroform (see chapter 4.2.2), the average off current is just 430 nA, and with the high on currents achieved, the average on/off ratio is 31 between - 20 and 0 V. Figure 23 shows a transfer curve. It is visible very clearly that the threshold voltage could be largely reduced to 5.5 V, and in spite of the use of toluene, which also causes increased bulk currents, the bulk resistance even increased to 140 MΩ. At V_{aa} = 20 V, μ_0 is $5.9 \cdot 10^{-3} cm^2/Vs$.

Using *solvent 3* yielded the same high percentage of working devices, and the average on/off ratio could be increased from just over 30 to 148, in spite of lower on current. The reason is that with this material system, the threshold voltage was still lowered, down to 3.3 V on average. Also the bulk resistance is much higher, with 4.1 GΩ. Thereby, the average off current is reduced to just 65 nA. Figure 24 shows this difference in logarithmic plots of transfer curves from the two different devices.

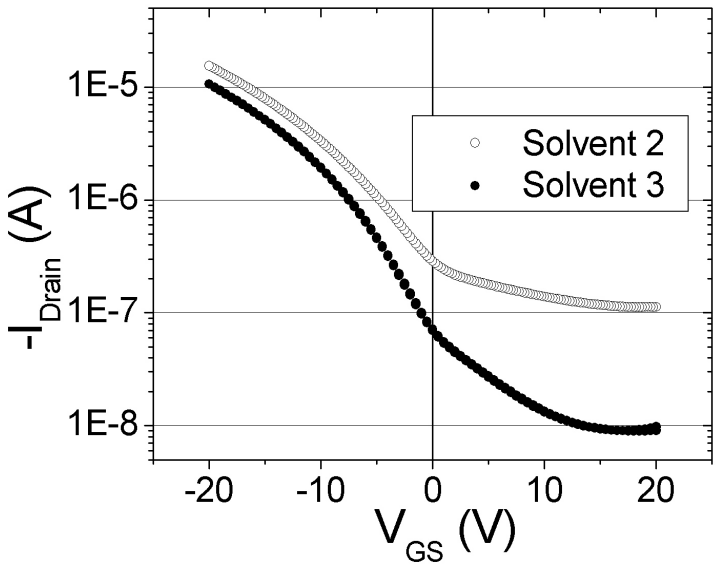

Figure 24: Transfer curves (logarithmic plot) of transistors with ca. 30 nm thick P3HT as semiconductor, spin-coated from solution in toluene, at V_{DS} = -20 V. The insulator is 350 nm thick *PolyIC insulator*, spin-coated from solution in *solvent 2* (empty points) and *solvent 3* (filled points).

With the use of the chemically similar *solvent 4*, the average off current was further reduced to 58 nA, resulting in an increased on/off ratio of 157. These results demonstrate the high importance of the interface between semiconductor and insulator for the device performance. Therefore, optimization of the on/off ratio via improved threshold voltage and bulk resistivity, the challenge presented in chapter 1.3, could not be obtained by just tuning the semiconductor material (and its solvent) alone, but was achieved by selection of the best suited gate insulator, with the insulator solvent playing a significant role.

Chemical modifications of *solvent 4* allowed for additional tuning of the threshold voltage, resulting in dramatic further reduction of the off current and in an average on/off ratio close to 500, with single devices having on/off ratios of more than 1000. This will be described in the section on charge transport, in chapter 5.4.

5 Modeling of charge transport in P3HT OFETs

5.1 Fitting and data extraction

In order to achieve a consistent model for the charge transport in a disordered system like P3HT, several parameters of the transistors were changed in order to check how this affects the electrical transistor characteristics. The varied parameters included the thickness of the semiconductor thin film, which also changes the average grain size in the P3HT film, the temperature of the sample during the measurement and the composition of the insulator solvent.

A common way of analysing transistor characteristics and their changes upon variations in the sample preparation or temperature is to investigate the charge carrier mobility and the threshold voltage extracted from transfer curve measurements. However, in case the mobility is not constant, but depends on the charge carrier density and therefore on the gate voltage, a linear fit (or a quadratic fit in the saturation regime) cannot reproduce the whole transfer curve. In most cases, only a very small part of the curve, generally at the highest (most negative) gate voltage, is then considered for the determination of the mobility as shown in figure 25.

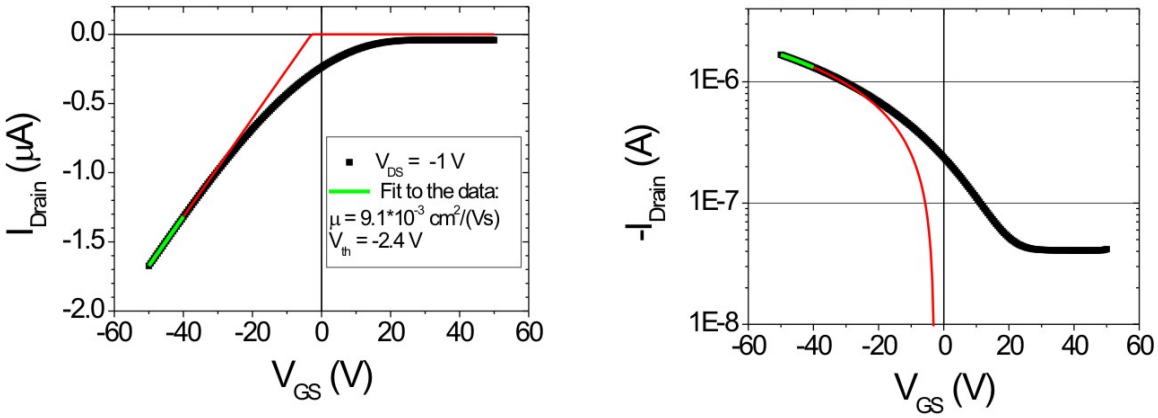

Figure 25: Transfer curve of an OFET recorded in linear regime (V_{DS} = -1 V) shown in linear (left) and logarithmic (right) plot. The short green line shows a linear fit to the curve in the range of V_{GS} = -50 V to -40 V. The red curve shows how the fit with the hereby determined parameters extends over the whole voltage range.

In this case, a linear fit was made to the transfer curve in the range from V_{GS} = -50 V to -40 V. This fit gives indeed the charge carrier mobility at this particular voltage range, whereas the deviation of the fit is enormous in the rest of the measured voltage range. Thus, the second parameter that was determined from the fit, the "threshold voltage", is meaningless as it is very far away from the physical threshold voltage at which the transistor opens when a conducting channel is formed. As a result, the mobility at the chosen gate voltage range is the only information obtained from such a fit, but even this information is not well suited for comparison with other transistors, as threshold voltage shifts or different curvatures of the transfer curve have to be taken into account carefully. All other information contained in the curve, like the true threshold voltage or the curvature of the slope, related to the carrier concentration dependence of the mobility, can not be obtained from such a fit. Fitting over the entire gate voltage range as shown in figure 26 does not solve this problem either, as the fit is then closer to the entirety of the transfer curve, but still the deviation is too big, the threshold voltage is not determined correctly and no information on the gate voltage dependence of the mobility is obtained.

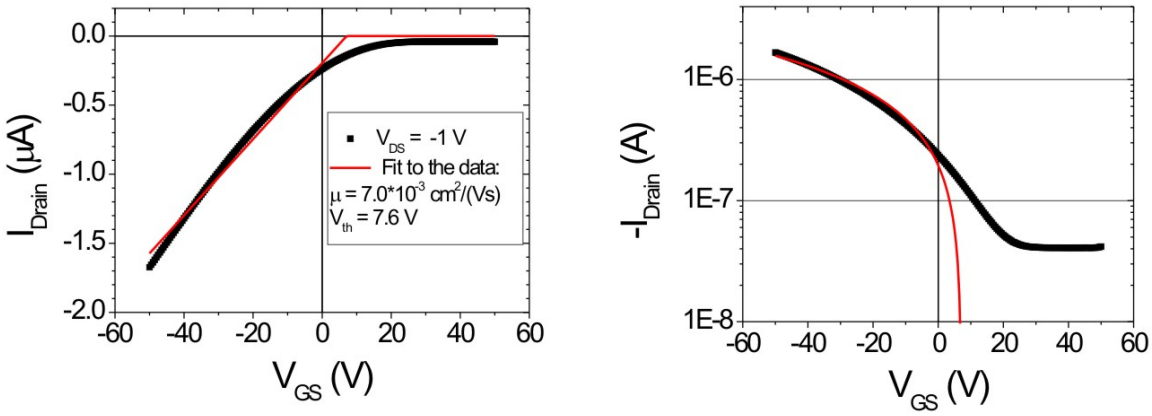

Figure 26: Transfer curve of an OFET recorded in linear regime (V_{DS} = -1 V) shown in linear (left) and logarithmic (right) plot. The red line shows a linear fit to the entire curve.

Due to these reasons, in this work a fit was used which takes into account the dependence of the charge carrier mobility on the carrier density, which is tuned by the gate voltage. In this fit, the expression from Vissenberg and Matters, as shown in equation 15 in chapter 2.3.3 was simplified for the use at one certain temperature as:

$$\mu(V_{GS}) = \mu_0 \left(\frac{V_{GS} - V_{th}}{V_{aa}} \right)^{\gamma} \tag{35}$$

The exponent γ corresponds to the second exponent $2\left(\frac{T_0}{T} - 1\right)$ in equation 15. Via

$$\gamma = 2\left(\frac{T_0}{T} - 1\right) = 2\left(\frac{\sigma_{DOS}}{k_B T} - 1\right) \tag{36}$$

it is thus directly related to the width σ_{DOS} of the density of states N

$$N \propto exp\left(\frac{E}{\sigma_{DOS}}\right) \tag{37}$$

and therefore provides valuable information about the energetic disorder of the system. γ=0 represents the case of a constant charge carrier mobility, as in well-ordered systems like evaporated oligomer films. The prefactor μ_0 yields the mobility at V_{GS}-$V_{th} = V_{aa}$, which also defines the parameter V_{aa}, which is therefore not a fitting parameter, but a parameter whose value is chosen according to the voltage range which is taken into account.

Figure 27 shows a fit according to formula 35 to the same curve as in figures 25 and 26. One can see that now the entire tranfer curve is fitted accurately. In addition, the fit parameter γ gives information about the shape of the transfer curve.

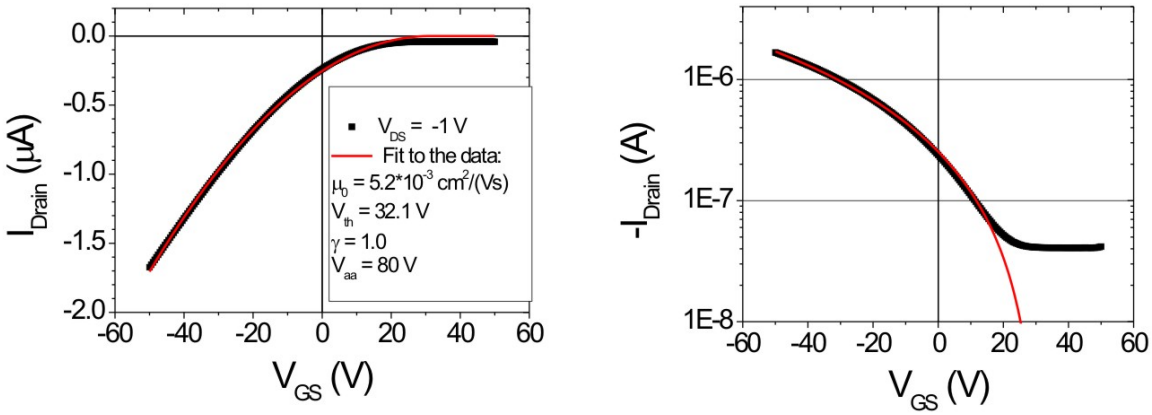

Figure 27: Transfer curve of an OFET recorded in linear regime (V_{DS} = -1 V) shown in linear (left) and logarithmic (right) plot. The red line shows a fit to the entire curve according to equation 35.

The only part of the transfer curve at which there is still a considerable deviation of the fit is the area around the threshold voltage and in the off regime, above the threshold voltage. In contrast to the prediction, the current is not completely switched off at gate voltages more positive than the threshold, but an approximately constant current remains. As will be shown later in section 5.2, this current is increasing with semiconductor film thickness and thus particularly pronounced in the curves shown here, which were taken from a transistor with a P3HT thickness of more than 200 nm. For the fitting, the current I_{VM}, which is the transistor current as in equation 2 with a charge carrier mobility according to equation 35, was therefore extended by an additional, constant current, depending only on the drain voltage and an additional fit parameter, the bulk resistance R_{bulk}:

$$I_{Drain} = I_{VM} + \frac{V_{DS}}{R_{bulk}} \tag{38}$$

This simplified description of the bulk current is useful for most purposes. A more detailed model of the bulk current will be given in section 5.2.5 of this chapter. A fit to the transfer curve following this equation can be seen in the following figure 28. The fit can now really reproduce the entire curve, except a small part in the subthreshold regime. One can notice that due to the wrong reproduction of the curve around the threshold, not only the threshold voltage itself was miscalculated by more than 10 Volts by fit equation 35, but also the deviation in the values of the mobility and the

exponent γ is considerable.

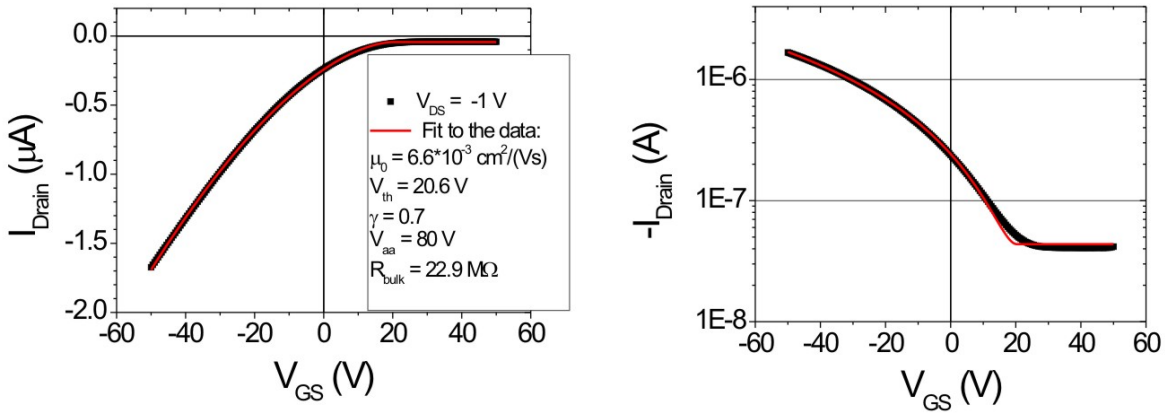

Figure 28: Transfer curve of an OFET recorded in linear regime (V_{DS} = -1 V) shown in linear (left) and logarithmic (right) plot. The red line shows a fit to the entire curve according to equation 38.

5.2 Active layer thickness dependence

Growth studies of organic semiconductors have played a major role in the attempts to understand the relations between growth and ordering of the organic molecules in the semiconductor layer on the one hand, and the quality of charge transport, mainly expressed by the charge carrier mobility, on the other hand. As an example, thickness dependent studies on oligothiophenes deposited by molecular beam deposition in ultra-high vacuum revealed that the charge carrier mobility is highest upon completion of the first and second monolayer and remains fairly constant when further increasing the semiconductor thickness. This finding showed that the charge transport in these systems takes place mainly in the first two monolayers close to the insulator / semiconductor interface [72]. After the completion of the first monolayer and before the completion of the second monolayer, the mobility has a local minimum. This shows that the presence of incomplete layers even hinders charge transport in the underlying complete monolayer(s).

Unlike these small oligothiophene molecules deposited in vacuum by evaporation, the long polythiophene chains processed from solution do not show such high ordering [73]. Several studies on the dependence of the charge carrier mobility on the P3HT film thickness have been performed [74] [75] [76], also with respect to structural ordering

in the layer [77] [78]. They were performed on bottom-gate transistors on silicon substrates with the silicon serving as common gate electrode and a silicon oxide layer serving as gate insulator on which source and drain electrodes as well as the P3HT were deposited. Increasing mobility with increasing P3HT layer thickness was found for thin layers in these bottom-gate transistors on silicon substrates. Sandberg et al. presume that because of interfacial strain, thin layers / monolayers are poorly ordered whereas the presence of a highly ordered bulk in thicker films causes an ordering effect in the interfacial layer [77]. This reordering is obviously completed at a thickness of ca. 20 nm, where Wang et al. found a constant charge carrier mobility after a strong increase with thickness for thinner layers [76]. Further deposition of the polymer to even higher thickness does not have a big effect on the interface layers any more. As the charge transport takes place mainly in the part of the semiconductor adjacent to the gate insulator, the charge carrier mobility remains fairly constant with further increased thickness.

In silicon-based OFETs P3HT is processed on the smooth surface of silicon oxide. In top-gate devices however, the interface between insulator and semiconductor, at which the charge transport is presumed to take place, is the one between the upper side of the P3HT layer and the organic insulator deposited on top of it. Thus possible changes in the P3HT surface roughness, e.g. with increasing layer thickness, would directly affect the charge transport properties. Knipp et al. showed that in bottom-gate pentacene OFETs the charge carrier mobility of a device with a rough surface of the gate dielectric was more than one order of magnitude lower than in a film deposited on a smooth surface, while all other parameters remained the same [79]. In a more quantitative study, Steudel et al. investigated the relation between the rms value of the SiO_2 surface and the charge carrier mobility in OFETs produced on this surface and also found a strong mobility decrease with increasing rms value [80]. A similar result was found by Jung et al. [81] with spin-coated polythiophenes on SiO_2 and could be related to the grain size variation with surface roughness. Therefore, the thickness dependence of the P3HT charge carrier mobility determined in silicon-based bottom-gate devices cannot be transferred to the top-gate device setup.

To study the dependence of the transistor behavior on the thickness of the P3HT film, a series of MaDriX standard samples was produced as described in chapter 3, where the P3HT thickness was varied systematically while all other parameters were kept constant. *Sepiolid PX MaDriX* (see chapter 4.2.1) was taken as P3HT and processed from solution in chloroform. The thickness of the semiconductor layer was varied by varying the concentration of the P3HT solution (see figure 29). The thickness of the layers was measured by a Dektak profilometer and confirmed by atomic force microscopy (AFM). As gate insulator, a thick (860 nm) layer of PMMA with a molecular weight of 1250 kDa was used. Figure 30 shows transfer curves from samples with six

different thicknesses, recorded at V_{DS} = -1 V. There is a clear trend to higher currents with higher P3HT thickness. The details will be analyzed in the following sections.

P3HT concentration in chloroform (wt-%)	P3HT thickness (nm)
0.02	3
0.05	10
0.1	12
0.2	17
0.3	21
0.5	39
0.7	53
1.0	88
2.0	216

Figure 29: Concentrations of P3HT in chloroform and the resulting layer thicknesses.

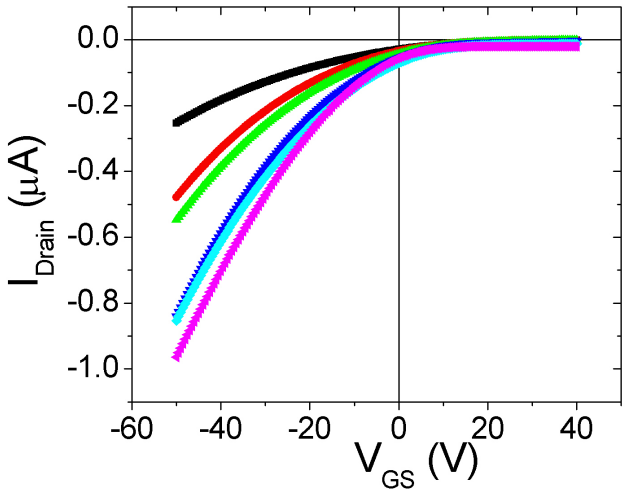

Figure 30: Transfer curves at V_{DS} = -1 V of six *K20* transistors with 12, 21, 39, 53, 88, and 216 nm P3HT thickness.

5.2.1 Charge carrier mobility

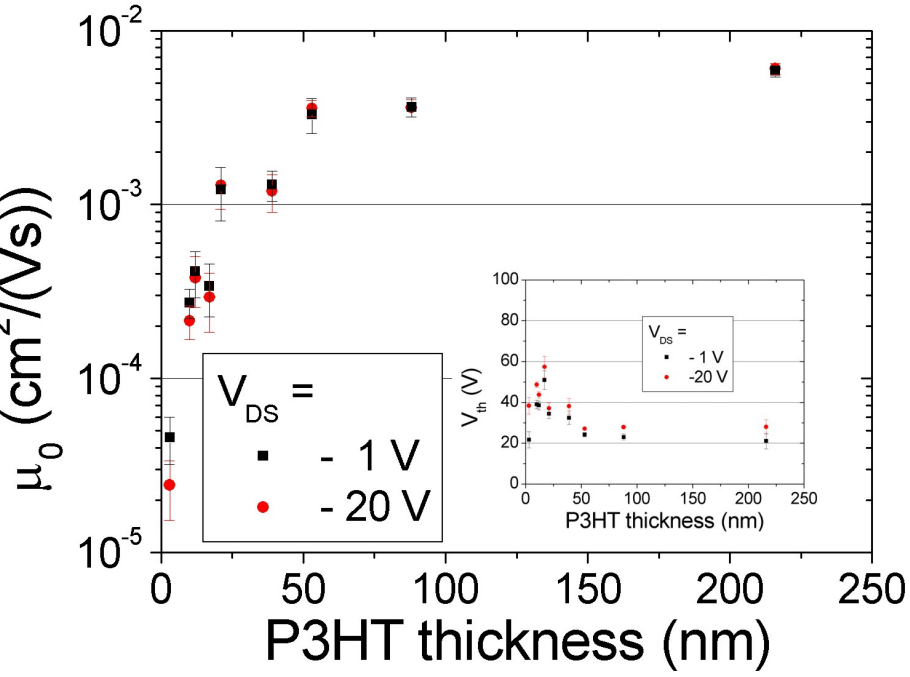

Figure 31: Average and standard deviation of the charge carrier mobility prefactor μ_0 of the *K20* transistors of nine different samples, plotted over the P3HT thickness. The black points show the values obtained from fits of transfer curves recorded in the linear regime at V_{DS} = -1 V, the red points are obtained from transfer curves recorded at V_{DS} = -20 V. V_{aa} = 80 V. The small graph shows the threshold voltage.

Figure 31 shows the average values and standard deviation of the charge carrier mobility prefactor μ_0 (at V_{aa} = 80 V) and the threshold voltage of the 12 transistors with L = 20 μm of nine different samples with the nine different P3HT layer thicknesses between 3 and 216 nm, as shown in the table in figure 29. As experiments with P3HT transistors processed by dip-coating have shown, a single monolayer of P3HT corresponds to a thickness of 2 nm [77] [82]. While for the smallest thickness of 3 nm, obtained by spin-coating a 0.02 wt-% solution, a low charge carrier mobility of just $2.4 \cdot 10^{-5}$ $\frac{cm^2}{Vs}$ is observed, at a film thickness of 21 nm the mobility increases by almost two orders of magnitude to $1.3 \cdot 10^{-3}$ $\frac{cm^2}{Vs}$. Upon further thickness increase, the mobility increase becomes less dramatic, and for films with thicknesses higher than 50 nm, a saturation of the mobility value at $4 \cdot 10^{-3}$ $\frac{cm^2}{Vs}$ is observed. In devices with thicker active layer, like the ones with 88 and 216 nm P3HT thickness, no significant increase of on-current

and mobility can be observed any more. The threshold voltage does not show a definite trend over the entire thickness range.

The low charge carrier mobility in very thin films of just a few monolayers can be explained in a similar way as by Sandberg et al. [77] for very thin films in bottom-gate devices: Due to interface strain, the molecular order directly at the interface to the substrate is very poor. In an ultra-thin film of only one or two monolayers, the conducting transistor channel is identical to the entire semiconductor film, and the charge transport quality suffers from poor molecular order of the polymer chains. In thicker films, while the first few monolayers close to the substrate probably remain poorly ordered, higher layers which are more distant to the substrate can assemble in a more highly ordered way. This is of great importance for top-gate transistors, as the charge transport channel, which is located close to the interface to the gate insulator, is exactly located in this upper part of the P3HT film. This explains why the charge carrier mobility is increased by almost two orders of magnitude upon increasing the layer thickness by less than one order of magnitude, from 3 to 20 nm. In even thicker layers, the influence of the substrate interface on the molecular order in the higher parts becomes less important, and at a thickness of 50 nm, the transistor channel has obviously the highest molecular order which is possible for this system.

5.2.2 Disorder parameter *gamma*

If the molecular order in the transistor channel is the decisive factor for the mobility dependence on the layer thickness, this ordering should also be reflected in the electronic order of the system. As shown in chapter 2.2 and 2.3.3, higher disorder means a broader distribution of hopping sites and is reflected by larger dependence of the charge carrier mobility on the carrier concentration and therefore on the gate voltage. The gamma parameter in equation 35 should then be higher in thinner films.

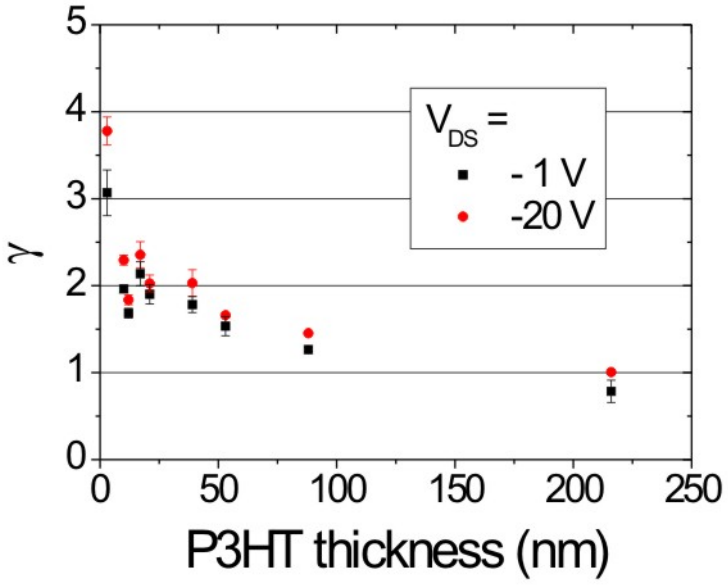

Figure 32: Average and standard deviation of the mobility exponent γ of the *K 20* transistors of nine different samples, plotted over the P3HT thickness. The black points show the values obtained from fits of transfer curves recorded in the linear regime at V_{DS} = -1 V, the red points are obtained from transfer curves recorded at V_{DS} = -20 V.

Figure 32 shows the average and standard deviation of the mobility exponent γ in dependence of the semiconductor thickness. Indeed, the exponent is very high for transistors with very thin P3HT layer and strongly decreases from 3.8 at 3 nm thickness down to less than 1.5 in thicknesses above 40 nm. For even bigger thickness, the change is much less dramatic. The behavior of gamma therefore follows the trend described above, showing high disorder in very thin P3HT films and increasing ordering in the transistor channel when the semiconductor layer is thicker. Above a layer thickness of ca. 50 nm, gamma is only reduced slightly, showing that the layer is thick enough so that the channel at the interface to the insulator is not influenced by the strain from the substrate any more. The effect of further increasing the semiconductor thickness is therefore small. From the values of γ the width of the exponential density of states is determined to be 38 meV (γ = 1.0) for the thickest film and increases up to 74 meV (γ = 3.8) in the thin films of 3 nm thickness. The analysis of the gamma exponent thus confirms that the mobility in thin P3HT films is low due to the molecular disorder of such a thin film, while the best ordering and thus also the maximum mobility is attained at 50 nm film thickness.

5.2.3 Structural order

In order to verify if this increase in electronic order with increasing layer thickness is also reflected by the structural order of the film, seen in better cristallinity, atomic force microscopy (AFM) images were recorded. Figure 33 shows the phase contrast images of six layers of P3HT *Sepiolid PX MaDriX* spin-coated from solution in chloroform onto glass or silicon substrates. From top to bottom, the P3HT concentration, and thereby the layer thickness, was increased from $\approx$ 0.01-0.02 wt-%, which corresponds to just $\approx$ 3 nm thickness, to 2 wt-% and thus a layer thickness of more than 200 nm. The thinnest film, shown in the upper left, which in the OFET exhibits very low charge carrier mobility and high mobility exponent γ, shows only a small degree of cristallinity. From a Fourier transformation of the image, the correlation length is determined to be smaller than 25 nm (AFM measurements were analyzed using the *WSxM* software [83]). In the 10 nm thick P3HT film shown in the upper right, the cristallinity is visibly higher, and the typical correlation length was determined to be between 50 and 60 nm. This is in good agreement with the finding that compared to the first film, the charge carrier mobility in such an OFET is almost one order of magnitude higher, with a strong decrease of γ at the same time.

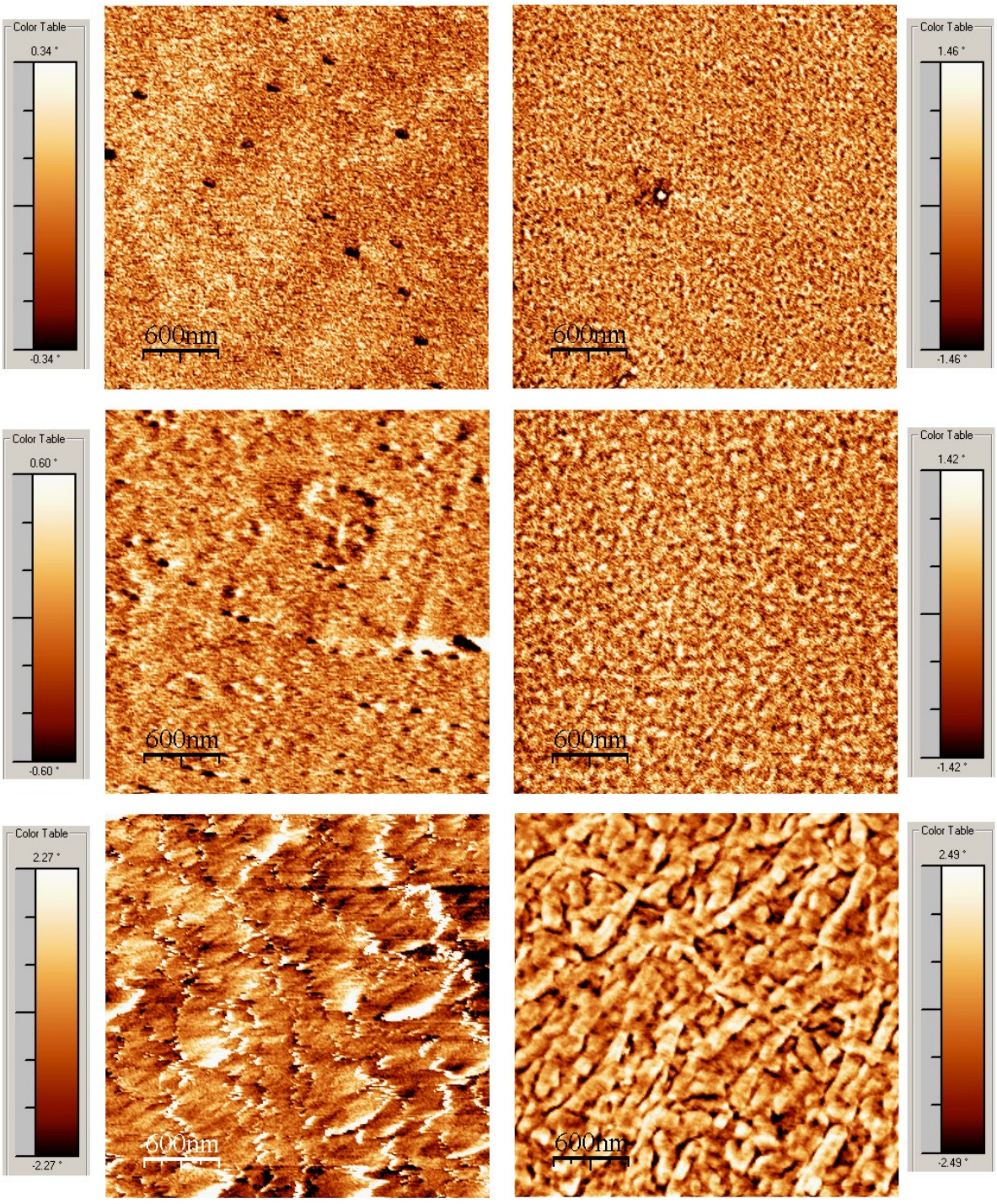

Figure 33: Phase contrast AFM pictures taken on 6 different P3HT films spin-coated on glass / silicon from solution in chloroform. All pictures are 3 x 3 μm^2 large, and the scale bar has a length of 600 nm. The P3HT thickness of the films shown is (from upper left to lower right): 3, 10, 20, 53, 88, and 216 nm.

The trend continues with a typical correlation length of 80 - 85 nm observed in a 20 nm thick film, while the film with 50 nm thickness exhibits around 150 nm correlation length. In contrast to what would be expected from the electrical measurements, the ordering keeps on increasing even upon further thickness increase beyond 50 nm: Typical correlation length is ca. 300 nm in a 88 nm thick layer and 500 nm in the 216 nm layer. However, not only is the size of the crystallites increased as it is the case in the range from 3 to 50 nm thickness, but also the layer structure is different in those thick films, as the polymer crystallizes in big rod-like structures. This change is clearly reflected in the surface roughness of the P3HT films: While all films with thickness up to 50 nm exhibit a smooth surface with an RMS value of 0.4 to 0.6 nm, the RMS roughness of the 100 nm thick layer is 3.4 nm and 4.8 nm for the thickest sample. The difference becomes clearly visible in the pictures in figure 34, where the AFM topography measurements of the 53 and of the 216 nm layer are shown with the same z-scale: On a scale that can display the entire topography range of the thicker sample, hardly any height difference is visible in the 53 nm sample.

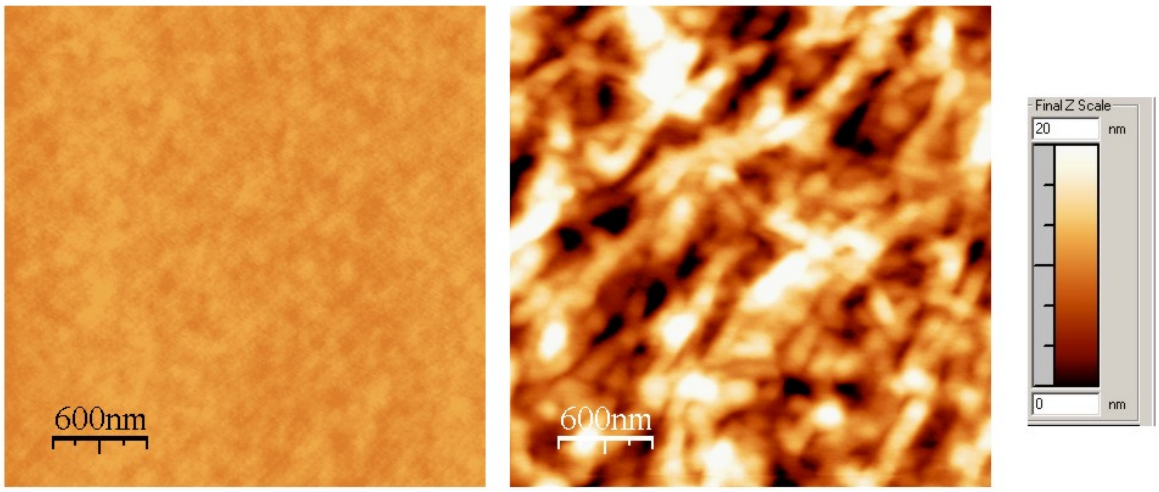

Figure 34: Topography AFM pictures taken on two of the P3HT films whose phase contrast images are shown in figure 33: On the left side, a 53 nm thick film, and on the right, a 216 nm film. Both pictures are 3 x 3 μm^2 in size, the z-scale is the same in both pictures with a height difference of 20 nm between white and black.

The fact that mobility and gamma are almost independent of the layer thickness for thicknesses higher than 50 nm thus has to be considered as the result of two contrary effects: On the one hand, the planar order keeps on increasing with increasing film thickness, with larger and larger crystallites forming. On the other hand, the vertical

order decreases, the P3HT surface becomes rougher in thicker films. As, in a transistor, this surface forms the interface to the gate dielectric where charge transport takes place, higher roughness there cancels out any improvement one would expect from larger grain sizes.

5.2.4 Dependence on solvent

Many studies have proven that in OFETs with spin-coated semiconductor films, the performance is improved when the semiconductor is spin-coated from solution in solvents with higher boiling points [84] [85]. This is most often attributed to the fact that high-boiling point solvents evaporate more slowly, and therefore the semiconductor layer has more time to form which improves its molecular ordering. If this is the case, one should not only expect higher charge carrier mobility, but also a reduced gamma exponent upon the use of toluene (boiling point: 111 °C) as P3HT solvent instead of chloroform (boiling point: 61 °C).

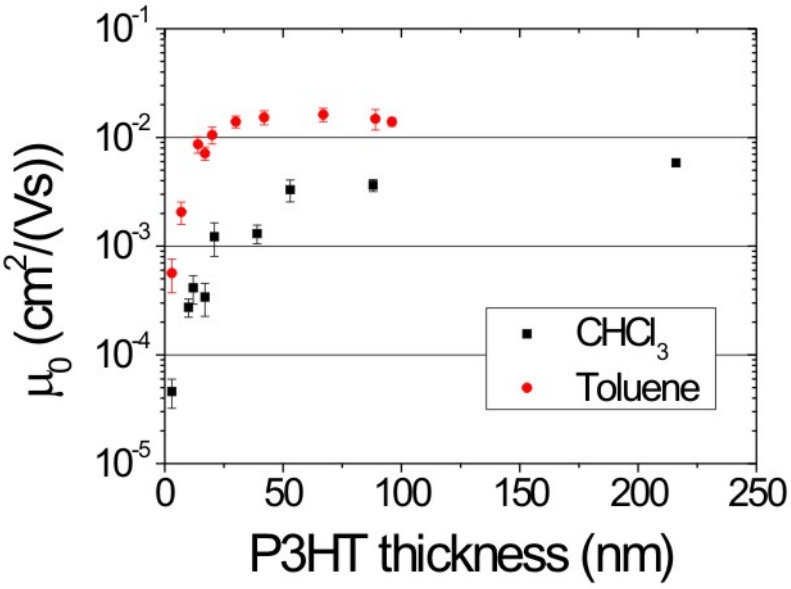

Figure 35: Average and standard deviation of the charge carrier mobility prefactor μ_0 of the *K 20* transistors of different samples, plotted over the P3HT thickness. The black points show the values from the transistors prepared with P3HT solution in chloroform, also displayed in figure 31, the red points are obtained from samples which were prepared with P3HT solution in toluene.

Figure 35 shows the mobility prefactor μ_0 plotted over the thickness of the P3HT layer for samples prepared from P3HT solutions in toluene together with the measurements on samples prepared from chloroform solutions shown above. It is clear that over the entire thickness range, the mobility is higher for the samples made from toluene solution than for those from chloroform solution. Up to a layer thickness of ca. 40 nm, the difference is about one order of magnitude. The qualitative thickness dependence of the toluene samples is very similar to that of the chloroform samples: While the mobility is very low at 3 nm layer thickness ($5.7 \cdot 10^{-4}$ $\frac{cm^2}{Vs}$) it increases drastically with increased layer thickness before reaching a maximum mobility and then staying constant upon further thickness increase. This maximum mobility is now $1.6 \cdot 10^{-2}$ $\frac{cm^2}{Vs}$. In contrast to the use of chloroform, this maximum mobility is already reached at a P3HT thickness of 30 nm. Due to the reduced solubility of P3HT in toluene, no layers thicker than 100 nm could be produced.

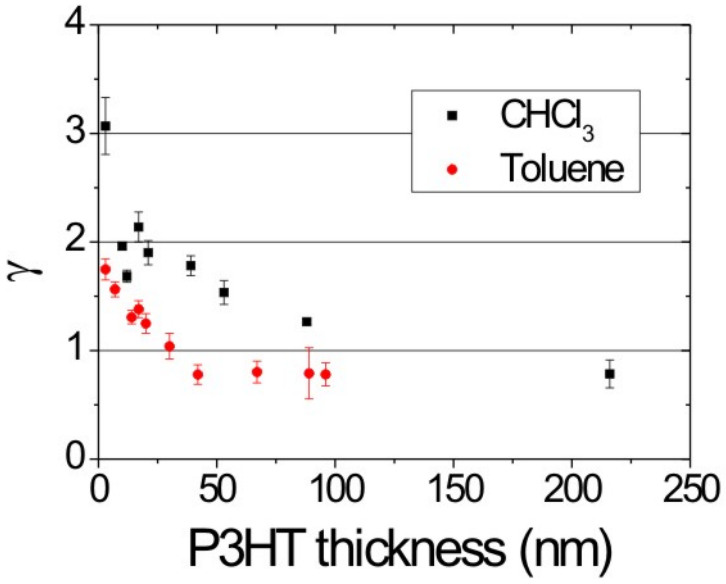

Figure 36: Average and standard deviation of the mobility exponent γ of the *K20* transistors of different samples, plotted over the P3HT thickness. The black points show the values from the transistors prepared with P3HT solution in chloroform, also displayed in figure 32, the red points are obtained from samples which were prepared with P3HT solution in toluene.

That this improvement in performance can be really attributed to higher ordering in the transistor channel, is proven by figure 36. For all layer thicknesses, the exponent γ is considerably lower with toluene than with chloroform. Even for the thinnest sample the average gamma is just 1.7. With increasing P3HT thickness, it decreases down to 0.8 at 42 nm and remains at this value for all higher thicknesses. The width of the density of states follows as 47 meV for the thinnest sample and 36 meV for all thick samples.

In conclusion, the mobility of P3HT top-gate transistors is low with monolayer P3HT films and strongly increases with semiconductor thickness. After a thickness of ca. 50 nm (solvent: chloroform) or 30 nm (solvent: toluene), the mobility hardly changes with P3HT thickness. This behavior can be attributed to the molecular ordering in the channel, which is reflected by the mobility exponent γ, which decreases with increasing layer thickness and also stays roughly constant after a certain threshold. Using the higher boiling point solvent toluene instead of chloroform increases the OFET mobility due to higher molecular ordering, also seen in a lower gamma value.

5.2.5 Bulk current

After analyzing the transistor current thoroughly, i.e. the current at gate voltages more negative than the threshold voltage, it is worth having a look on the current in the off-state, at more positive gate-source voltages than the threshold voltage. Any currents flowing in this regime are of high importance for device switching, as they increase the "off" current and therefore lead to decreased on/off ratios. This was also shown in chapters 4.2 and 4.3, with certain materials having bad off currents due to high bulk current.

According to most transistor descriptions, also those presented in chapter 2, the transistor is turned off completely when the gate-source voltage equals the threshold voltage. The transistor channel is then totally depleted of charge carriers, and no current is possible. However, in practice, current also flows in this regime, as seen in chapters 4.2 and 4.3. In the analysis there, it was called the bulk current, as, due to the depletion of the actual transistor channel, it is presumed to be located in the whole semiconductor layer.

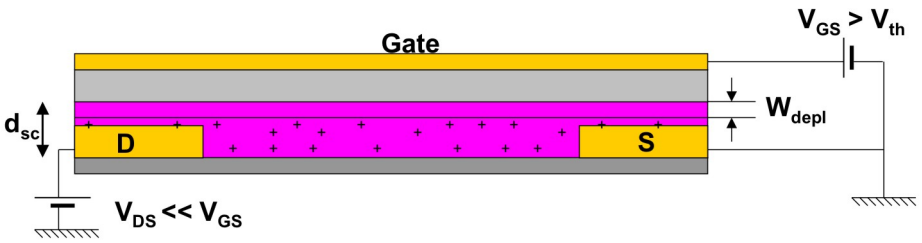

Figure 37: Sketch of the situation in an OFET with closed transistor channel. Charge carriers originated from doping with an acceptor concentration N_A are - at low drain voltage - distributed equally in the semiconductor over the whole layer thickness d_{sc}. Upon application of a gate voltage higher than the threshold voltage, the bulk is gradually depleted of carriers, with a depletion width W_{depl} which is a function of the gate voltage.

As at the threshold voltage, the transistor channel is depleted of intrinsic charge carriers, the carriers for the bulk current have to be provided by dopants to the semiconductor, which are present in the entire material with an acceptor concentration N_A. When the gate voltage is increased above the threshold voltage, carriers provided by these acceptors are gradually depleted (see figure 37). According to Maxwell's equation, the charge concentration in a depletion zone with width W_{depl} is related to the electric field necessary to produce the depletion by:

$$-q \cdot N_A = \rho = \epsilon_{sc}\epsilon_0 \nabla \vec{E} = \epsilon_{sc}\epsilon_0 \frac{\partial E_z}{\partial z} \tag{39}$$

So the electric field in the semiconductor is:

$$E_{sc} = W_{depl} \cdot \frac{-q \cdot N_A}{\epsilon_{sc}\epsilon_0} \tag{40}$$

With the potentials over semiconductor and insulator

$$\Delta\varphi_{sc} = \frac{1}{2} W_{depl} E_{sc} \tag{41}$$

$$\Delta\varphi_{ins} = d_{ins} E_{ins} = d_{ins} \frac{\epsilon_{sc}}{\epsilon_{ins}} E_{sc} \tag{42}$$

one obtains the following relation between the applied gate voltage

$$V_{GS} - V_{th} - V(x) = \Delta\varphi_{sc} + \Delta\varphi_{ins} \tag{43}$$

and the depletion width:

$$V_{GS} - V_{th} - V(x) = W_{depl} \cdot \frac{q \cdot N_A}{\epsilon_{sc}\epsilon_0} \cdot \left(\frac{1}{2}W_{depl} + d_{ins}\frac{\epsilon_{sc}}{\epsilon_{ins}}\right) \tag{44}$$

If one assumes that the bulk current is proportional to the thickness of the whole layer reduced by the depletion width, the bulk current at low drain voltages where the term V(x) can be neglected is described as follows:

$$\frac{I_{bulk}\left(V_{GS}\right)}{V_{DS}} = \left(d_{sc} - W_{depl}\left(V_{GS}\right)\right)\frac{W}{L}\sigma_{bulk} \tag{45}$$

$$\frac{I_{bulk}}{V_{DS}} = \left(d_{sc} - \left[\sqrt{\left(d_{ins}\frac{\epsilon_{sc}}{\epsilon_{ins}}\right)^2 + 2\frac{\epsilon_{sc}\epsilon_0}{q \cdot N_A}\left(V_{GS} - V_{th}\right)} - d_{ins}\frac{\epsilon_{sc}}{\epsilon_{ins}}\right]\right)\frac{W}{L}\sigma_{bulk} \tag{46}$$

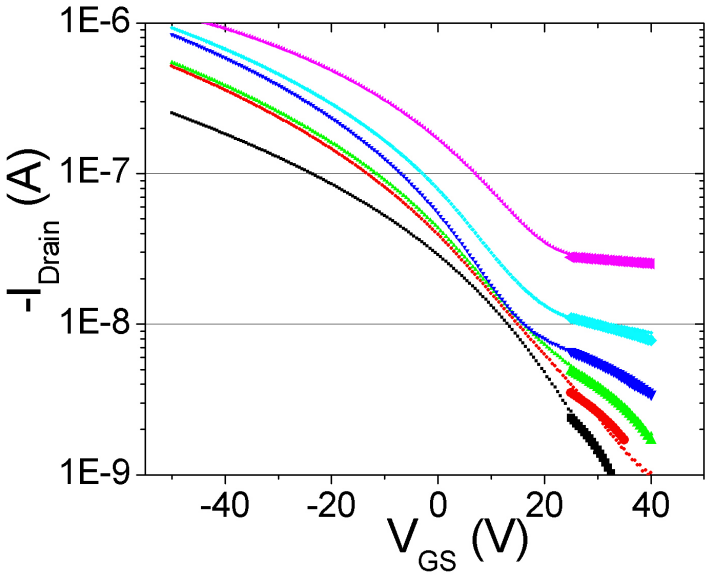

Figure 38: Transfer curves at V_{DS} = -1 V of six *K20* transistors with 12, 21, 39, 53, 88, and 216 nm P3HT thickness. The thick lines from V_{GS} = 25 to 40 V show simulations according to equation 46, with a bulk conductivity of 0.125 nS/μm and N_A of $1.4 \cdot 10^{17} cm^{-3}$.

Figure 38 shows the validity of this model for 6 different P3HT thicknesses over a wide range from 12 to 216 nm. With a bulk conductivity of 0.125 nS/μm, an acceptor concentration value of $N_A = 1.4 \cdot 10^{17} cm^{-3}$ and $\epsilon_{P3HT} = 2$, equation 46 describes the bulk current above the threshold voltage of V_{th} = 25 V accurately. It has to be noted that at the threshold voltage, the bulk current increases linearly with the semiconductor thickness over the entire thickness range. Thus, with thickness increasing beyond the above mentioned 50 nm, where the mobility and the on-current only show slight increase with thickness, the on/off ratio decreases. The point at which the mobility reaches a saturation therefore constitutes an optimum thickness value for transistor performance, combining high charge carrier mobility with reasonably low bulk current.

5.3 Temperature dependence

5.3.1 On-current

Chapter 2.3 presented different models of charge transport in disordered organic semiconductors. According to which mechanism of charge transport is described by the model and how the energetic landscape, in which the transport takes place, looks like in the model, each description predicts a different dependence of the charge carrier mobility. The main parameter that distinguishes the predictions of the models is the dependence of the mobility on the temperature, which was also given in chapter 2.3 for each presented model.

Temperature dependent measurements were performed with *K10* transistors of standard MaDriX samples, which were fixed onto a large copper block in vacuum. The copper block was cooled with liquid nitrogen or heated electrically. While the block with the samples was slowly ($<$ 1 K / min) warming up to room temperature after having been cooled to around 100 K and afterwards was heated from room temperature to 360 K, transfer curves were recorded, from which all relevant parameters were extracted according to equation 38 with charge carrier density dependent mobility as shown in equation 35.

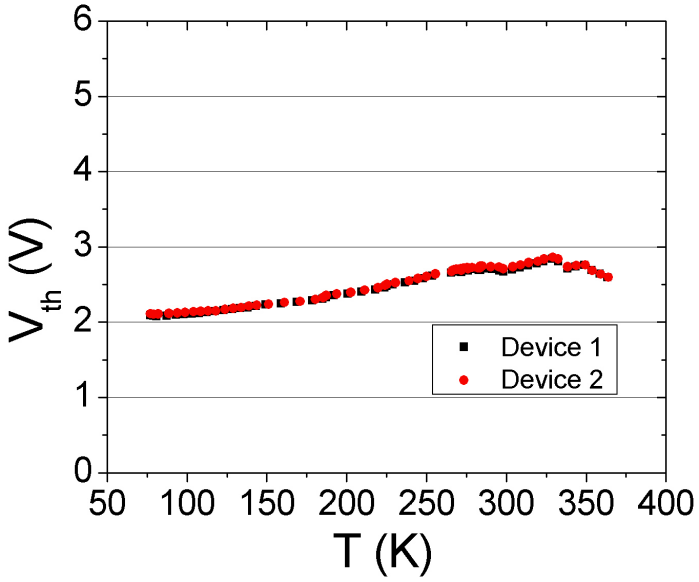

Figure 39: Threshold voltage versus temperature for two samples. Each point corresponds to one temperature, at which a transfer curve was recorded from which the threshold voltage was extracted according to equation 35.

Figure 39 shows the threshold voltage of two transistors on one sample. The variation of the threshold voltage is less than one volt over a temperature range of more than 250 Kelvin. The threshold voltage can thus be considered as a parameter that does not depend on the temperature of the device.

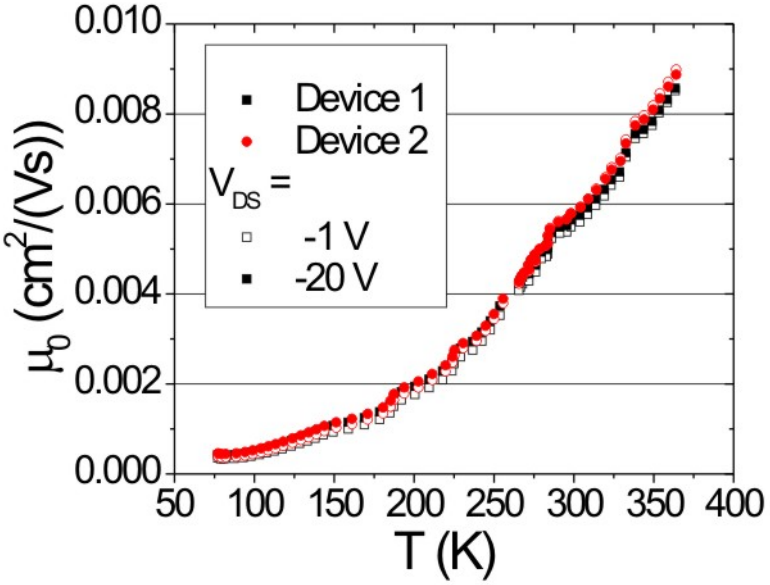

Figure 40: The mobility prefactor μ_0 at V_{aa} = 20 V versus temperature for the same two samples as in figure 39. Empty symbols show the mobility prefactor extracted from transfer curves in the linear regime (V_{DS} = -1 V), the filled ones originate from transfer curves at V_{DS} = -20 V.

The dependence of the charge carrier mobility prefactor μ_0 from equation 35 on temperature is plotted in figure 40, extracted from transfer curves with V_{aa} taken as 20 V. There is no big difference between the two samples considered, and the influence of a factor of 20 in the drain-source voltage is also minuscule. As expected, the mobility strictly monotonically increases with temperature. Unlike in crystalline systems, where band transport is hindered by vibrations, which increase with higher temperature, all models presented in chapter 2.3 predict an increase with temperature, as charge transport is thermally activated. This holds true for the *multiple trapping and release* model, where charges are thermally activated from traps into a transport level, as well as for all descriptions based on hopping, which is a thermally activated process as well.

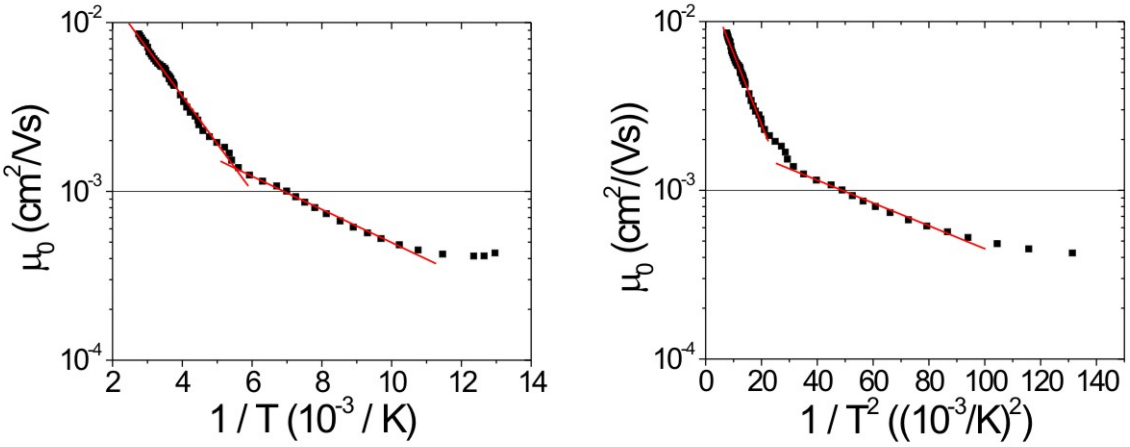

Figure 41: Mobility prefactor μ_0 at $V_{aa} = 20$ V versus temperature as in figure 40, plotted in logarithmic scale over $\frac{1}{T}$ (left) and $\frac{1}{T^2}$ (right). The red lines show linear fits to the curves with the parameters described in the text.

As explained in chapter 2.3, many models predict an $exp\left(-\frac{1}{T}\right)$ or $exp\left(-\frac{1}{T^2}\right)$ dependence of the mobility. To check for such dependencies, the mobility is shown in an *Arrhenius plot*, i.e. in logarithmic scale over $\frac{1}{T}$, in the left part of figure 41, and over $\frac{1}{T^2}$ in the right part. An $exp\left(-\frac{1}{T}\right)$ or $exp\left(-\frac{1}{T^2}\right)$ dependence should then be seen as a straight line.

In both plots, however, the slope is bigger at higher temperature than in the range of low temperatures. One can, however, distinguish two separated regions in which the slope is fairly linear. The corresponding fits are shown as red lines in figure 41. In the left picture, two regions can be fitted, the temperature range above 180 K and the range below 180 K. Below 180 K, the fit follows the expression $\mu_0(T) = 4.8 \cdot 10^{-3} \frac{cm^2}{Vs} \cdot exp\left(-\frac{226K}{T}\right)$ or $\mu_0(T) = 4.8 \cdot 10^{-3} \frac{cm^2}{Vs} \cdot exp\left(-\frac{19.5meV}{k_B T}\right)$, while above 180 K, the mobility can be expressed as $\mu_0(T) = 4.9 \cdot 10^{-2} \frac{cm^2}{Vs} \cdot exp\left(-\frac{648K}{T}\right)$ or $\mu_0(T) = 4.9 \cdot 10^{-2} \frac{cm^2}{Vs} \cdot exp\left(-\frac{55.9meV}{k_B T}\right)$. When applied to the MTR model (see chapter 2.3.1), this means that there are two different kinds of trap states: one with a depth of ca. 20 meV, from which charges are activated at low temperatures, and others with a depth of ca. 56 meV, thermal activation from which dominates at temperatures above 180 K. The "undisturbed" charge carrier mobility, i.e. when all carriers are excited into the conduction band in the limit of very high temperatures, would be $4.9 \cdot 10^{-2} \frac{cm^2}{Vs}$.

The situation is quite similar for the fits to the log μ over $\frac{1}{T^2}$ plot. Below 170 K,

the mobility can be described as $\mu_0(T) = 2.1 \cdot 10^{-3} \frac{cm^2}{Vs} \cdot exp\left(-\left(\frac{125K}{T}\right)^2\right)$ or $\mu_0(T) = 2.1 \cdot 10^{-3} \frac{cm^2}{Vs} \cdot exp\left(-\left(\frac{10.8meV}{k_B T}\right)^2\right)$, above 215 K the dependence is $\mu_0(T) = 1.7 \cdot 10^{-2} \frac{cm^2}{Vs} \cdot exp\left(-\left(\frac{310K}{T}\right)^2\right)$ or $\mu_0(T) = 1.7 \cdot 10^{-2} \frac{cm^2}{Vs} \cdot exp\left(-\left(\frac{26.8meV}{k_B T}\right)^2\right)$.

The mobility variation with temperature can hence be described by both $exp\left(-\frac{1}{T}\right)$ and $exp\left(-\frac{1}{T^2}\right)$ dependences, if the temperature range is divided into two sections. From the plots, no preference can be made for one of those two descriptions. It has to be noted, however, that a separation into two parts with different activation energy and different undisturbed mobility would require not only two different types of trap states, but especially two different transport levels: one with lower carrier mobility into which carriers can be activated even at low temperatures, and one at higher energy, so that carriers can only be activated into it at higher temperatures, and where the charge carrier mobility is about one order of magnitude higher than in the lower transport level. A physical explanation of such a behavior is problematic, and a model that does not require such artificial separation is preferable. In addition, both models do not predict any dependence of the mobility on the charge carrier concentration and therefore do not provide an appropriate description of the measurement.

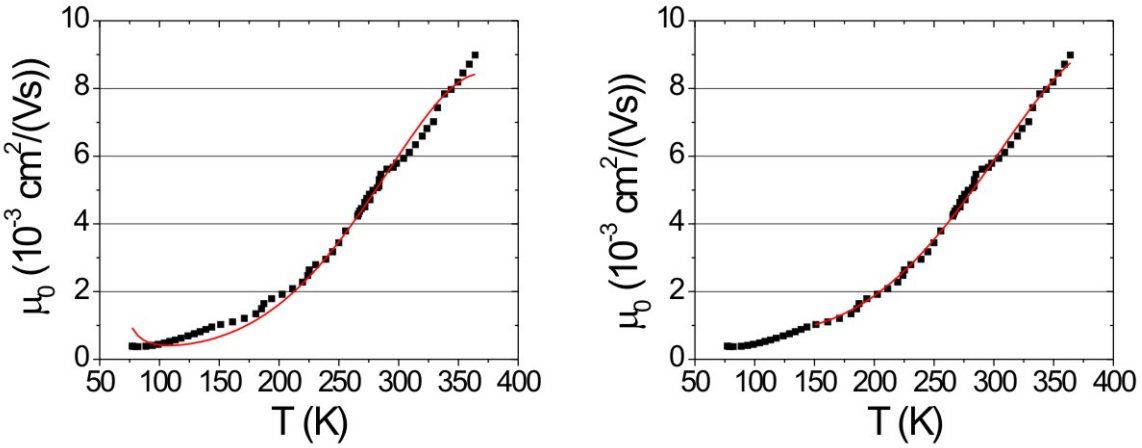

Figure 42: Mobility prefactor μ_0 at $V_{aa} = 20$ V versus temperature. The red lines show fits according to equation 15 (Vissenberg-Matters model) over the entire temperature range (left) and for T > 150 K (right).

Charge carrier density dependent mobility is included in the model of hopping transport in an exponential density of states by Vissenberg and Matters (chapter 2.3.3), with which transfer curves at one certain temperature can be fitted successfully (see section 5.1). Equation 15 describes the dependence of the charge carrier mobility μ on temperature and gate voltage, which is connected to the carrier density, according to this model. The red line in the left graph of figure 42 shows a fit according to this equation over the entire temperature range, with $\sigma_0 = 3.1 \cdot 10^4 \frac{S}{m}$, $T_0 = 444$ K and the localization length $a^{-1} = 0.80$ nm. The fit can follow the curve moderately, with deviations mainly in the low-temperature regime. In their development of the percolation description, Vissenberg and Matters assume that $s_c k_B T >> k_B T_0$, where s_c is the exponent of the critical percolation conductance. Thus the description is not valid at very low temperatures. The right graph shows a fit to the mobility curve, starting at 150 K. With this restriction, the fit can reproduce the curve very well, with the fitting parameters $\sigma_0 = 2.3 \cdot 10^4 \frac{S}{m}$, $T_0 = 479$ K and $a^{-1} = 0.90$ nm. While this value of T_0 is in the range of values found in litterature (e.g. 425 K in polythiophene [44], 385 and 380 K in pentacene and PTV ([26] on data from [86])), the localization length determined from the measurements presented here is way higher (cf. 0.16, 0.22 and 0.08 nm in the same references). This is the reason for the comparably low variation of the charge carrier mobility, which varies by less than two orders of magnitude from 100 to 360 K, compared to 3 to 5 orders of magnitude in reference [26].

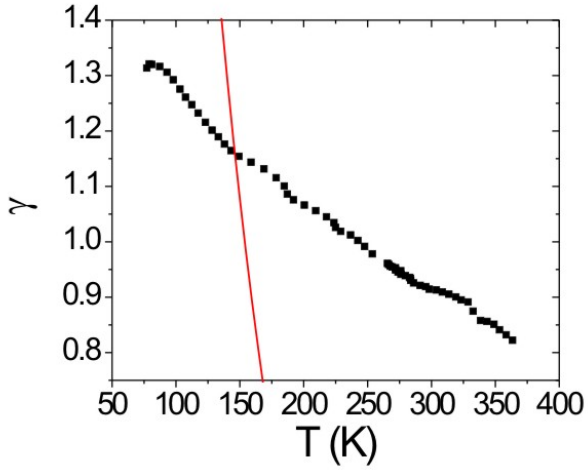

Figure 43: Mobility exponent γ versus temperature. The red line shows the best possible fit for $\gamma = 2\left(\frac{T_0}{T} - 1\right)$.

Although the temperature dependence of the mobility can well be described by equation 15, this does not hold true for the temperature dependence of the moblity dependence on charge carrier concentration, expressed by the exponent γ in equation 35. According to equation 15, γ would be equal to $2\left(\frac{T_0}{T}-1\right)$. This would imply a huge variation of γ from 7.6 to 0.66 from 100 to 360 K, whereas figure 43 shows the determined γ values from the transfer curves with varied temperature, which only vary from 1.3 to 0.8. For this reason, the parameters determined in the fit in the right part of figure 42 cannot retract the entire field of transfer curves for all temperatures. In order to do this, a variation of the T_0 parameter with temperature has to be assumed. Figure 44 shows how this fit parameter, determined from individual fits to each single transfer curve, varies with temperature.

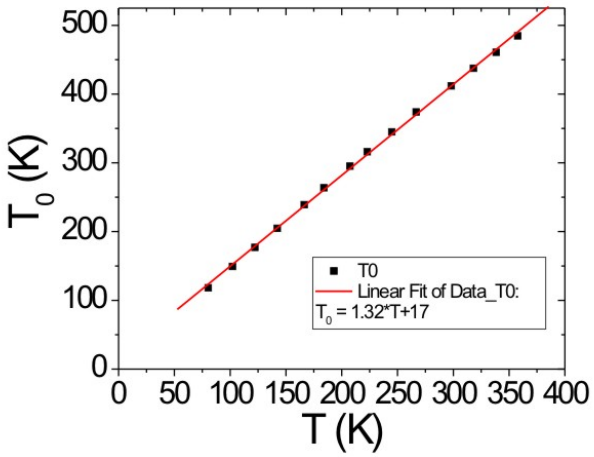

Figure 44: Fit parameter T_0 as determined from single transfer curves, plotted over the temperature at which the transfer curves were recorded. The red line shows a linear fit to the curve.

The fit parameter T_0 increases linearly with the temperature at which the transfer curve was recorded. The fit gives the relation of $T_0 = 1.32T + 17K$. Thus instead of $2\left(\frac{T_0}{T}-1\right)$ as predicted by Vissenberg and Matters, γ is described as $2\left(\frac{17K}{T}+0.32\right)$. Such a deviation can be due to a difference in the shape of the density of states, which does not follow a purely exponential relation. With this modification done, the temperature dependence of the transistor parameters in this investigation on top-gate P3HT samples is modeled very well by the Vissenberg-Matters model.

The model by Limketkai et al., introduced in chapter 2.3.4, extends the Vissenberg-Matters model by an additional dependence of the charge carrier mobility on the electric

field applied to the channel. The black points in figure 45 show the mobility μ_0 at V_{aa} = 20 V determined by transfer curves with a drain voltage of V_{DS} = -1 V, whereas the red points show the mobility values from the V_{DS} = -20 V transfer curves. The black line is the fit to the black points, and the red line shows the prediction of the Limketkai model for the mobility at a 20 times increased drain field, i.e. at V_{DS} = -20 V. The graph shows clearly that the measured mobility at V_{DS} = -20 V (F = 2 $\cdot 10^6 \frac{V}{m}$) hardly differs from that at V_{DS} = -1 V (F = 1 $\cdot 10^5 \frac{V}{m}$) and stays far lower than the prediction of the Limketkai model for V_{DS} = -20 V. The observed field dependence of the mobility is thus much smaller than the description by Limketkai, and the Vissenberg-Matters description without any mobility dependence on the field reproduces the measurement much better than the Limketkai model.

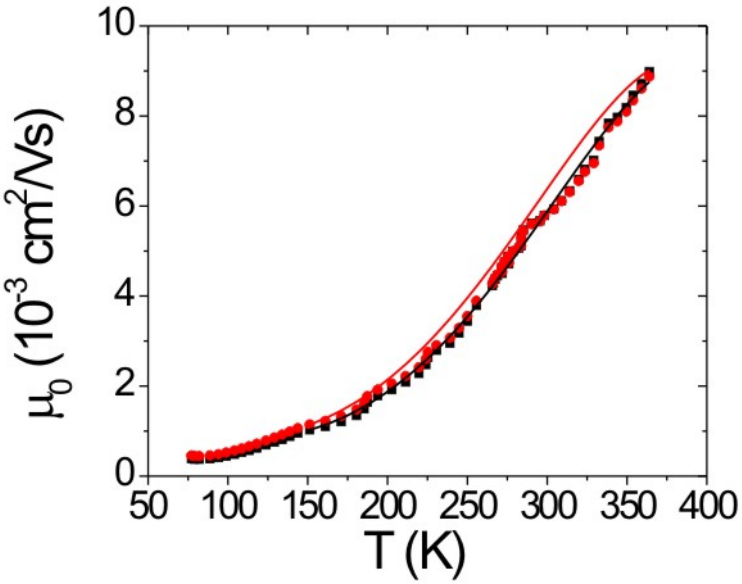

Figure 45: Charge carrier mobility μ_0 at V_{aa} = 20 V extracted from transfer curves recorded with V_{DS} = -1 V (black points) and with V_{DS} = -20 V (red points) plotted over temperature. The black line shows a fit to the V_{DS} = -1 V curve according to Limketkai's model, for T > 150 K. The fit parameters are: $\sigma_0 = 2.3 \cdot 10^4 \frac{S}{m}$, T_0 = 480 K, a^{-1} = 0.90 nm, F = 100 000 $\frac{V}{m}$ (fixed). The red line shows the prediction for F = 2 000 000 $\frac{V}{m}$ with otherwise the same parameters.

5.3.2 Off-current

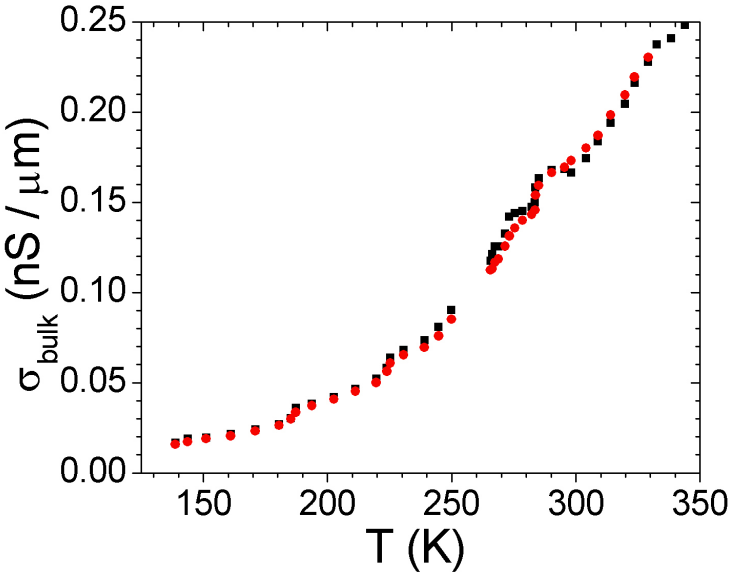

Figure 46: Bulk conductivity σ_{bulk} plotted over the temperature. The black points show the values determined by a fit to the bulk current (V_{GS} = +2 to +4 V) of the transfer curves taken at each temperature, according to equation 46. The red points are calculated values according to equation 49, with μ_0 and γ extracted from the transfer curve fits at each temperature, h = 0.8 nm and $N_A = 0.85 \cdot 10^{17}\ cm^{-3}$, the value also determined in the fits for the black points.

After examining how the on-current varies with temperature, it is now interesting to investigate the behavior of the off-current, above the threshold voltage. It was demonstrated in section 5.2.5 that for different semiconductor thicknesses, the behavior of the off-current can be described well by equation 46, which describes the behavior as a function of the dopant concentration N_A and the bulk conductivity σ_{bulk}. The black points in figure 46 show the dependence of this bulk conductivity σ_{bulk} on temperature, determined for each temperature by a fit to the transfer curve with the threshold voltage determined from the overall fit of the curve. It is obvious that this determined temperature dependence resembles the temperature dependence of the mobility. Given that the charge carrier mobility is dependent on the charge carrier density as described by equation 35, one can calculate the mobility for each carrier concentration. Assuming that the mobility of the bulk carriers is equal to the mobility of the channel carriers, the charge carrier mobility for the bulk carrier concentration, which equals the acceptor

concentration N_A, can then be calculated as:

$$\mu(n) = \mu_0 \cdot \left(\frac{n}{n_0}\right)^{\gamma} \Rightarrow \mu(N_A) = \mu_0 \cdot \left(\frac{N_A}{n_0}\right)^{\gamma} \tag{47}$$

with n_0 the charge carrier concentration at $V_{GS} - V_{th} = V_{aa}$:

$$n_0 = \frac{C_i V_{aa}}{he} \tag{48}$$

where h is the (effective) height of the transistor channel.

With this relation, the bulk conductivity can be described as follows:

$$\sigma_{bulk} = \mu \cdot n \cdot q = \mu_0 \left(\frac{N_A}{\left(\frac{C_i V_{aa}}{he}\right)}\right)^{\gamma} \cdot N_A \cdot e \tag{49}$$

The red points in figure 46 show calculated values for σ_{bulk} according to this relation, with μ_0 and γ values taken from the fits to the on-current of the transfer curve at each temperature. Good agreement with the σ_{bulk} values from fits to the off-regime can be stated.

The bulk current remaining at the threshold voltage can hence be described by the conductivity that results from the acceptor concentration N_A and the mobility that is expected for this carrier concentration from the transfer curve. With this conductivity, the bulk current is determined with the drain-source voltage, the channel width and length, and the whole semiconductor thickness. With further increased gate voltage, this thickness (and with it the current) is reduced by the depletion width as described in section 5.2.5 with equations 44 and 46. One major consequence of this behavior is that the off-current has a very similar temperature dependence to the on-current, which means that the on/off ratio of the transistors does not change significantly upon temperature variation.

5.4 Threshold voltage tuning with the insulator solvent

For the optimization of organic semiconductors in devices like organic field-effect transistors, research is mainly focused on high charge carrier mobility [87] [88] for high current levels [89] and high switching speeds [90] [51], the compatibility with low-cost and large-area production techniques [91], or thermal [92] and long-time stability [93]. However, an important figure of merit in many applications, the on/off ratio of the

transistor, depends crucially on the threshold voltage. In order to use OFETs as a switching device in low-voltage circuits, a reasonable low gate voltage V_{on} is needed to turn on the device and usually a gate voltage V_{off} of 0 Volt is assumed to turn it off. For these settings a threshold voltage close to zero is of crucial importance. While a high negative (in the p-type case) threshold voltage results in low on-currents or high operation voltages, a positive threshold voltage dramatically increases the off-current at zero gate voltage, thus deteriorating the on/off-ratio.

The origin of the threshold voltage is closely related to charges present in the insulator or at the insulator/semiconductor interface [94] [95]. When trap states exist at this interface, charges induced by the gate field first fill these traps, and a high negative voltage is necessary until finally charges can be accumulated in the transistor channel. On the other hand, if charges are present in the channel even at zero gate field, a positive threshold voltage is necessary to deplete the channel and turn the transistor off, resulting in undesirable high current at $V_{GS} = 0$. The same applies to high bulk currents as described above in section 5.2.5. As already demonstrated in chapter 4.3, the choice of the insulator solvent which is applied onto the semiconductor can have a large effect on the threshold voltage. Similarly, the threshold voltage is also very sensitive to the exposure of the semiconducting layer to acids or bases, which can result in embedded additional charges in the transistor. In the following, shifting the threshold voltage is investigated in two ways. The first option is to expose the semiconducting layer of a bottom-gate structure directly to acidic or basic fluids for a short period of time. The second option concerns again top-gate devices, with a study on how the chemical composition of the insulator solvent affects the threshold voltage of the buried semiconducting channel.

The bottom-gate and bottom-contact device was produced on highly n-doped silicon wafers with 58 nm thick thermally grown silicon oxide as gate dielectric. The silicon serves as the gate electrode. Onto the oxide, 20 nm thick source and drain electrodes, consisting of gold with a 3 nm titanium adhesion layer underneath, were patterned by optical lithography. Both metals were thermally evaporated onto the substrates. For the reduction of trap states at the insulator / semiconductor interface and for better ordering of the organic molecules, a monolayer of hexamethyldisilazane (HMDS) was vapor-grown on the surface after cleaning with piranha solution and before the deposition of a thin film ($\approx$ 10 nm) of *Sepiolid PX MaDriX* as semiconductor, spin-coated from solution in toluene. Spin-coating, as well as all further treatments and the electrical measurements, took place in a glovebox in nitrogen atmosphere. As plastic substrates for the top-gate transistors, standard MaDriX samples were used, with 30 nm of *Sepiolid PX MaDriX* spin-coated from solution in toluene and *PolyIC insulator* with a layer thickness of 350 nm. Both spin-coating steps were carried out in open air with room temperature solutions. As top gate electrode, 100 nm gold was

sputter-coated through a shadow mask.

5.4.1 Bottom-gate samples on silicon substrates

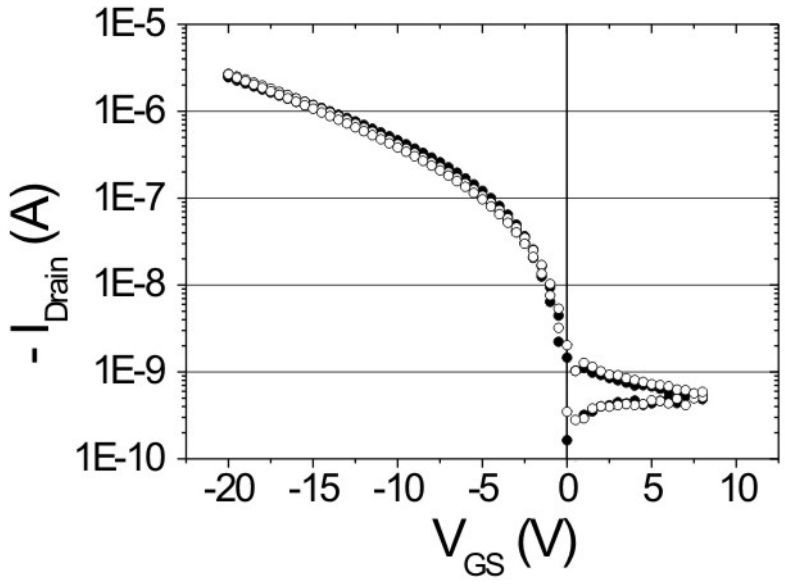

Figure 47: Transfer curves of a bottom-gate transistor measured in forward (V_{GS} = +10 to -20 V) and reverse direction (-20 to +10 V). The black points show the measurement before contact to *solvent 4*, the white circles the measurement thereafter (see text). L = 50 μm, W/L = 400, d_{ox} = 58 nm, V_{DS} = -20 V.

Figure 47 shows the transfer curve of a transistor on silicon substrate, with a channel length L of 50 μm and a W/L ratio of 400 at a drain-source voltage of -20 Volts. The mobility at V_{GS} = -20 V is determined to be $9 \cdot 10^{-4}$ $\frac{cm^2}{Vs}$ and the threshold voltage is at + 0.3 V. γ is around 3 in all the measurements, a high value which is typical for very thin P3HT films (see chapter 5.2.2). The on/off ratio, if defined again as the ratio between the on drain current at V_{GS} = -20 V and the off current at V_{GS} = 0 V, is 1700. The hysteresis is negligible in the regime where the transistor is turned on, as the measurement was carried out in a glovebox, under exclusion of oxygen and humidity. To check for any influence of the insulator solvent used in the top-gate devices on P3HT, pure *solvent 4* without anything dissolved in it was spin-coated on the P3HT layer. As seen in figure 47, the transfer characteristics of the device remain almost

unaffected: The charge carrier mobility is just slightly improved to $1.2 \cdot 10^{-3}$ $\frac{cm^2}{Vs}$ and the threshold voltage shifted minimally upwards by + 0.1 V to now 0.4 V. The on/off ratio slightly decreased to now 1320.

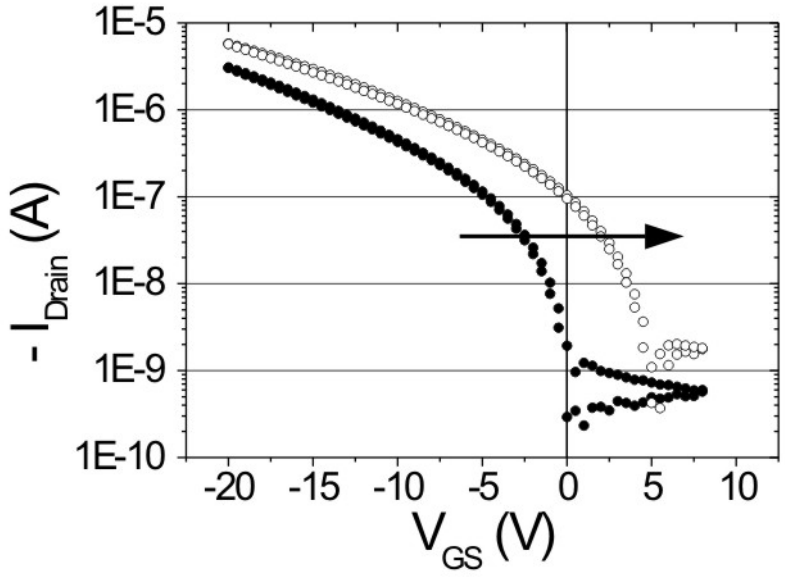

Figure 48: Transfer curves of the same transistor as in figure 47, measured in forward (V_{GS} = +10 to -20 V) and reverse direction (-20 to +10 V). The black points show the measurement before contact to *solvent 4* with 10 vol-% of an acid added, the white circles the measurement thereafter (see text). L = 50 μm, W/L = 400, d_{ox} = 58 nm, V_{DS} = -20 V.

To investigate the effect of acid on the OFET characteristics with focus to changes in the threshold voltage, *solvent 4* was spin-coated again on top of the P3HT layer, but this time with addition of 10 vol-% of an acid. The result can be seen in figure 48: The threshold voltage was shifted by almost 5 volts in the positive direction, to now + 5.3 V. This has a dramatic effect on the on/off ratio, i.e. it lowers the on/off ratio from far more than 1000 down to no more than just 55. The mobility at V_{GS} = -15 V, i.e. at the same distance to the threshold voltage as before, remains completely unaffected at $1.2 \cdot 10^{-3}$ $\frac{cm^2}{Vs}$.

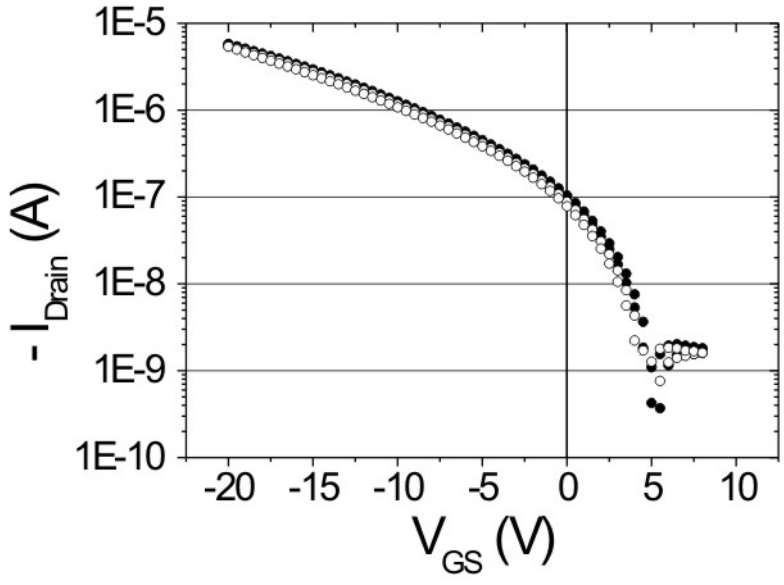

Figure 49: Transfer curves of the same transistor as in figures 47 and 48, measured in forward (V_{GS} = +10 to -20 V) and reverse direction (-20 to +10 V). The black points show the measurement before contact with water, the white circles the measurement thereafter (see text). L = 50 μm, W/L = 400, d_{ox} = 58 nm, V_{DS} = -20 V.

As shown in figure 49, pure water does not have any effect on the transistor characteristics: After covering the P3HT surface with water for one minute, the mobility as well as the threshold voltage remain completely unchanged. In order to test if the threshold shift can be reversed by exposing the P3HT surface to a basic liquid, the transistor was then covered with a 25% aqueous solution of ammonium hydroxide for one minute. While the mobility still remained at $1.2 \cdot 10^{-3}$ $\frac{cm^2}{Vs}$, the transfer curve in figure 50 shows impressively that the threshold voltage was more than recovered, and the on/off ratio rose from 55 to 2600!

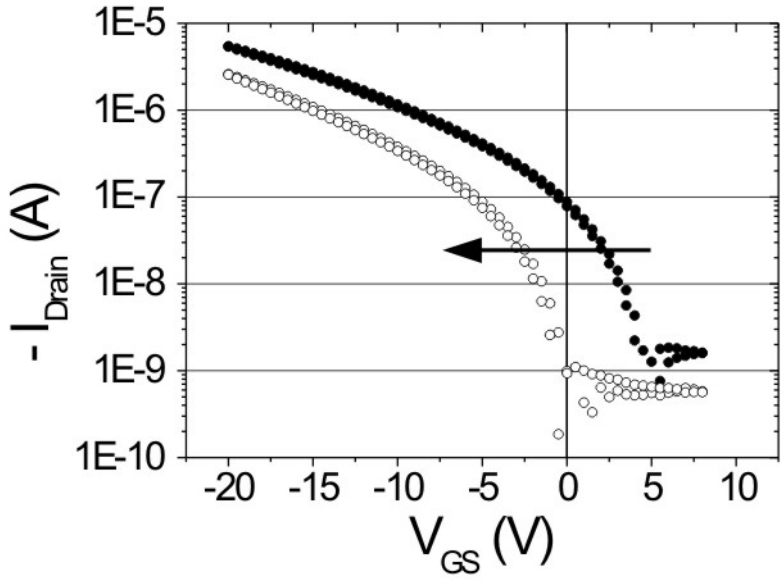

Figure 50: Transfer curves of the same transistor as in figures 47 to 49, measured in forward (V_{GS} = +10 to -20 V) and reverse direction (-20 to +10 V). The black points show the measurement before contact with ammonium hydroxide solution, the white circles the measurement thereafter (see text). L = 50 μm, W/L = 400, d_{ox} = 58 nm, V_{DS} = -20 V.

These results clearly show the strong effects of acids and bases on the threshold voltage. While acid provokes a threshold voltage shift towards more positive values, more negative gate voltage can be achieved by the impact of basic solution on the transistor channel. Pure water alone does not affect the threshold voltage. The same applies to *solvent 4*, the solvent used for the insulator in top-gate devices.

5.4.2 Samples on plastic substrates

All results in the following section represent the statistical average of at least 10 *K10* transistors fabricated in a single process on the same substrate. All transfer curves were again fitted according to gate-voltage dependent charge carrier mobility with additional bulk current, as described by equation 38. As the threshold voltages in all measurements were close to 0 and the transfer curves measured to V_{GS} = -20 V, V_{aa} was chosen as 20 V in the entire analysis.

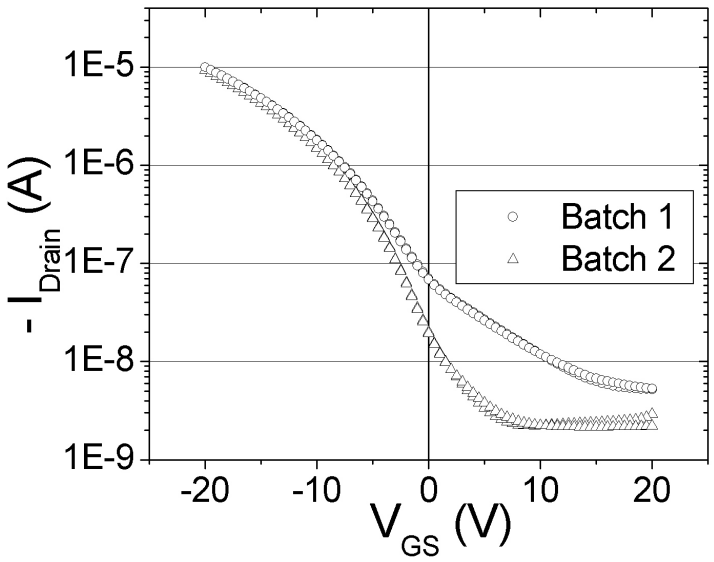

Figure 51: Average transfer curves from two top-gate samples measured in forward (V_{GS} = + 20 to - 20 V) and reverse direction (-20 to +20 V). The circles show a transistor from sample 1 in the table of figure 52 with insulator prepared from solution in *solvent 4*, batch 1, the triangles a transistor from sample 2 with insulator prepared from solution in *solvent 4*, batch 2 (see text). L = 10 μm, W/L = 1000, $d_{insulator}$ = 350 nm, V_{DS} = - 20 V.

Sample no.	Description	μ_0 (10^{-3} cm^2/Vs)	V_{th} (V)	γ	R_{bulk} (GΩ)	on/off
1	Batch 1	5.0	3.3	1.07	2.8	157
2	Batch 2	6.0	1.3	0.85	7.7	356
3	Batch 2 with 100 ppm acid	5.2	3.4	1.01	2.3	174
4	Batch 2 with 0.2 vol-% acid	4.7	4.1	1.15	2.1	91
5	Batch 1 with 0.2 vol-% NH_4OH solution	6.1	3.3	0.99	4.7	161
6	Batch 1 with 0.4 vol-% solvent 5	5.5	2.2	0.95	3.7	251
7	Batch 2 with 0.4 vol-% solvent 5	6.4	1.5	0.87	10.6	489
8	Batch 1 (P3HT P 200)	2.2	11.0	1.62	0.43	32
9	Batch 2 (P3HT P 200)	2.2	5.5	1.17	2.4	100

Figure 52: Average transistor values of the samples mentioned in the text. Data determined from fits to transfer curves at V_{DS} = - 20 V according to charge carrier density dependent mobility with V_{aa} = 20 V. The on/off ratio is the ratio of the drain current at V_{GS} = - 20 V and the drain current at V_{GS} = 0.

Figure 51 shows average transfer curves of two transistors (samples 1 and 2 in the table of figure 52) principally prepared in the same way. The only difference is, that a different batch of the same insulator solvent (*solvent 4*) from the same manufacturer was used. While solvent batch 1 yields transistors with an average threshold voltage of 3.3 V and R_{bulk} of 2.8 GΩ, transistors prepared using solvent batch 2 show improved characteristics of V_{th} = 1.3 V and R_{bulk} = 7.7 GΩ. The average on/off ratio, defined again as the ratio between the on current at V_{GS} = - 20 V and the off current at V_{GS} = 0 V, is therefore increased from 140 to more than 380! At the same time, the transfer curves from sample 2 are less curved than those of sample 1, with an average gamma of 0.85 instead of 1.07.

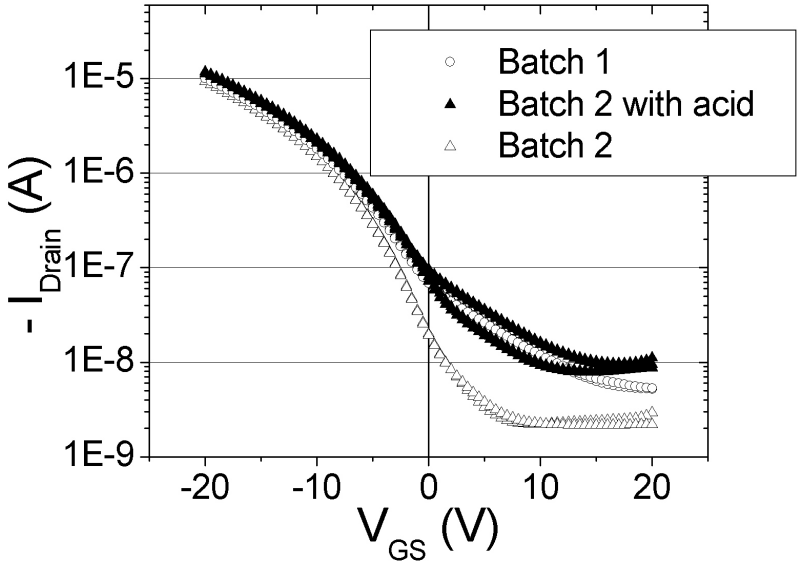

Figure 53: Average transfer curves from four top-gate samples measured in forward (V_{GS} = +20 to -20 V) and reverse direction (-20 to +20 V). The open symbols show the transistors from figure 51, from samples 1 and 2, the full triangles show two transistors with insulator prepared from solution in *solvent 4*, batch 2 with 100 ppm (sample 3) and 0.2 vol-% (sample 4) of an acid added, respectively (see text). L = 10 μm, W/L = 1000, $d_{insulator}$ = 350 nm, V_{DS} = -20 V.

To demonstrate how even small variations in the insulator solvent composition can be responsible for such big effects, 100 ppm of an acid (more details in [43]) was added to solvent batch 2 upon the preparation of sample 3. This little addition of acid is sufficient to switch the behavior to that of sample 1 whose insulator was spin-coated from a solution in batch 1 (see figure 53 and the table of figure 52). As can be seen in the table of figure 52, this sample 3 is almost identical with sample 1 in mobility, threshold voltage, bulk current, gamma and on/off ratio. Even an extensively further increase of the acid concentration in the solvent upon the preparation of sample 4 amplifies this trend just very slightly.

In order to invert this effect, 0.2 vol-% of 25% ammonium hydroxide solution was added to the *solvent 4* upon the preparation of sample 5 with solvent batch 1. Although this hardly affects the threshold voltage, the bulk current could be decreased, with R_{bulk} increasing from 2.8 GΩ to 4.7 GΩ (figure 54). But the good characteristics of sample 2 could not be achieved in this way.

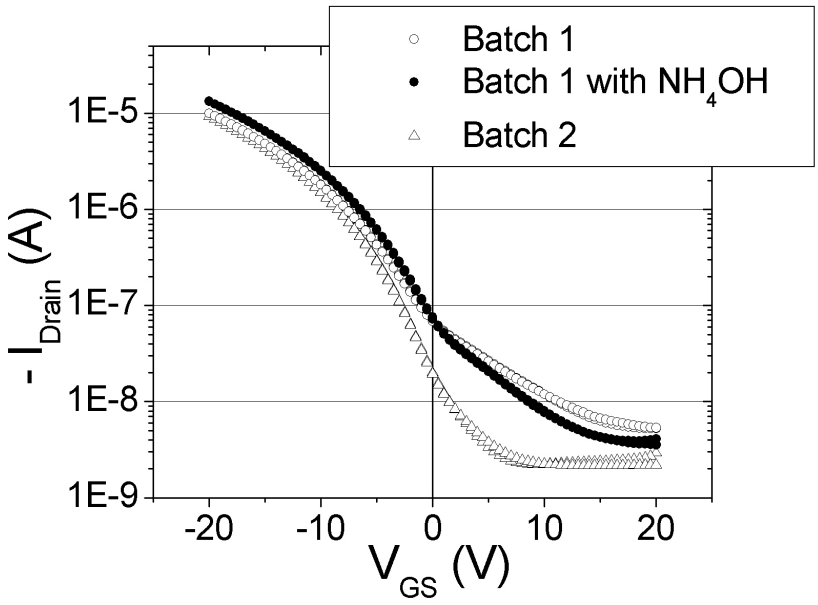

Figure 54: Average transfer curves from three top-gate samples measured in forward (V_{GS} = +20 to -20 V) and reverse direction (-20 to +20 V). The open symbols again show the transistors from sample 1 and 2, with insulator prepared from solution in *solvent 4*, batch 1 and 2, the full circles a transistor with insulator prepared from solution in *solvent 4*, batch 1 with 0.2 vol-% ammonium hydroxide solution added (sample 5, see text). L = 10 μm, W/L = 1000, $d_{insulator}$ = 350 nm, V_{DS} = -20 V.

However, *solvent 4* is in a chemical equilibrium with the acid used as additive for sample 3 and 4 and another organic solvent (*solvent 5*). The reaction equation can be found in [43]. The amount of acid present in the substance should thus decrease upon the addition of *solvent 5*. Therefore, a small amount of 0.4 vol-% of this solvent was added to the *solvent 4* batches 1 and 2 upon the preparation of gate insulator layers for samples 6 and 7.

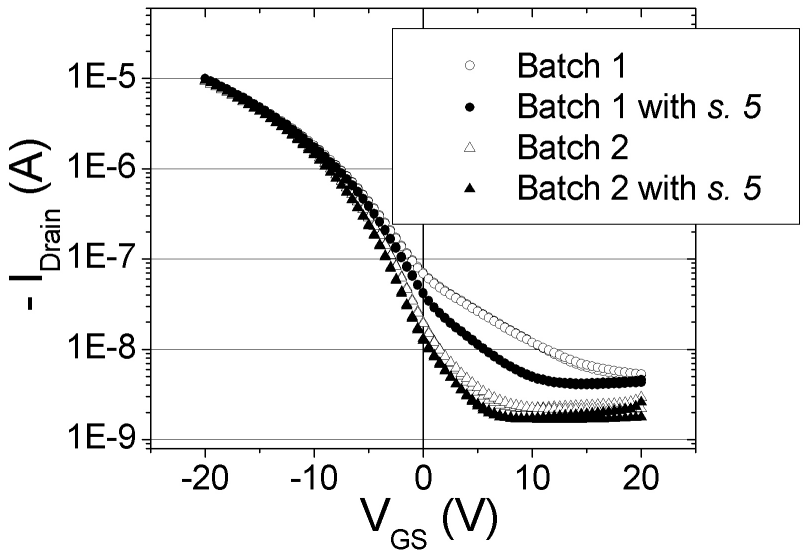

Figure 55: Average transfer curves from four top-gate samples measured in forward (V_{GS} = +20 to -20 V) and reverse direction (-20 to +20 V). The empty symbols show the transistors from figure 51, with their insulators prepared from solutions in the two different *solvent 4* batches, the full symbols show transistors with insulators prepared from solutions in the same batches with 0.4 vol-% of *solvent 5* added (see text). L = 10 μm, W/L = 1000, $d_{insulator}$ = 350 nm, V_{DS} = -20 V.

The average transfer curves shown in figure 55 demonstrate that the qualities in the off regime of the transistors made with solvent batch 1 were indeed considerably improved by this chemical modification. The threshold voltage was shifted from an average 3.3 V by more than one volt to 2.2 V, and the bulk resistance increased from 2.8 to 3.7 GΩ (see the table of figure 52). With these changes, the average on/off ratio is increased from 160 to 250. Gamma is decreased as well, from 1.07 to 0.95. Even the better solvent batch 2 could be slightly further improved, with the average bulk resistance reaching 10.6 GΩ. Thus the addition of *solvent 5* to the insulator solvent raises the average on-off ratio from 380 to 490.

In order to assure that this phenomenon is more general and not just specific to the chosen P3HT, the more than 98% regio-regular P3HT *Sepiolid P 200* (see chapter 4.2.1) was used for the same experiment. Due to the high regio-regularity, in the same layer thickness the current is highly increased in comparison to the less regular P3HT. The threshold voltage, however, is more positive and therefore the off-current at V_{GS} = 0 much higher, resulting in lower on/off ratios.

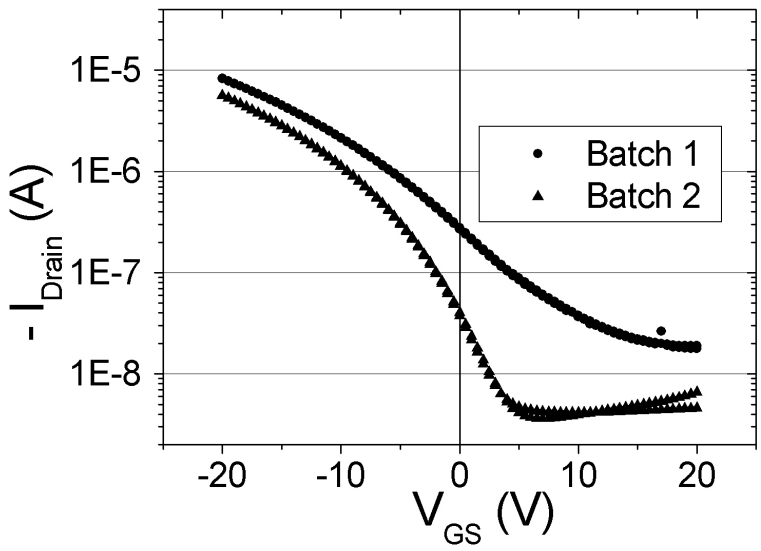

Figure 56: Average transfer curves from two top-gate samples with highly regio-regular P3HT, measured in forward (V_{GS} = +20 to -20 V) and reverse direction (-20 to +20 V). The circles show a transistor with insulator prepared from solution in *solvent 4*, batch 1 (sample 8), the triangles a transistor with insulator prepared from solution in *solvent 4*, batch 2 (sample 9, see text). L = 10 μm, W/L = 1000, $d_{insulator}$ = 350 nm, V_{DS} = -20 V.

Figure 56 shows average transfer curves taken from two devices prepared with a 30 nm layer of this extremely regio-regular P3HT, applied from solution in chloroform, and the same insulator prepared in the same way as described above, again dissolved in batches 1 (sample 8) and 2 (sample 9) of *solvent 4*. The same effects are visible, with the transistors made from batch 1 having higher threshold voltage (11.0 instead of 5.5 V) and lower bulk resistance (0.4 instead of 2.4 GΩ) than those made from batch 2, significantly decreasing the on/off ratio from 100 to 30 and increasing gamma from less than 1.2 to more than 1.6. But in this case it was also possible to reach improved values by adding *solvent 5* to the insulator solution, which shifted e.g. the threshold voltage of the transistors prepared with batch 2 from 5.5 to 3.7 V.

5.4.3 Conclusion

In an organic field-effect transistor, the conducting channel in the semiconductor is quite thin and formed directly at the interface to the gate insulator. Studies on well-

ordered oligothiophenes, which grow in layer-by-layer mode, show that this channel is no thicker than just two monolayers [96]. And also for less ordered systems like P3HT it has been shown that the charge transport takes place in a channel close to the interface, as also confirmed in chapter 5.2. Therefore the morphological and electronic nature of the interface has a major impact on the transistor characteristics. It is therefore clear that in top-gate devices as those investigated here, the nature of the gate insulator, which is deposited directly on the surface of the semiconductor, which will become the conducting channel, has a big influence on the transistor properties. The results shown above demonstrate that even small modifications of the chemical composition of the insulator solvent have considerable impact on the transistor characteristics.

When the semiconductor gets into contact with an acidic liquid, the free protons from the acid provoke increased doping of the P3HT, creating additional holes at zero field. Holes which are created deeper in the layer increase the bulk current which is still present at more positive gate voltages than the threshold. And the additional holes close to the interface provoke that already at more positive gate voltage, a conducting channel is formed, which means that the threshold voltage is shifted to more positive values. The additional states also cause a broadening of the density of trap states, reflected in the higher value of γ that accompanies the shifts to higher bulk current and more positive threshold. The sensitivity of all these parameters, combined in shifting on/off ratio, is very high even to small variations of the insulator solvent composure. Therefore the changes in the transfer characteristics allow to detect solvent ingredients with concentrations in the ppm regime, where even high-tech chemical analysis tools reach their limit of sensitivity.

It is demonstrated how the threshold voltage of organic field-effect transistors on silicon can be shifted by contact of the semiconductor to acid or base. In top-gate devices, with an organic insulator deposited from solution in *solvent 4*, a solvent well suited due to its low impact on the semiconductor, small amounts of acid in the solvent have big impact on the transistor characteristics. While addition of acid to the solvent in the ppm regime shifts the threshold voltage towards more positive values, addition of another organic solvent shifts the chemical equilibrium towards less acid in the solvent. Transistors with insulator prepared from such solutions exhibit a threshold closer to zero, less residual current in the off-regime above the threshold, and less dependence of the mobility on the charge carrier concentration, due to a narrower distribution of hopping states. Thus the transistor qualities can be tuned by small additions to the insulator solvent, namely the on/off ratio can be largely improved, and the transistor characteristics are shown to be a very sensitive tool for the detection of solvent impurities.

6 Frequency Prediction from DC Parameters

6.1 Introduction

After the extensive description of a large variety of charge transport aspects in the previous chapter, the last chapter of this thesis is dedicated to the question of the switching frequency that can finally be achieved with OFETs in an organic circuitry. The chapter also addresses questions of device geometry and contact resistance, and develops a complete model of the transition frequency including these effects. High switching speeds are of crucial importance for almost any kind of OFET application, as higher frequencies in AC setups open up new fields of applications: While frequencies in the kHz range are sufficient for simpler applications such as electronic paper, more sophisticated circuits like for radio frequency identification (RFID) tags or active-matrix displays require switching frequencies in the MHz range [97]. Despite this importance of AC qualities and especially high frequencies, DC measurements are most often used for OFET characterization and optimization. This chapter investigates to what extent the AC characteristics of organic transistors like the transition frequency f_T can be predicted from these DC characteristics.

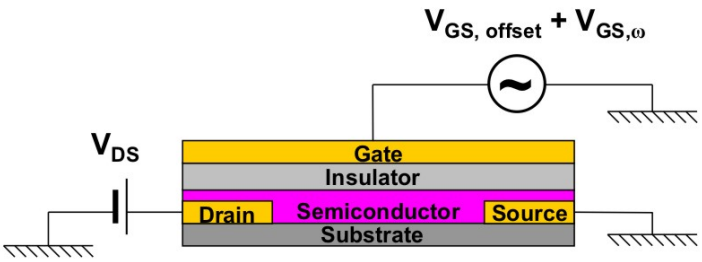

Figure 57: Schematic picture with the AC voltage applied to the gate electrode and the DC voltage applied to the drain of the standard transistor also used for the frequency investigations. The source is grounded. The substrate is PET foil, with *MaDriX P3HT* as the semiconductor and *PolyIC insulator* as gate insulator. All contacts are made from gold.

For the frequency investigations, *K10* transistors from standard MaDriX samples were chosen. In all AC measurements, an AC voltage with DC offset was applied to the gate by a 33220 Agilent waveform generator while DC voltages were applied to the drain. The source electrode was always grounded (see figure 57).

6.2 Theory and Results

In the linear regime ($|V_{DS}| << |V_{GS} - V_{th}|$), the drain current of a p-channel FET is described by the gradual channel approximation as

$$I_D = -\frac{W}{L}\mu C_i V_{DS}\left(V_{GS} - V_{th}\right) \tag{50}$$

with the charge carrier mobility μ, the specific insulator capacitance per area C_i, and the threshold voltage V_{th} (see chapter 2.1). Upon application of an AC gate voltage, the drain current from equation 50 is changed to

$$I_D = -\frac{W}{L}\mu C_i V_{DS}\left(V_{GS,offset} - V_{th} + V_{GS,\omega}\right) - i\omega C_{GD} V_{GS,\omega} \tag{51}$$

with the DC component $V_{GS,offset}$ and the AC component $V_{GS,\omega}$ of the gate-source voltage. The second contribution, independent of the drain voltage and proportional to the frequency of the AC voltage, occurs due to the capacitance C_{GD} of the insulator between the gate and the drain electrode. It consists of the direct capacitance $C_{GD,0}$ between the electrodes themselves, and (again in linear regime) half of the channel capacitance C_{Ch}:

$$C_{GD} = C_{GD,0} + \frac{1}{2}C_{Ch} = C_i\left(A_{GD,0} + \frac{1}{2}W \cdot L\right) \tag{52}$$

where $A_{GD,0}$ is the overlap area between gate and drain (see figure 58).

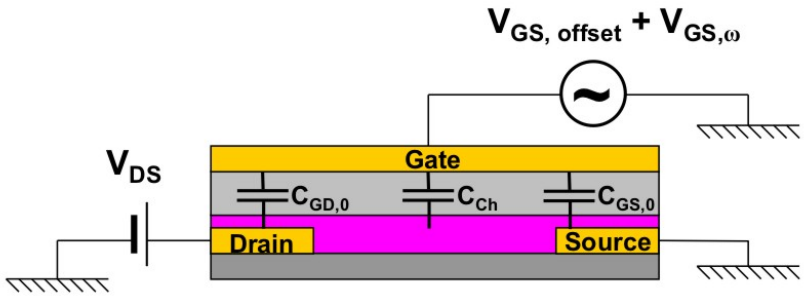

Figure 58: Capacitances occurring in the OFET.

So the AC component is described as

$$\tilde{I}_{D,\omega} = -\frac{W}{L}\mu C_i V_{DS} V_{GS,\omega} - i\omega C_{GD} V_{GS,\omega} \tag{53}$$

It has to be noted that the current does not depend directly on $V_{GS,offset}$ and is thus constant for all $V_{GS,offset} < V_{th}$ in well-ordered systems with constant charge carrier mobility. In disordered systems like P3HT however, where the mobility is a function of the gate-source voltage (see equation 16), $\tilde{I}_{D,\omega}$ increases with increasing, i.e. more negative, $V_{GS,offset}$.

Upon application of an AC gate-source voltage, the gate current, ideally 0 with DC gate voltage, is caused by the capacitance between gate electrode and source plus drain electrode:

$$\tilde{I}_{G,\omega} = i\omega \left(C_{GD} + C_{GS}\right) V_{GS,\omega} \tag{54}$$

The frequency at which the gate current equals the drain current is known as the *transition frequency* f_T. It is an important limitation of the transistor in any AC application, as above this frequency, when the gate current is higher than the drain current, it is impossible to drive a second transistor with the first transistor. The approach described above yields a similar dependence of the transition frequency upon voltage, mobility and channel length as obtained by considering the charge transition time through the channel as minimal period for switching. This simple approach yields a transition frequency [91] [98] of

$$\omega_T = \frac{\mu \left|V_{DS}\right|}{L^2} \tag{55}$$

However, this relation is only valid for an ideal transistor and does not take into account any side effects present in real devices, like the contributions from parasitic capacitances from the electrode areas. To include them one has to calculate the frequency at which the gate and the drain current, determined in equations 53 and 54, are equal:

$$\omega_T \left(C_{GD} + C_{GS}\right) \approx -\frac{W}{L}\mu C_i V_{DS} \Rightarrow \omega_T \approx -\frac{WLC_i}{C_{GD} + C_{GS}} \frac{\mu V_{DS}}{L^2} = a\frac{\mu \left|V_{DS}\right|}{L^2} \tag{56}$$

where it is assumed that the first, transistor action related term dominates in equation 53. With equation 56 the correction factor

$$a = \frac{WLC_i}{C_{GD} + C_{GS}} = \frac{C_{Ch}}{C_{Ch} + (C_{GD,0} + C_{GS,0})} \tag{57}$$

to the simple $\frac{\mu V_{DS}}{L^2}$ description is obtained. a approaches unity for vanishing source and drain contact areas and becomes more prominent if their overlap with the gate electrode increases.

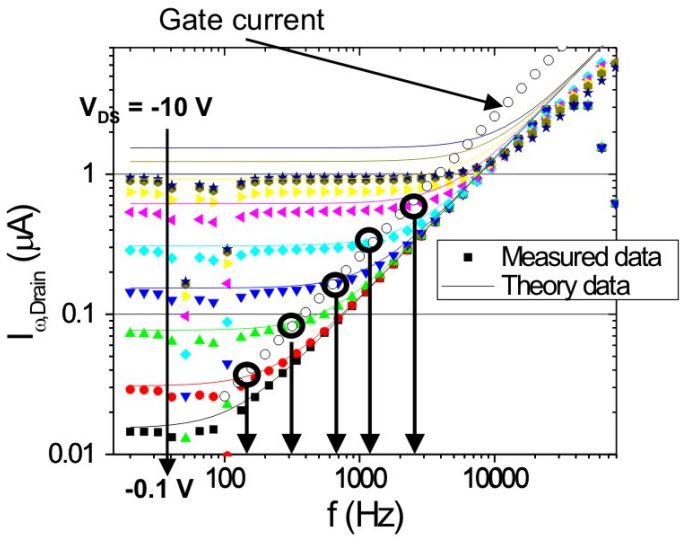

Figure 59: Measurement of AC drain current for drain-source voltages from -0.1 to -10 V, plotted over the AC frequency. The thin lines represent the theoretical predictions according to equation 53. The white points show the gate current. The crossing of the drain and gate current lines marks the transition frequency, shown by the black arrows for different drain-source voltages. L = 10 μm, W/L = 10 000, d_{P3HT} = 30 nm, $d_{Insulator}$ = 350 nm, $V_{GS,offset}$ = -10 V, $V_{GS,\omega}$ = 0.2 V

Figure 59 shows a measurement of the AC drain current plotted over the frequency for different drain-source voltages V_{DS}. The gate current is shown by the white dots. The transition frequency is determined for each drain voltage as the point where the gate current crosses the respective drain current curve, as shown by the arrows. This transition frequency in dependence on the drain-source voltage is plotted in figure 60.

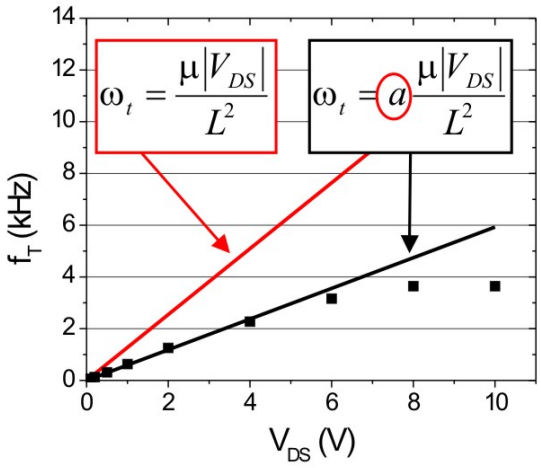

Figure 60: Determined transition frequencies for the device in figure 59 plotted over the applied drain-source voltage (black points). The lines show the predictions according to the formulas given.

The experimental data is significantly lower than a simple $\frac{\mu V_{DS}}{L^2}$ prediction. However, it agrees well with the predictions taking into account the parasitic capacitances as described above, determined by the overlap areas of the *K10* transistor structures and the charge carrier mobility extracted from the DC transfer curves of this single device. For high V_{DS}, there are obviously deviations, as the predictions for the linear regime are not valid any more.

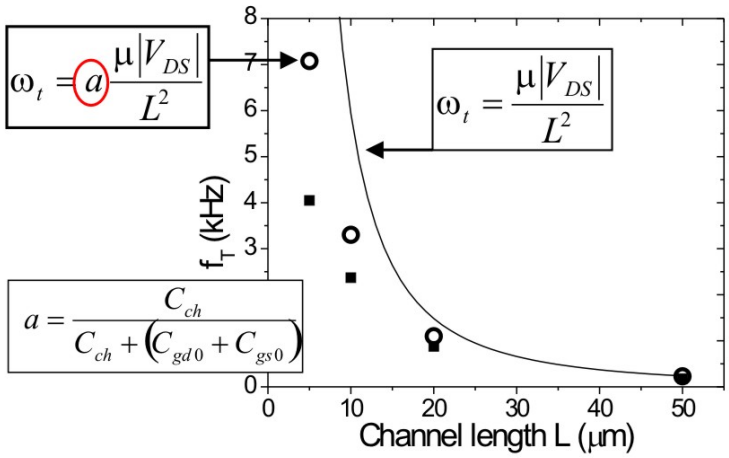

Figure 61: Transition frequency from different devices over channel length L. The line represents the behavior without parasitic capacitances. Those are included in the open circles, which were calculated according to the geometry of each device. The black points show the measured transition frequencies. d_{P3HT} = 30 nm, $d_{Insulator}$ = 350 nm, $V_{GS,offset}$ = -10 V, $V_{GS,\omega}$ = 0.2 V, V_{DS} = -4 V

In figure 61, the determined transition frequencies for different devices on the same substrate, obtained at V_{DS} = -4 V, are plotted over the channel length of the devices. All devices use a transistor layout with an electrode dimension (width of source and drain gold fingers) of 10 μm. For large channel length like L = 50 μm, the contribution of the additional parasitic capacitances can almost be neglected, and the prediction of the transition frequency including parasitic capacitances hardly differs from the standard $\frac{\mu V_{DS}}{L^2}$ prediction. However, by decreasing the channel length, the contribution of the 10 μm contact areas becomes more and more important, and the transition frequencies predicted are way lower than $\frac{\mu V_{DS}}{L^2}$.

6.3 Contact resistance

The actually measured transition frequencies, shown in figure 61 as black points, are, however, even lower than that, especially for the small channels. The reason for this is contact resistance, not taken into account until now. But obviously, in small channels, where the channel resistance of the transistor becomes smaller and smaller, the contact resistance plays a more and more prominent role, and therefore has to be included in

the model. The exact origin of contact resistance [99], its modeling (e.g. [100]) and ways to decrease it (e.g. [101]) have been an active field of OFET research until now.

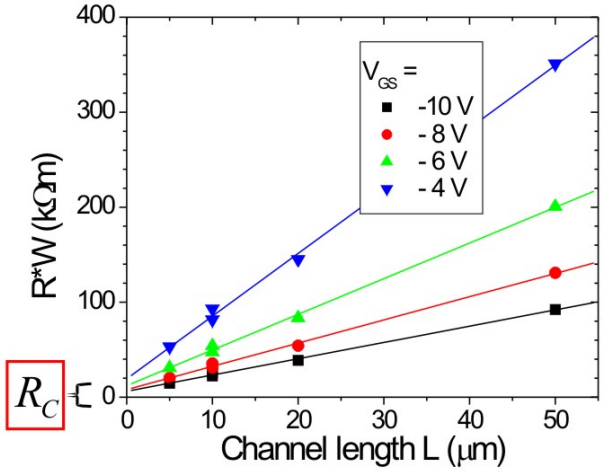

Figure 62: Total transistor resistance of different devices on the same substrate, multiplied with the channel width W, plotted over the channel length for different gate-source voltages. The slope of the resulting lines yields the sheet resistance R_S, the intercept with the y-axis the contact resistance R_C. d_{P3HT} = 30 nm, $d_{Insulator}$ = 350 nm, $V_{DS,\omega}$ = 0.2 V, $V_{DS,offset}$ = -1 V

Contact resistance can be determined with the transfer line method [102], applying a DC voltage at the gate, and the AC voltage at the drain, or in pure DC measurements. Plotting the overall resistance, multiplied with the channel width, over the channel length of the respective devices, yields straight lines for each gate voltage, as shown in figure 62. The slope yields the sheet resistance R_S of the transistor, while the y-axis intercept yields the total specific contact resistance R_C, which is the sum of the source and drain contact resistances multiplied by the channel width W. Not only does the channel resistance vary with the gate voltage, but also the contact resistance. Therefore it is practicable to calculate a value L_0, which is the length by which the transistor seems longer due to contact effects. L_0 is determined by simply dividing R_C by R_S. In this case, it is determined to be 3.6 μm. The contact effects affect the transition frequency by reducing the drain current. Due to the voltage drop at the drain and source contacts, the drain current is reduced to

$$I_D = -\frac{W}{L}\mu C_i \left(V_{GS,offset} - V_{th} + V_{GS,\omega}\right)\left(V_{DS} - \frac{R_C}{W} I_D\right) - i\omega C_{GD} V_{GS,\omega}\left(1 + i\omega C_{GD}\frac{R_C}{2}\right)^{-1} \tag{58}$$

With $|V_{GS,\omega}| << |V_{GS,offset} - V_{th}|$ and neglecting the C_{GD} capacitance related current the AC drain current becomes

$$\tilde{I}_D = \left[-\frac{W}{L}\mu C_i V_{GS,\omega} V_{DS}\right]\left(1 - \frac{W}{L}\mu C_i \left(V_{GS,offset} - V_{th}\right)\frac{R_C}{W}\right)^{-1} \tag{59}$$

As the first bracket represents the ideal current without contact effects, the additional correction factor c due to the presence of the contact resistance is obtained as

$$c = \frac{1}{1 - \frac{W}{L}\mu C_i \left(V_{GS,offset} - V_{th}\right)\frac{R_C}{W}} = \frac{L}{L - \mu C_i \left(V_{GS,offset} - V_{th}\right) R_C} \tag{60}$$

With the sheet resistance being $R_S = -\frac{1}{\mu C_i \left(V_{GS,offset} - V_{th}\right)}$, c can be written as

$$c = \frac{L}{L + \frac{R_C}{R_S}} = \frac{L}{L + L_0} \tag{61}$$

6.4 Complete model

So, in a complete model, including parasitic capacitances as well as contact resistance, the transition frequency is determined to be

$$\omega_T = a \cdot \frac{\mu \left|V_{DS}\right|}{L^2} \cdot c \tag{62}$$

with the two correction factors

$$a = \frac{C_{Ch}}{C_{Ch} + \left(C_{GD,0} + C_{GS,0}\right)} \tag{63}$$

accounting for the parasitic capacitances and

$$c = \frac{L}{L + L_0} \tag{64}$$

for the contact resistance.

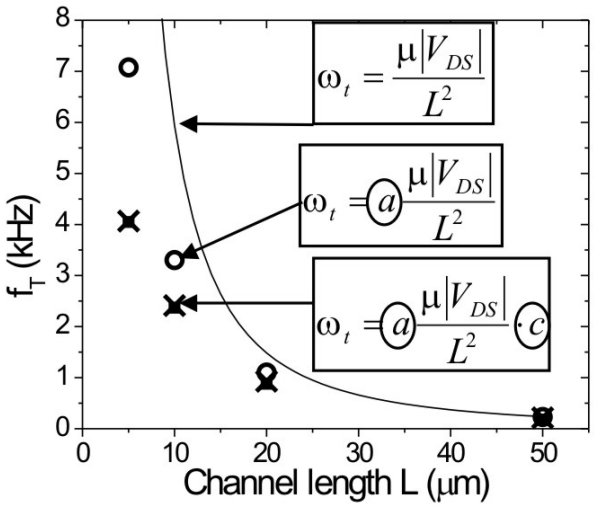

Figure 63: Transition frequency from different devices over channel length L, similar to figure 61. The crosses now represent the complete model including parasitic capacitances and contact resistance and predict very well the measured values (black points).

Figure 63 shows the validity of the presented model. The measured transition frequencies, plotted as black points, are in very good agreement with the predicted values from the complete model, calculated from the mobility determined in the DC measurements and including parasitic capacitances and contact resistance. Limiting factors towards higher frequencies are obvious from the model presented, which is not necessarily the channel length. The values of the transition frequencies are significantly lower than those calculated without contact resistance, and for the L = 5 μm case, even almost one order of magnitude lower than a simple $\frac{\mu V_{DS}}{L^2}$ prediction. It becomes clear that in order to achieve high frequencies in AC applications, it is important to reduce the channel length [90] [103] and use high-mobility materials [51]. In addition, small electrode overlap areas and especially low contact resistance are of crucial importance!

7 Conclusion

The focus of this thesis lies on questions of charge transport in disordered organic semiconductors, investigated on top-gate plastic foil OFETs with the widely used polymer semiconductor poly(3-hexylthiophene) (P3HT). In contrast to standard analysis methods, not only the charge carrier mobility, usually determined by linear (linear regime) or quadratic (saturation regime) fits to a very small part of the transfer curves, is taken into account. Instead, the complete transfer curves from gate voltages of +20 V to -20 V or +50 to -50 V, depending on the material system, are systemetically analyzed, which reveals a lot of additional physical information. In the analysis of the on-current regime of the transistor, i.e. at gate voltages below the threshold voltage (for p-type transistors), the more than linear increase of the current with gate voltage in the linear regime and the more than quadratic increase in the saturation regime due to charge carrier density dependence of the charge carrier mobility are taken into account by fitting the transfer curves with a gate-voltage dependent mobility. This fit yields three parameters for analysis: threshold voltage, charge carrier mobility at a fixed distance from the threshold voltage, and the exponent that describes the increase of mobility with gate voltage. While the charge carrier mobility is a measure of the overall quality of the transistor channel, its exponent is directly related to energetic disorder in the channel, reflecting the width of the density of hopping states. The threshold voltage, an important parameter for switching off the device, informs about residual charges in the transistor channel which provide current even without any applied gate field. It is determined as the true voltage at which the transistor channel is depleted of carriers, which can not be provided by any standard linear or quadratic fit. As the transistor current is found not to be zero even above the threshold voltage due to residual charges in the bulk of the semiconductor, this part of the transfer curves also is included in the analysis. The bulk current contains information on bulk conductivity and doping level and, together with the threshold voltage, determines the off-current, which is crucial for the on/off ratio of a transistor.

All these parameters are analyzed with respect to their dependence on the semiconductor layer thickness in chapter 5, with the thickness varied from just a few nanometers to the maximum which is possible due to the limited solubility of P3HT in the used solvents. It was found that the mobility is very low in thin films of P3HT, but increases drastically over two orders of magnitude with increasing thickness. However, the mobility does not increase any further above a saturation thickness of around 50 nm. This finding is explained by the behavior of the exponent with which the mobility increases with gate voltage. The exponent is very high in thin films and strongly decreases with increasing film thickness, eventually reaching a saturation value as well. This shows that thin films exhibit high energetic disorder, but the ordering is largely improved in thicker films. The result is confirmed by AFM phase contrast measure-

ments which show that the structural ordering also is larger in thicker P3HT films, with the size of the semiconductor grains distinctly increasing with the layer thickness. While thin films are highly disordered due to interfacial strain to the substrate, the distance of the layer surface, which becomes the interface to the gate insulator at which the transistor channel is situated, to the substrate increases in thicker films and the substrate influence is reduced. However, very thick P3HT films show increased surface roughness, which compensates the improvement in grain size and leads to the saturation of the mobility. Transistors with P3HT processed from solution in toluene, which has a higher boiling point than chloroform so that there is more time for formation of a well-ordered layer, generally exhibit higher mobility and lower energetic disorder, and the maximum ordering is achieved at lower semiconductor thickness than by using chloroform as P3HT solvent. The bulk current remaining at the threshold voltage is found to be proportional to the semiconductor thickness, and the depletion of the semiconductor bulk upon further increase of the gate voltage is dramatically slowed down in thicker films. Therefore, the thickness at which saturation in mobility occurs is also the optimum in the on/off ratio.

Transistor characteristics are also analyzed with respect to their dependence on temperature, from liquid nitrogen temperature to ca. 90°C. The result is compared to the predictions of different charge transport models. The mobility is found to increase monotonically with temperature. However, no pure $exp\left(-\frac{1}{T}\right)$ behavior as typical for the MTR model can be observed. The same applies to the $exp\left(-\frac{1}{T^2}\right)$ dependence of the mobility predicted by the Gaussian Disorder Model and the Correlated Disorder Model. On the other hand, the progression of the mobility with increasing temperature is in very good agreement with the prediction made by the charge transport model of Vissenberg and Matters. In this model, the slope of the mobility increase with temperature is determined by the localization length of the charge carriers, which can thus be determined from the measurement. The model also includes, in contrast to e.g. the MTR model, the clearly observed dependence of the mobility on charge carrier density. While this parameter decreases with increasing temperature, the decrease is not as strong as predicted by the model. This can be attributed to a different description of the density of hopping states than the purely exponential relation assumed by Vissenberg and Matters. With this modification done, the temperature and carrier concentration dependence of the transistor characteristics can be described by the model in an excellent way. The bulk conductivity, which dominates above the threshold voltage, is shown to follow a temperature dependence which can be directly derived from the channel mobility.

While the mobility and its dependence on carrier density vary so strongly with temperature and can be optimized by tuning the semiconductor thickness, the threshold voltage is not significantly affected in these experiments. However, it is strongly shifted

even by small chemical variations in the solvent of the insulator which is applied on top of the semiconductor. It has been demonstrated that addition of acid to the solvent in the range of 100 ppm makes the threshold voltage distinctly more positive. In the same way, addition of another solvent, which shifts the chemical equilibrium towards the original solvent and away from the acid, shifts the threshold voltage in the desired direction, towards more negative values, tremendously increasing the on/off ratio of the transistors. This behavior is due to the creation of charges in transistor channel and bulk upon the presence of acidic media, which cause a higher number of charge carriers present at zero field and thus require a higher positive gate voltage in order to deplete the semiconductor of charges and turn off the device.

In chapter 6, the maximum frequency has been investigated in devices with different transistor geometry. As expected, the frequency is proportional to the charge carrier mobility and inversely proportional to the square of the transistor channel length. However, the measured transition frequency does not increase as much as predicted by this simple description. One reason for this are the parasitic capacitances between the gate electrode and the source and drain electrodes which reduce the transition frequency according to their overlap in the transistor design. The second essential reduction factor for the frequency is shown to be the contact resistance which occurs due to charge injection and extraction into and out of the channel. The contact resistance is determined with the transfer line method and shown to feature the same gate-voltage dependence as the channel resistance, thus behaving like an additional channel length. Its ratio to the real channel length gives a further reduction of the transition frequency. A complete model is presented which predicts the transition frequency from the DC device characteristics and the transistor geometry and accurately describes the measurements.

These detailed chapters on transistor modeling are preceded by a brief introduction into the subjects this thesis addresses (chapter 1), a description of the basic mechanisms of charge transport in disordered systems including an overview on existing transport models (chapter 2), and a short summary of the experimental details (chapter 3).

Chapter 4 is dedicated to the search of an optimized semiconductor / insulator material combination. The analysis shows the higher charge carrier mobility of P3HT with higher regio-regularity. On the other hand, because of a more positive threshold voltage, the off-current (measured at $V_{GS} = 0$ V) is increased even more than the on-current, and the on/off ratio therefore decreased. A large increase in performance upon utilization of high boiling point solvents is demonstrated, with a mobility increase of almost one order of magnitude for P3HT spin-coated from solution in toluene instead of chloroform. Measurements with a wet-chemically processed n-type semiconductor in an otherwise unchanged sample setup (same substrate, same insulator) demonstrate the feasibility of logic circuits. In addition to these semiconductor tests, two different

solution-processable organic insulator materials have been tested and applied from solutions in various solvents. These investigations reveal the crucial influence of insulator material and solvent on the transistor characteristics due to the fact that the insulator is applied directly on the semiconductor surface, exactly where the charge transport in a top-gate transistor takes place. Therefore optimization of the transistor performance can never be achieved by tuning the semiconductor layer alone, but optimal mobility, threshold voltage etc. strongly depend on the choice of a suitable insulator and solvent. In cooperation with other group members and project partners, a device layout and measurement system was developed which allows the production and measurement of a large number of devices, so that all results presented in this thesis are extracted from the statistical analysis of a large number of equal transistors and guarantee high reliability.

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